Mixed-Signal-Controlled Flyback-Transformer-Based Buck Converter With Improved Dynamic Performance and Transient Energy Recycling

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***Abstract*—This paper introduces a practical modification of the buck converter and a complementary controller that are well suited for point of load applications with highly dynamic loads. The presented flyback-transformer-based buck (FTBB) converter has faster transient response than the conventional buck, allowing for a reduction in the output capacitance without penalty in the size of the magnetic core. During heavy-to-light load transients, the FTBB converter also recycles excess energy stored in the magnetic component, providing a useful energy savings mechanism. In this modification, the conventional buck inductor is replaced with the primary winding of the flyback transformer, an extra switch, and a set of small auxiliary switches on the secondary side. During heavy-to-light load transients, the inductor current is steered away from the output capacitor to the input port, achieving both energy recycling and savings due to reduced voltage overshoots. The light-to-heavy transient response is improved by reducing the equivalent inductance of the primary transformer winding to its leakage value. A mixed-signal current-programmed mode controller regulates operation of the converter. The controller provides minimum output voltage deviation and ensures seamless transitions between different operating modes. The performance of the FTBB converter is verified with a 6-to-1-V, 3-W, 390-kHz experimental prototype. In comparison with an equivalent buck converter, the experimental system has about three times smaller maximum output voltage deviation, allowing for the same output capacitor reduction and, for frequently changing loads, about 7% decrease in power losses.**

***Index Terms*—DC-DC power converters, digital control, energy efficiency, flyback transformers, switched-mode power supply, transient response.**

I. Introduction

IN MODERN low-power applications such as mobile devices, consumer electronics, and communication equipment, point-of-load (PoL) switch-mode power supplies (SMPSs) are required to provide tightly regulated voltage having small deviation during load transients. In these systems, usually operating with an output voltage no larger than 1 V, the SMPS output voltage deviation is strictly limited to ensure proper system performance [1]–[3]. It is also of key importance to minimize the volume of the SMPS reactive components, i.e., their output filters, which in the targeted applications usually occupy a large portion of the entire unit [4].

To achieve tight output voltage regulation and minimize the size of reactive components, operation at a high switching frequency and fast control methods are usually required. The high-frequency operation minimizes the size of filter components. However, this improvement comes at the price of a power conversion efficiency degradation due to increased switching losses [5].

With the emergence of digital control in low-power SMPS, a number of recent methods [6]–[17] drastically improve the dynamic response of converters, thus minimizing the size of the output capacitor. Arguably, the time-optimal [6]–[15] and minimum-deviation [16], [17] controllers are among the most effective. In the time-optimal-controlled systems [6]–[13], the converter recovers from a transient through a single ON–OFF switching action, in practically minimum possible time. However, this process usually exposes components to a much larger current than nominal. In minimum-deviation controllers [16], [17], the peak current is limited to the nominal value at the expense of a longer recovery time after the initial output voltage deviation has been suppressed. Ideally, for a conventional buck converter, both of these controllers respond to a load transient with minimum possible output voltage deviation, allowing the maximum reduction in the size of the filtering capacitor. However, the reduction is limited by the physical constrains of a given power stage, namely by the slew rate of the inductor current charging the output capacitor during transients [18], [19]. This rate is proportional to the ratio of the voltage applied across the inductor and the inductance value [5]. For converters with low output voltage, this value is usually fairly small; hence, a relatively large output capacitor is still required [18], [19].

To overcome the inductor current slew-rate limitations, numerous modifications of the buck topology have been proposed [20]–[43]. In these systems, during load transients, the converter dynamically changes its own configuration to improve the output capacitor charging/discharging rate. In general, these methods can be divided into the inductor slew-rate and/or current-steering-based improvements [20]–[23], current injection methods [24]–[40], and stepping-inductor-based solutions [41]–[43].

In the inductor slew-rate and current-steering improvement methods [20]–[23], several additional switches are added to the current conduction path. They are used to increase the voltage

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across the filter inductor and drastically improve the current slew rate. For heavy-to-light load transients, the slew-rate improvement is sometimes combined with the steering of the inductor current away from the output capacitor, to further reduce the capacitor energy storage requirements [20], [21]. These solutions are better suited for the buck–boost than for the buck configuration [21]. This is because the extra switches already existing in the current conduction path do not have a significant effect on the conduction losses.

Injection methods [24]–[40] use a small parallel auxiliary stage to inject extra charge into the output capacitor. Examples include additional circuits consisting of a smaller converter [24]–[31], transformers [32]–[34], an *LC*/*RC* network [35]–[38], or a pair of linearly controlled active clamps [39], [40]. The auxiliary circuit is activated during transients, to help inject or remove the charge from the output capacitor, drastically minimizing its energy storage requirements. Yet, for frequent transients, the auxiliary circuit usually decreases the converter efficiency. In some cases, the reduction in capacitance comes at the price of a noticeable increase in the overall inductance size and volume.

In the stepping-inductor buck converter [41]–[43], the conventional inductor is replaced with a three-winding structure. The secondary and tertiary windings are used during transients, for reduction of the equivalent inductance to the transformer leakage value and the current slew-rate improvement. This modification effectively minimizes the output capacitor with a minor increase in the inductance volume and with no extra switches added to the main conduction path. However, this previously reported solution is not the most suitable for the targeted low-voltage applications due to the limitations of the power transistors' blocking voltage. In low-power applications, the transistors are usually integrated with the controller, and implemented in a cost-effective low-voltage CMOS technology. These transistors can only handle a voltage slightly larger than the supply, limiting the ability of the stepping-inductor systems to improve heavy-to-light transient response. During the transients, the reflected auxiliary winding voltage reduces the voltage across the leakage inductor [43] to a very low value. As a consequence, the benefit of an improvement in the current slew rate using the stepping inductor is canceled. An attempt to minimize this problem by increasing the windings turns ratio would significantly increase the blocking voltage requirements for the auxiliary-side transistors. The blocking voltage requirement could be several times higher than the supply voltage, preventing cost-effective implementation and possible on-chip integration.

The main goal of this paper is to introduce a practical low-voltage power supply that overcomes current slew-rate limitations of the conventional buck converter, allowing a reduction in the output capacitance with a low or no penalty in the power conversion efficiency and the overall inductance size and volume. The flyback-transformer-based buck (FTBB) converter and a complementary mixed-signal controller as shown in Fig. 1 combine the stepping-inductor and the current-steering concepts. Here, the inductor is replaced with a conventional flyback transformer of approximately the same size. The converter also has an extra power switch S_0 on the primary side and several small switches on the secondary side of the transformer. For frequently

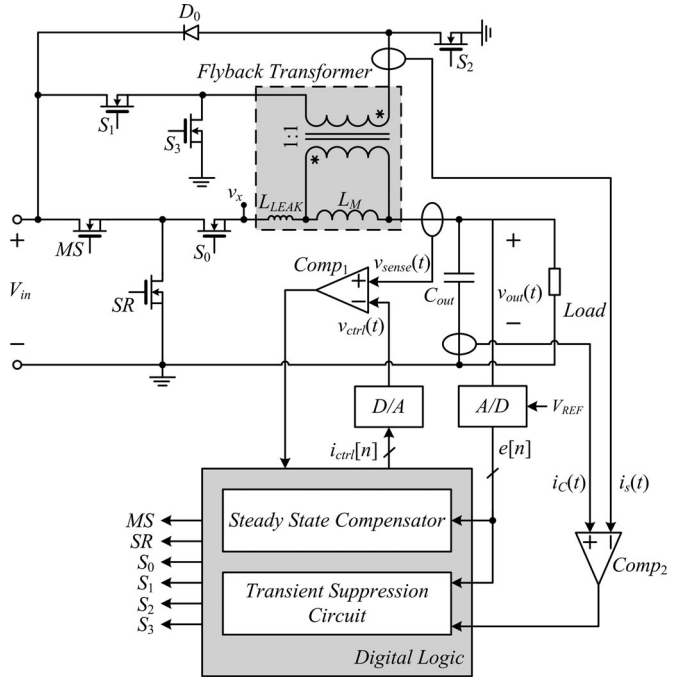

Fig. 1. FTBB converter and the complementary mixed-signal controller.

changing loads, the extra conduction losses introduced by the switch S_0 are partially or completely compensated by energy recycling ability of this topology that sends energy back to the power source during heavy-to-light transients. This energy savings mechanism can potentially extend the battery life of modern portable devices, in which most of the loads are digital in nature and changing very frequently [44], [45].

The penalty in the overall inductance volume of the introduced system is smaller than in other solutions [24]–[34]. The size of the magnetic core, the largest contributor to the overall size of the magnetic components in low-power applications [5], is no larger than that of a conventional buck converter. The inductor only requires an additional winding, rated for a much smaller average current than that of the primary winding.

The introduced FTBB converter does not require transistors with overly large blocking voltage, an undesired characteristic for conventional stepping-inductor solutions [41]–[43]. Here, the transistors are required to block voltages no larger than the input voltage $V_{\rm in}$. Hence, the presented solution is better suited for cost-effective integration.

A mixed-signal current-programmed mode (CPM) controller [46]–[48] governs the operation of the converter as shown in Fig. 1. The voltage loop processes digital signals and, through a D/A converter, gives a reference to the analog current loop. The controller also contains a transient suppression block that activates auxiliary circuits during transients and ensures seamless transitions between different modes.

The paper is organized as follows. Section II explains operation of the presented FTBB converter. In Section III, the architecture of the mixed-signal controller is described, with particular focus on the seamless transition between the transient and steady-state modes of operation. Section IV discusses

the design tradeoffs, the influence of additional switches on the system efficiency, and the loss compensation through energy recycling. This section also shows an analysis of the efficiency for the FTBB converter as a function of the load change frequency. It also explains why the FTBB converter is more efficient than the conventional buck converter for frequently changing loads. Results obtained with a 6-to-1-V, 3-W experimental prototype that verify the performance of the FTBB converter are presented in Section V. Section VI concludes this paper.

II. System Description and Operating Principle

The converter in Fig. 1 is a modification of a conventional buck converter. The inductor of the power stage is replaced by a 1:1 flyback transformer. The flyback transformer is modeled as an ideal transformer with added leakage and magnetizing inductances, $L_{\rm LEAK}$ and L_M, respectively. The total inductance on the primary side is $L_M + L_{\rm LEAK}$. A switch S_0 is also inserted in the main conduction path in series with the primary winding. The secondary winding of the flyback transformer is connected to three auxiliary switches S_1–S_3, and a free-wheeling diode D_0. The leakage inductance associated with the secondary winding is neglected since it does not have a significant influence on the system operation.

As described in the following sections, the converter operates in three different modes. In steady state, it behaves as a conventional buck converter, utilizing the primary-side inductance. During heavy-to-light load transients, it steers the magnetizing current away from the capacitor, to the voltage source. This minimizes the output capacitor overcharge and, at the same time, recycles a portion of the energy that would have been lost otherwise. To suppress light-to-heavy transients, it utilizes the stepping-inductor concept, where the equivalent inductance on the primary side is reduced to the leakage value. In this way, the current slew rate is improved.

A mixed-signal CPM controller regulates the operation. In steady state, the controller operates as a conventional system [5]. During transients, it utilizes two different optimum-deviation algorithms to achieve recovery with minimum possible voltage deviation.

A. Steady-State Operation

When the output voltage $v_{\rm out}(t)$ is within a predetermined tolerance band near the voltage reference, the system is in steady state. Switch S_0 is kept ON and the auxiliary switches S_1–S_3 are kept OFF, and the converter functions in a conventional buck configuration with output filtering inductance $L_M + L_{\rm LEAK}$. Here, all of the transistors on the secondary side are kept OFF to prevent possible current paths through the body diodes.

In this mode, the mixed-signal controller in Fig. 1 indirectly regulates the output voltage, by varying the inductor current. It uses an A/D converter to compare the output of the converter with the voltage reference $V_{\rm REF}$ and create a digital equivalent of the output voltage error value, signal $e[n]$. This signal is passed to the steady-state compensator that creates a digital reference for the current loop $i_{\rm ctrl}[n]$. The current reference $i_{\rm ctrl}[n]$ is then converted into an analog equivalent $v_{\rm ctrl}(t)$, through a D/A converter and compared with the signal from a primary current-sensing circuit $v_{\rm sense}(t) = R_s \times i_p(t)$, where R_s is the "gain" of the current-sensing circuit and $i_p(t)$ is the current flowing through the primary winding. In this way, the output voltage $v_{\rm out}(t)$ is indirectly regulated.

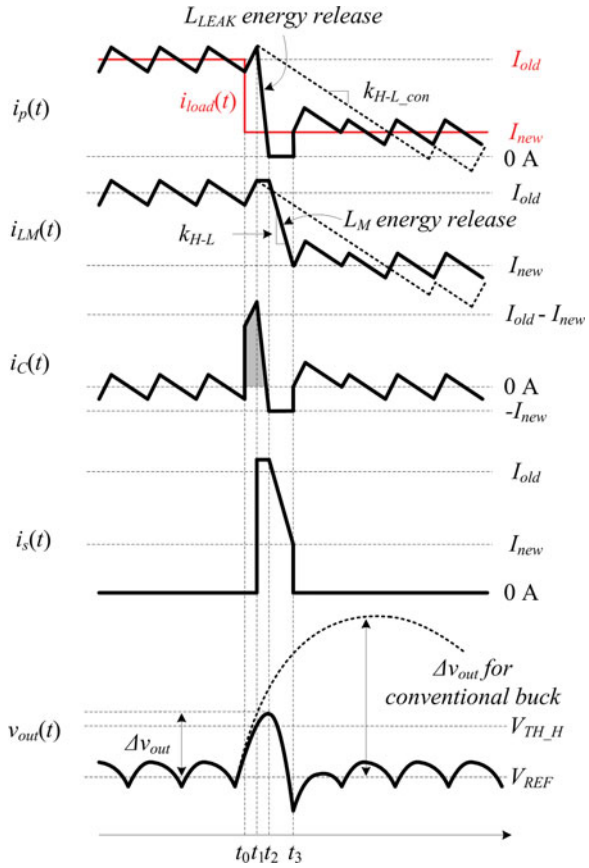

Fig. 2. Key current and voltage waveforms during a heavy-to-light load transient recovery.

B. Heavy-to-Light Load Transient Recovery

The recovery from a heavy-to-light load transient is conducted in two phases (as shown in Fig. 2). In the first phase, the stored energy of the leakage inductance is released without causing a large voltage stress across transistors. In the second phase, the output voltage deviation is suppressed, through magnetizing inductor current steering. In the following sections, two methods for the leakage inductance energy release (for relatively large and small values of $L_{\rm LEAK}$) are presented as well as the subsequent current-steering technique.

1) Leakage Inductance Energy Release (Large $L_{\rm LEAK}$ Case): The initial phase of a heavy-to-light load transient response for a relatively large $L_{\rm LEAK}$ can be described by the key current and voltage transient waveforms and the equivalent converter circuits as shown in Figs. 2 and 3(a), respectively.

The converter initially operates with a load current $i_{\rm load}(t) = I_{\rm old}$. At t_0, the load current steps down to a new value $I_{\rm new}$ causing a positive capacitor current $i_C(t)$. This change is detected when the output capacitor voltage increases beyond the

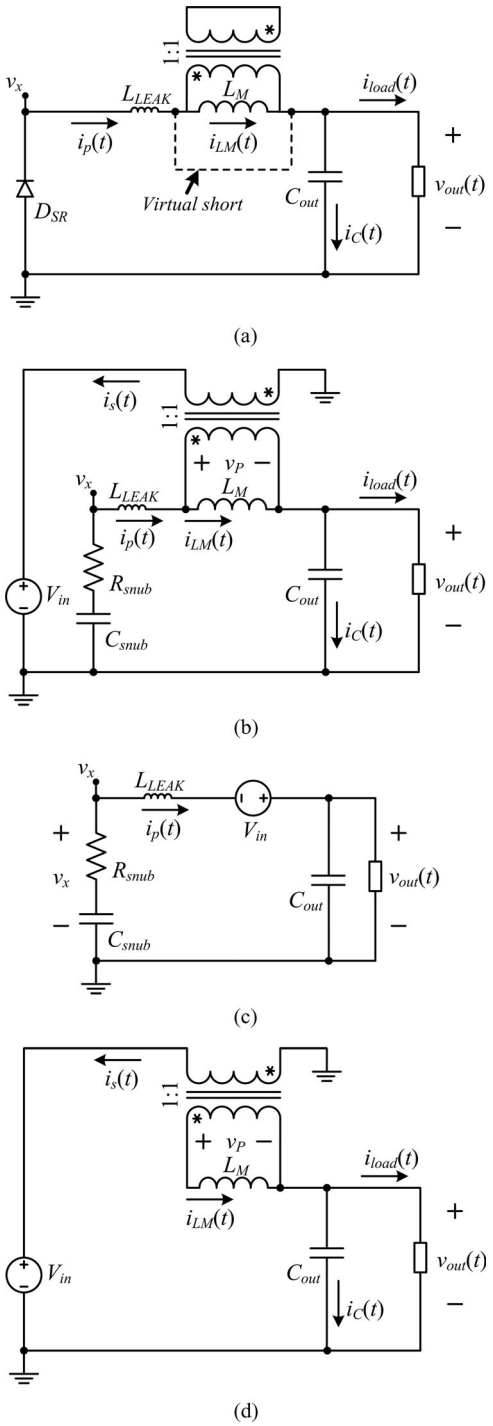

Fig. 3. Equivalent circuits during leakage inductance energy release (t_1–t_2) for (a) large $L_{\rm LEAK}$ and (b) small $L_{\rm LEAK}$. (c) $L_{\rm LEAK}$ energy released through an *RC* snubber circuit. (d) Equivalent circuit of the converter during magnetizing inductor current steering (t_2–t_3).

threshold value $V_{\rm TH\_H}$ at $t = t_1$, causing the converter to enter transient suppression mode. At this point, the main switch, MS, and the synchronous rectifier, SR, are switched OFF and S_2 and S_3 are turned ON (see Fig. 1) to release the energy stored in the leakage inductance. As a result, the body diode of the SR starts conducting, forming the equivalent circuit as shown in Fig. 3(a). In this way, a virtual short circuit is created across the magnetizing inductance L_M while the energy in $L_{\rm LEAK}$ dissipates via the body diode of SR, $D_{\rm SR}$. Now, the primary current, i.e., the leakage inductance current $i_p(t)$, quickly drops to zero with a slew rate of $(V_{\rm out} + V_D)/V_{\rm LEAK}$, where V_D is the forward voltage drop of $D_{\rm SR}$. When $i_p(t)$ reaches the zero value, $D_{\rm SR}$ turns OFF. At this point, the energy release process is complete and only the magnetizing current $i_{\rm LM}(t)$ circulates through the transformer. The primary current-sensing circuit detects this condition and initiates the following phase, i.e., voltage recovery and the magnetizing current-steering process.

Ideally, the previously described procedure results in the leakage inductance energy release without exposing transistors to a high voltage stress. Also, this procedure does not require an extremely fast zero-current detection circuit, since after the $D_{\rm SR}$ turns OFF, the leakage current remains zero.

However, in practice, problems can arise due to the reliance on the body diode of SR. Compared to the current slew rate, this diode is relatively slow and, as a consequence, the voltage spikes still might occur. To minimize this problem, a Schottky diode can be added in parallel with $D_{\rm SR}$. Alternatively, instead of using the body diode, the transistor SR can be kept ON during the leakage inductance recovery phase. However, such a solution would require a very fast zero-current detection circuit and/or an *RC* snubber to absorb any energy left in the leakage inductance due to nonideal zero-current detection.

2) Leakage Inductance Energy Release and Snubber Circuit for a Small $L_{\rm LEAK}$: For high-quality flyback transformers with a very low $L_{\rm LEAK}$, the detection of zero leakage current can be eliminated. The energy stored in $L_{\rm LEAK}$ can be absorbed by the use of a small *RC* snubber. In this case, at $t = t_1$, MS and S_0 are switched OFF; S_1 and S_2 are switched ON (see Fig. 1). The SR is also switched ON to limit the voltage stress on the transistor S_0 and the circuit in Fig. 3(b) is formed. Now, as can be seen from Fig. 3(c), a negative voltage across $L_{\rm LEAK}$ is applied and the snubbing resistor $R_{\rm snub}$ absorbs its stored energy. To protect S_0, by ensuring that the voltage $v_x(t)$ never drops below $-V_{\rm in}$, the snubber resistor $R_{\rm snub}$ is selected such that $R_{\rm snub} \times I_{\max} < V_{\rm in}$, where $I_{\max}$ is the maximum load current.

In addition to eliminating the need for zero leakage inductance current detection, this circuit also has less frequent switching action than the previously shown implementation. As will be described in the next section, the state of the switches is the same as in the next phase of the transient recovery process. However, these advantages come at the price of the snubber circuit losses.

3) Suppression of the Output Voltage Overshoot Through Current Steering: At the end of the leakage energy release phase, the switches are set such that the equivalent circuit in Fig. 3(d) is formed. Transistors MS and S_0 are turned OFF while SR, S_1, and S_2 are in ON position.

During this portion of the recovery period (t_2 to t_3), the energy stored in L_M is recycled by steering the current $i_{\rm LM}(t)$ to the input voltage source via the secondary winding current $i_s(t)$, and the load current is fully supplied by the output capacitor $C_{\rm out}$, allowing $v_{\rm out}(t)$ to drop. As a result, the problem of large capacitor current causing the output voltage overshoot

in the conventional buck [16] is eliminated. During this time, a constant voltage $v_p = -V_{\rm in}$ is applied across the magnetizing inductance, where $V_{\rm in}$ is the input voltage of the converter.

In addition to stopping the capacitor from being overcharged, the FTBB converter also improves the current slew rate. During a heavy-to-light load transient, the magnetizing current decreases at the rate

$$k_{H\_L} = \frac{v_{\rm p}}{L_M} = \frac{-V_{\rm in}}{L_M}. \tag{1}$$

This is significantly higher than that of an equivalent conventional buck converter [16]

$$k_{H-L\_{\rm con}} = \frac{-V_{\rm out}}{L} \tag{2}$$

where $L = L_M + L_{\rm LEAK}$ is the output filter inductance of the conventional topology. The improved slew rate is mostly due to the input voltage value, which is usually significantly higher than $V_{\rm out}$. As a result, the transient recovery process is significantly faster.

A minimum-deviation controller [16] is used to govern the operation of the converter during transients. As described in the following section, this controller completes its action when the inductor current $i_{\rm LM}(t)$ reaches the new load current $I_{\rm new}$, at $t = t_3$. At this point, the steady-state operation mode is resumed and the CPM controller reactivated.

For a potential full on-chip implementation of this system, issues related to the presence of negative switching node voltage $v_x = -(V_{\rm in} - V_{\rm out})$ during this phase need to be addressed. This negative value would cause the source/drain to substrate junction of switch S_0 to become forward biased. This problem could be solved if silicon on insulator technology is available. However, cost and thermal resistance issues would have to be considered. An alternative is to use a substrate bias that is lower than v_x, but this would introduce other nonideal requirements such as an extra negative bias voltage and power devices with breakdown voltage that is at least twice as high. Another possible option to circumvent this issue is to implement switch S_0 on a separate die. This would allow both the separation of its substrate connection from the rest of the converter and a cost-effective implementation in a low-voltage process.

C. Light-to-Heavy Load Transient

Recovery from light-to-heavy load transients is performed using the stepping-inductance principle [41]–[43], where a sequence of current pulses reversing the output voltage drop is created during a gradual recovery of the magnetizing current.

The key converter waveforms during a transient are as shown in Fig. 4. At t_0, $i_{\rm load}(t)$ steps to a higher value $I_{\rm new}$, causing a negative capacitor current $i_C(t)$ and a decrease of the output voltage $v_{\rm out}(t)$. When $v_{\rm out}(t)$ drops below the lower tolerance threshold $V_{\rm TH\_L}$, at $t = t_1$, the transient recovery mode is activated, by turning OFF SR and turning ON transistors MS, S_0, S_2, and S_3, over a fixed period $t_{\rm pulse}$. This forms the equivalent circuit shown in Fig. 5(a). A virtual short circuit across L_M is formed and the equivalent inductance of the main current path reduces to the leakage value $L_{\rm LEAK}$. In this way, the current

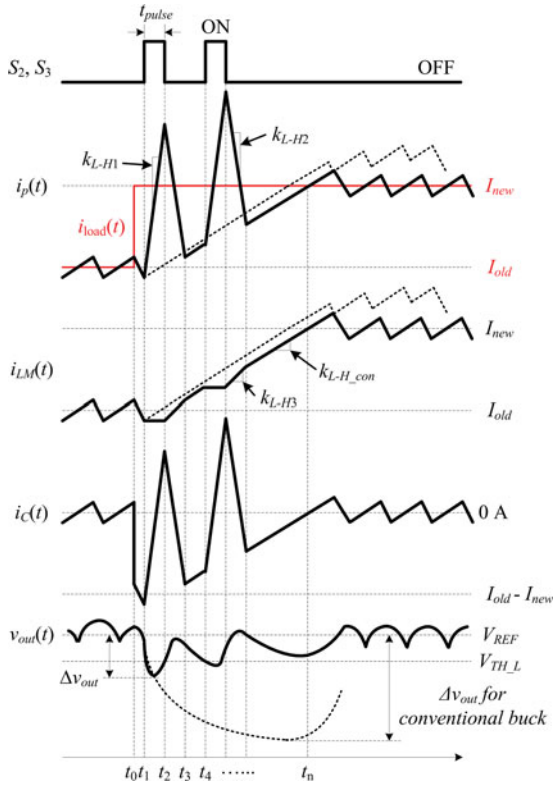

Fig. 4. Key current and voltage waveforms during a light-to-heavy load transient recovery.

slew rate of the primary side of the transformer is drastically increased to the value

$$k_{L-H1} = \frac{(V_{\rm in} - V_{\rm out})}{L_{\rm LEAK}} \tag{3}$$

and a current pulse is formed. As shown in Fig. 4, this pulse reverses the output voltage drop, over the period t_1 to t_2. During this time, the magnetizing current $i_{\rm LM}(t)$ remains constant.

To increase the magnetizing current, at $t = t_2$, S_2 and S_3 are turned OFF. During this time, the energy stored in $L_{\rm LEAK}$ is passed through the transformer and recycled to the input source through the free-wheeling diode D_0 (see Fig. 1) and the body diode of S_3, D_{S3}. Now, the equivalent circuit in Fig. 5(b) is valid, and the current $i_{\rm LM}(t)$ increases with the slew rate

$$k_{L-H3} = \frac{(V_{\rm in} + 2V_D)}{L_M} \tag{4}$$

where V_D is the forward voltage drop of diodes D_0 and D_{S3}. During this time, the primary current reduces with the rate

$$k_{L-H2} = \frac{(V_{\rm out} + 2V_D)}{L_{\rm LEAK}}. \tag{5}$$

This process continues until the currents $i_{\rm LM}(t)$ and $i_p(t)$ become equal and the current $i_s(t)$ in the secondary side reaches zero, forming the equivalent circuit in Fig. 5(c). This happens at the time instant t_3 (see Fig. 4). From this point on, the slew rate of the inductor current is equal to that of the conventional buck converter and the capacitor current is negative again. The converter remains in this configuration until the output voltage

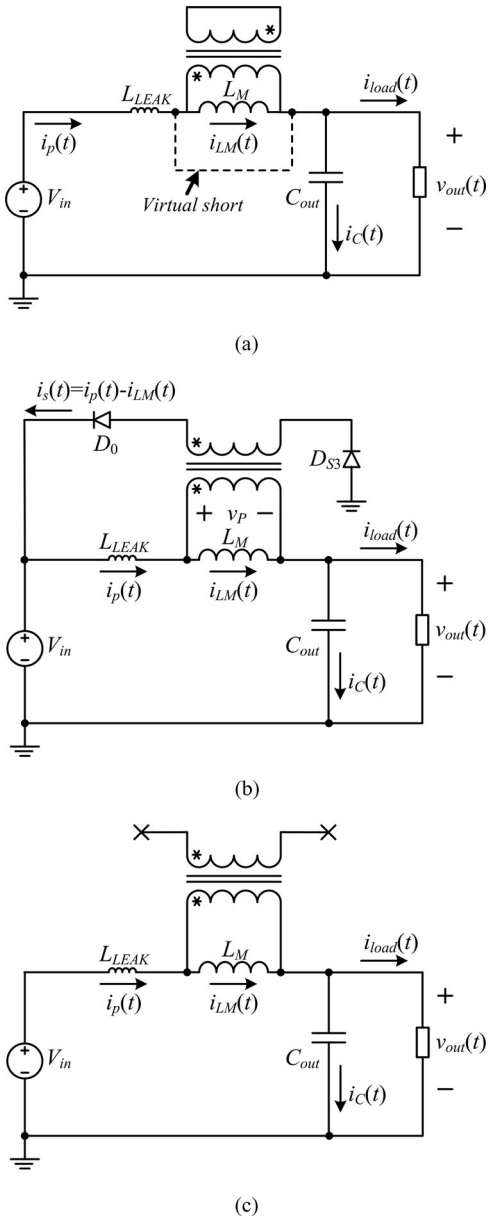

Fig. 5. Equivalent circuits of the converter when (a) current pulses in $i_p(t)$ suppress voltage undershoot (t_1–t_2). (b) Extra energy in $L_{\rm LEAK}$ is recycled to the input power source (t_2–t_3). (c) Currents $i_{\rm LM}(t)$ and $i_p(t)$ increase with a slew rate equal to an equivalent conventional buck converter (t_3–t_4).

drops beyond the lower threshold value $V_{\rm TH\_L}$ again, at $t = t_4$, and the secondary circuit is reactivated. The whole sequence is repeated until the magnetizing current $i_{\rm LM}(t)$ reaches the new load value $I_{\rm new}$. At that time instant, i.e., $t = t_n$ in Fig. 4, the steady-state mode of operation is resumed. As can be seen from Fig. 4, which also shows comparative waveforms of a minimum-deviation-controlled conventional buck converter [16], the FTBB converter has faster voltage recovery and much smaller output voltage deviation, even though the inductor current recovery is slightly delayed.

It should be noted that the problem of relying on the relatively slow body diode of the transistor S_3 for the leakage inductance energy release could occur in this case as well. However, in this case, the solution is fairly simple. Instead of using the body diode, the transistor S_3 can be kept ON during the interval described with Fig. 5 (b) and the soft switching achieved with the dedicated faster diode D_0. Then, S_3 can be turned OFF with zero current during the interval described with Fig. 5(c).

D. Inductor Volume

The previous discussion indicates that the inductor core volume of the FTBB converter is no larger than that of the conventional buck converter. In steady state, the energy storage requirements are the same, i.e., the FTBB converter requires the same inductance and current values, allowing the core of the same size to be used. During transients, the flux through the core used in the FTBB converter, defining its volume, is also no larger than that used in the conventional buck converter. As can be seen from Figs. 3 and 5, the action of auxiliary circuit practically results in zero net flux increase through the transformer core. This is due to the fact that the flux from the current in the secondary winding $i_s(t)$ cancels the one created by the current $i'_p(t) = i_p - i_{\rm LM}$. The FTBB converter requires only one small additional winding to handle $i_s(t)$, whose average value is much smaller than that of the primary winding current.

III. Controller Implementation

The controller in Fig. 1 provides signals for the switches of the FTBB converter in all modes of operation and also ensures seamless transitions between different modes. These include transitions between steady state and transients as well as transitions during transient, as described in the previous section.

A block diagram of the controller is shown in Fig. 6 and its operation is described by the state diagram in Fig. 7. It consists of two comparators, an A/D converter, a D/A converter, and fairly simple digital logic. The main functional blocks of the digital part are transient detector, proportional-integral (PI) compensator and transient current estimator, MS and SR switch selector, clock selector, and transient suppression logic.

The output voltage of the FTBB converter $v_{\rm out}(t)$ is quantized to its digital equivalent $v_{\rm out}[n]$, by the A/D converter at a sampling rate eight times higher than the switching frequency $f_{\rm sw}$. This digital value is then compared to the desired reference $V_{\rm REF}[n]$ to obtain the voltage error signal $e[n]$. This error is monitored by the transient detector that determines the mode of operation. The converter operates in steady-state mode of operation when there are no load transients, or disturbances are small, so the error voltage is smaller than the predefined threshold $e_{\rm TH}[n]$. Here, the threshold is a design parameter that, as described in the next section, is determined experimentally. Alternatively, a dedicated analysis could potentially be conducted to find the exact relation between the threshold setting and voltage overshoot values. Such an analysis would need to take into account the size and the slope of the load current steps, position of the step with respect to the state of the converter switches, system delays, filter component values, as well as influence of the output capacitor's equivalent series resistance (ESR) and other parasitic.

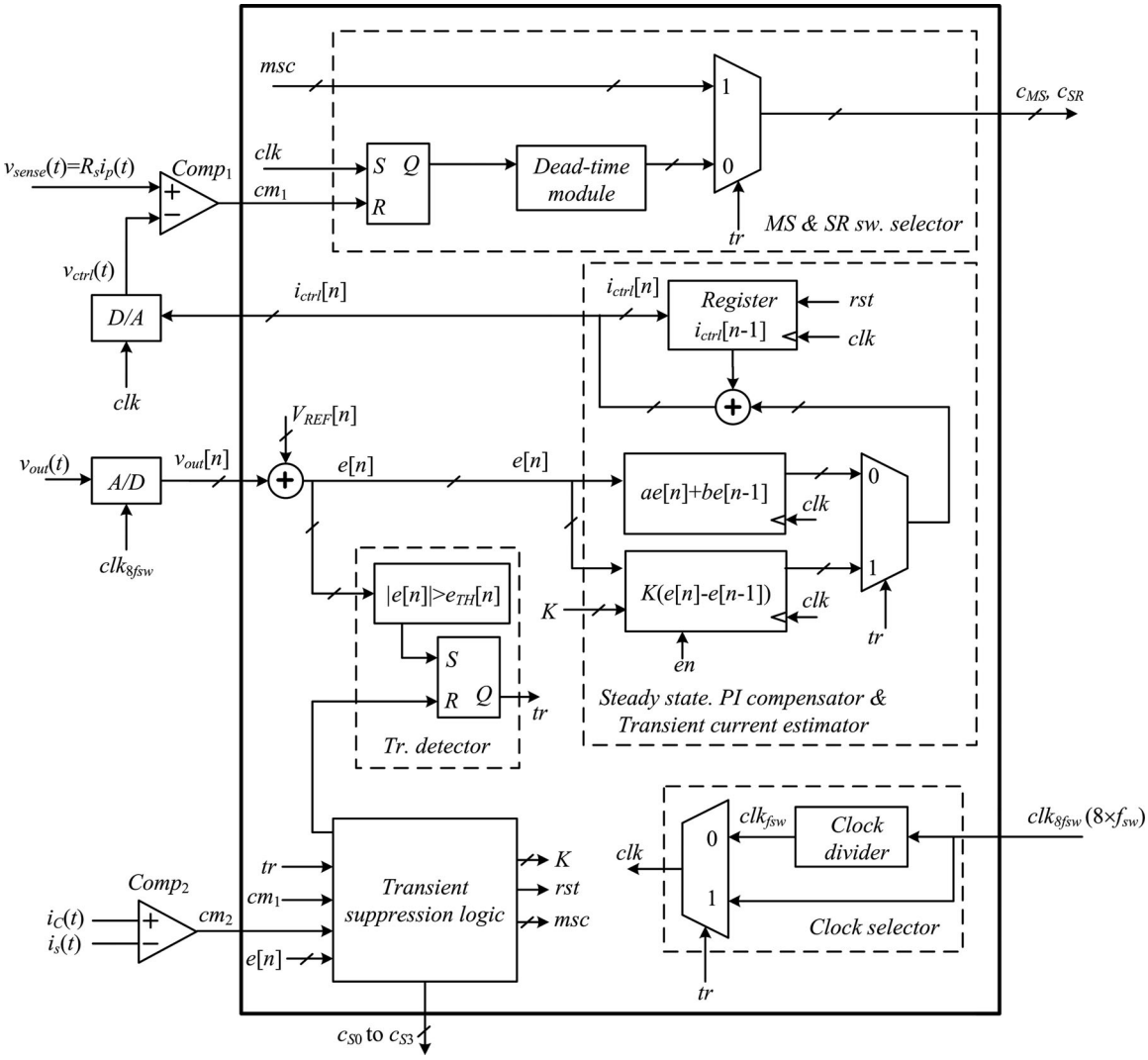

Fig. 6. Block diagram of the controller.

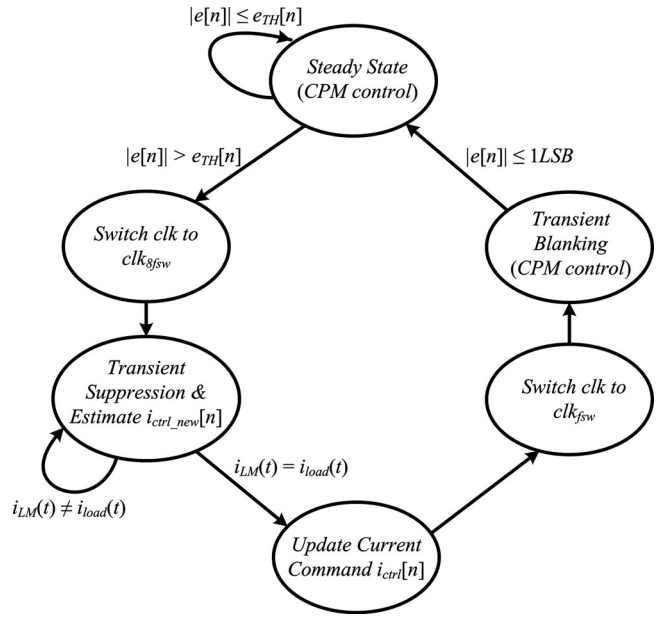

Fig. 7. State diagram of the digital controller.

In this mode, the output of the transient detector *tr* is low and the controller operates as a mixed-signal CPM system [46]–[48]. During this state, the clock selector produces *clk* pulses at $f_{\rm sw}$ and the PI compensator and transient current estimator block implements a conventional PI control algorithm [5]

$$i_{\rm ctrl}[n] = i_{\rm ctrl}[n-1] + ae[n] + be[n-1] \qquad (6)$$

to calculate $i_{\rm ctrl}[n]$. The calculated value is the input for the D/A converter, where a and b in (6) are the compensator coefficients calculated such that the stability of the system in steady state is ensured [5], $i_{\rm ctrl}[n-1]$ and $e[n-1]$ are the compensator's output and error values of one cycle before, respectively. In the next step, $i_{\rm ctrl}[n]$ is converted into a proportional voltage value $v_{\rm ctrl}(t)$ and compared with the signal $v_{\rm sense}(t) = R_s \times i_p(t)$, from the primary current-sensing circuit, to form an input for the MS and SR switch selector. This produces the control signals for switches MS and SR (see Fig. 1), labeled as $c_{\rm MS}$ and $c_{\rm SR}$, respectively.

A transient is detected when $e[n]$ exceeds the maximum allowable deviation, i.e., for $|e[n]| > e_{\rm TH}[n]$. At that point, the S-R latch of the transient detector is triggered and, consequently, the signal *tr* initiating a transient mode of operation is set. Now,

the transient suppression logic is activated. The clock selector produces *clk* signal at eight times $f_{\rm sw}$. Also, in this mode, the PI compensator block changes its structure and becomes an estimator of the primary current. As described later, this estimation is used to provide a seamless return to the steady state [11].

The transient suppression logic produces control signals for auxiliary switches S_0–S_3 (see Fig. 1), labeled as c_{S0}–c_{S3}, and indirectly controls the operation of the main switches, MS and SR, through a 2-bit main switch control signal, *msc*. As described in the following sections, the operation of transient suppression logic depends on the type of transient and, in addition to controlling all switches in the FTBB converter, this logic also ensures seamless mode transitions. After the transient is suppressed, the transient detector and the controller returns to the steady-state mode of operation.

A. Heavy-to-Light Transient Operation

The operation of the transient suppression logic during a heavy-to-light transient is fairly simple. It is mainly governed by the pulses of the comparators *Comp*$_1$ and *Comp*$_2$ and can be described by looking at Figs. 2 and 3. Upon a load transient, the register keeping value $i_{\rm ctrl}[n]$ is reset and a two-phase recovery sequence is performed, as described in Section II-B. The end of the leakage current energy release period, i.e., zero-current crossing, is detected by *Comp*$_1$ and this process is followed by the magnetizing inductor current-steering period (t_2 to t_3 in Fig. 2). The primary winding of the flyback transformer is now an open circuit and the load current is fully supplied by the output capacitor $C_{\rm out}$; thus, $i_{\rm load}(t) = -i_C(t)$. This period ends when the magnetizing current reaches the new load value, i.e., $i_s(t) = -i_C(t)$, detected by *Comp*$_2$. At this time instance, the $i_{\rm ctrl}[n-1]$ register of the PI compensator (see Fig. 6) is updated with the new current estimate, the transient detector is reset, and the steady-state mode of operation resumed.

To further minimize transient voltage deviation, the transient detector in Fig. 6 can be replaced by an asynchronous threshold detector as reported in [12], such that the inherent detection delays are practically eliminated.

B. Light-to-Heavy Load Transient Operation

For light-to-heavy transients, depicted in Figs. 4 and 5, the A/D converter and the comparator *Comp*$_2$ produce the main control signals. As described in Section II-C, as soon as a positive transient is detected, a virtual short across the primary winding is created over a fixed $t_{\rm pulse}$ period to form the rising slope of the short current pulse in Fig. 4. After this period, switches S_2 and S_3 (see Fig. 1) are turned OFF, so the equivalent circuits in Fig. 5(b) and (c) can be formed. The switches remain in this state until the voltage drop, i.e., $e[n]$, exceeds the predefined threshold, and the new pulse is initiated. The end of the light-to-heavy transient recovery mode is sensed when the magnetizing current reaches the new load value. This is performed through the detection of the capacitor current zero crossing during the mode of operation shown in Fig. 5(c). Since in this mode the secondary current $i_s(t)$ is zero, *Comp*$_2$ can be used for zero-crossing detection.

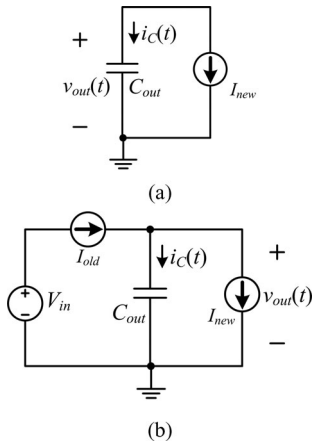

Fig. 8. Simplified equivalent circuits of the converter during the load current estimation period. (a) For a heavy-to-light load transient. (b) For a light-to-heavy load transient.

C. Seamless Transition to Steady State

To achieve smooth transitions to steady state from transient modes, the current command $i_{\rm ctrl}[n]$ of the PI compensator is updated such that the steady-state operation mode starts with an $i_{\rm ctrl}[n]$ value that matches the new load current value [11]. This value is obtained with a relatively simple estimation method, using the output voltage measurement and the transient current estimator in Fig. 6, which shares the same hardware with the PI compensator. To describe the method, Fig. 8 and the analysis shown here can be used. For simplicity, in this analysis, it is assumed that the output voltage deviation is significantly smaller than the dc output voltage value and, consequently, that the load can be represented as a current source.

The estimation of the new load current during a heavy-to-light load transient is performed during the time when the circuit in Fig. 3(d) is valid. Fig. 8(a) shows a simplified equivalent circuit during that period, where $I_{\rm new}$ is the new load value.

It can be seen that, during this phase, the load current is fully supplied by the output capacitor, and the output voltage deviation $\Delta v_{\rm out}$ over one sampling period $T_{\rm sample}$ can be represented as

$$\Delta v_{\rm out} = -\frac{T_{\rm sample}}{C_{\rm out}} I_{\rm new}. \tag{7}$$

Based on this equation, the new current command $i_{\rm ctrl\_new}[n]$ can be estimated as

$$i_{\rm ctrl\_new}[n] = K(e[n] - e[n-1]) \tag{8}$$

where $e[n] - e[n-1]$ is the difference between two successive voltage samples. It is proportional to the output voltage deviation. K is a constant that depends on the quantization bin of the A/D, the gain of the primary current-sensing circuit $T_{\rm sample}$, and $C_{\rm out}$. In a practical implementation, $e[n]$ and $e[n-1]$ are taken with a slight delay after a transient occurs, in order to

eliminate the influence of voltage ringing caused by the capacitor's equivalent series inductance.

To estimate the new current command after a light-to-heavy load transient, two $v_{\rm out}(t)$ samples are taken right after the transient is detected, and before the auxiliary switches are activated (during the t_0 to t_1 time interval in Fig. 4). During this brief period, the equivalent circuit of the converter can be modeled as shown in Fig. 8(b). Here, the inductor is replaced with a current source whose value is equal to the pretransient load current, labeled as $I_{\rm old}$.

Now, the output voltage deviation over one sampling period is

$$\Delta v_{\rm out} = -\frac{T_{\rm sample}}{C_{\rm out}}(I_{\rm new} - I_{\rm old}) \tag{9}$$

and the equivalent expression for the new current command value becomes

$$i_{\rm ctrl\_new}[n] = K(e[n] - e[n-1]) + i_{\rm ctrl\_old}[n] \tag{10}$$

where $i_{\rm ctrl\_old}[n]$ is the old steady-state current command. This was stored in the PI compensator prior the transient. Equations (7) and (9) indicate that the accuracy of the estimation and the value of factor K can be affected by variations in the output capacitance. To eliminate this problem, a self-calibration method can be employed [30], [49]–[51]. For example, the current estimator can be tuned according to its response to a small known current step, as described in the sensorless CPM-controlled system reported in [49].

To handle multiple nested light-to-heavy load transients, the A/D of this circuit can be modified as demonstrated in [11].

D. Prevention of Undesired Mode Transitions

Multimode controllers based on threshold voltage monitoring tend to suffer from undesired mode transitions when the output voltage gradually settles after a transient event [6]–[15]. This problem is avoided by introducing a blanking period after the transient suppression process is complete. As illustrated in Fig. 7, during this time, the converter is forced to operate with the steady-state CPM controller, until the output voltage settles to the nominal value and the error signal $e[n]$ is no larger than one quantization step of the A/D converter. Meanwhile, the difference between consecutive samples of the error signal, $e[n] - e[n-1]$, is monitored to determine whether a new load transient has occurred. If the controller detects a sudden change that results in $(e[n] - e[n-1]) > e_{\rm TH}[n]$, a new transient suppression process is activated.

IV. Energy Recycling and Losses of the Auxiliary Switches

The auxiliary switches S_0–S_3 (see Fig. 1) of the presented FTBB converter inevitably introduce extra conduction and switching losses and result in lower steady-state efficiency when compared to the conventional buck converter. However, these losses can be partially or fully compensated due to the ability to recycle energy in the FTBB converter. As demonstrated in the following section, for frequent load transients that are characteristic for PoL applications, the efficiency of the FTBB converter can be even better than that of the conventional buck converter. The range of operation where the FTBB converter has a higher efficiency than the conventional buck converter can be estimated using simulations and the following analysis.

As illustrated in Fig. 2, when the auxiliary switches S_1 and S_2 are turned ON and S_0 is turned OFF during a heavy-to-light transient recovery, magnetizing current $i_{\rm LM}(t)$ is steered back to the input source through the secondary winding of the transformer. As can be seen from the simulation results in Figs. 9 and 10, the current steering has two positive effects. First, a portion of energy stored in the inductance is always recycled. Second, reduced voltage overshoots also result in power savings. This is because during overshoots, excess power is unnecessarily delivered to the load.

The amount of energy savings obtained with the FTBB converter strongly depends on the load transient values and the control methods used. The simulation results in Figs. 9 and 10 show dynamic responses of the conventional buck and the FTBB converters for different load transients. Both converters are regulated with minimum-deviation control [16], have the same equivalent output filter inductances, and the same output capacitance values.

For heavy to a no-load transient (see Fig. 9), both the conventional buck and the FTBB converters recycle the entire energy stored in the inductor back to the source and no saving is achieved, even though the voltage overshoot of the FTBB converter is much smaller.

For heavy-to-light and heavy-to-medium load transients, the energy savings become noticeable. As shown in Fig. 10, a smaller amount or no energy is recycled by the buck converter, while the FTBB converter recycles a significant amount of energy. The amount of energy recycled through this mechanism can be calculated numerically from simulation or measurement results as

$$W_{\rm rec} = \int_0^{t_{is}} V_{\rm in} i_{\rm neg}(t) dt \tag{11}$$

where t_{is} is the inductor current settling time, $V_{\rm in}$ is the input voltage, and $i_{\rm neg}(t)$ is the negative portion of the input current.

In addition, for the buck converter, significantly larger than the nominal energy is delivered to the load due to the larger overshoot. This excess energy, i.e., overshoot energy, can be calculated as

$$W_{\rm os} = \int_0^{t_s} \left(\frac{v_{\rm out}(t)^2 - V_{\rm REF}^2}{R_{\rm new}} \right) dt \tag{12}$$

where t_s is the output voltage settling time, $V_{\rm REF}$ is the desired output value, and $R_{\rm new}$ is the new load value.

Based on the previous analysis, the energy savings of the FTBB converter obtained through current steering can be calculated as

$$W = (W_{\rm rec\_FTBB} - W_{\rm rec\_buck}) + (W_{\rm os\_buck} - W_{\rm os\_FTBB}) \tag{13}$$

where $W_{\rm rec\_FTBB}$ and $W_{\rm rec\_buck}$ are the energy recycled through the inductor current steering for the FTBB and buck converters, respectively. The terms $W_{\rm os\_FTBB}$ and $W_{\rm os\_buck}$

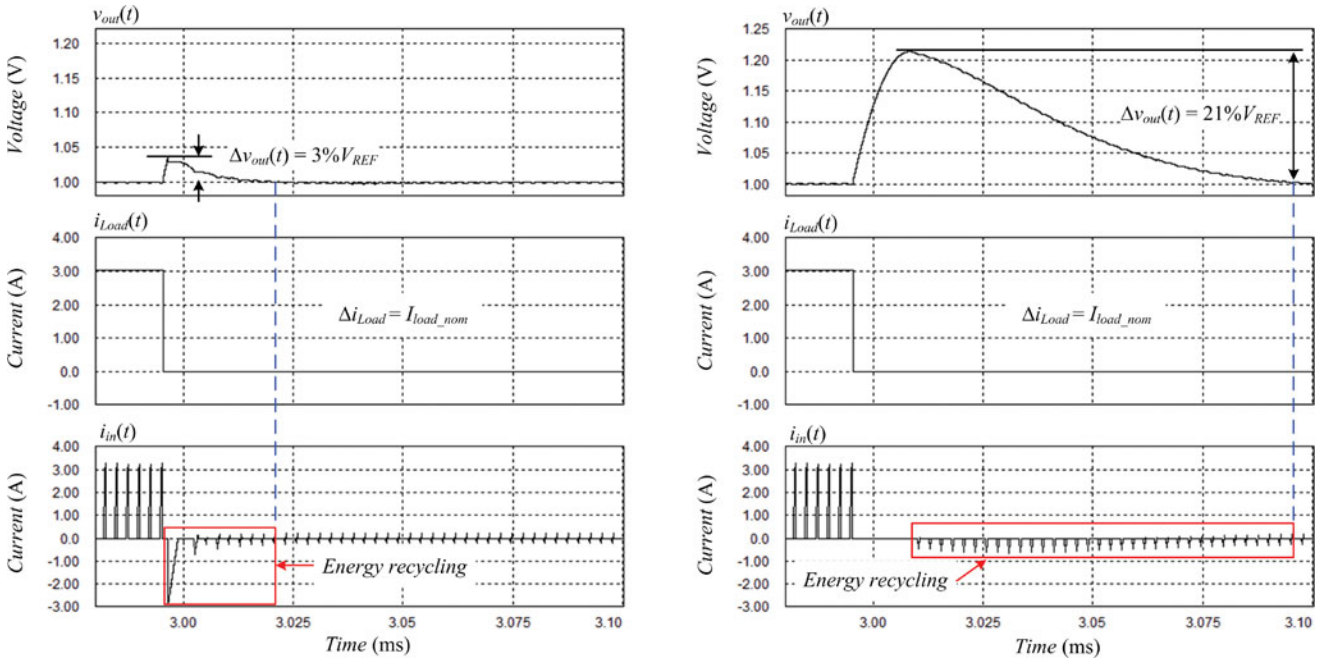

Fig. 9. Simulation results for a full-load to no-load transient for (left) the FTBB converter and (right) a buck converter. Top waveforms: output voltages $v_{\rm out}(t)$. Middle waveforms: load currents $i_{\rm load}(t)$. Bottom waveforms: input currents $i_{\rm in}(t)$ of the converters.

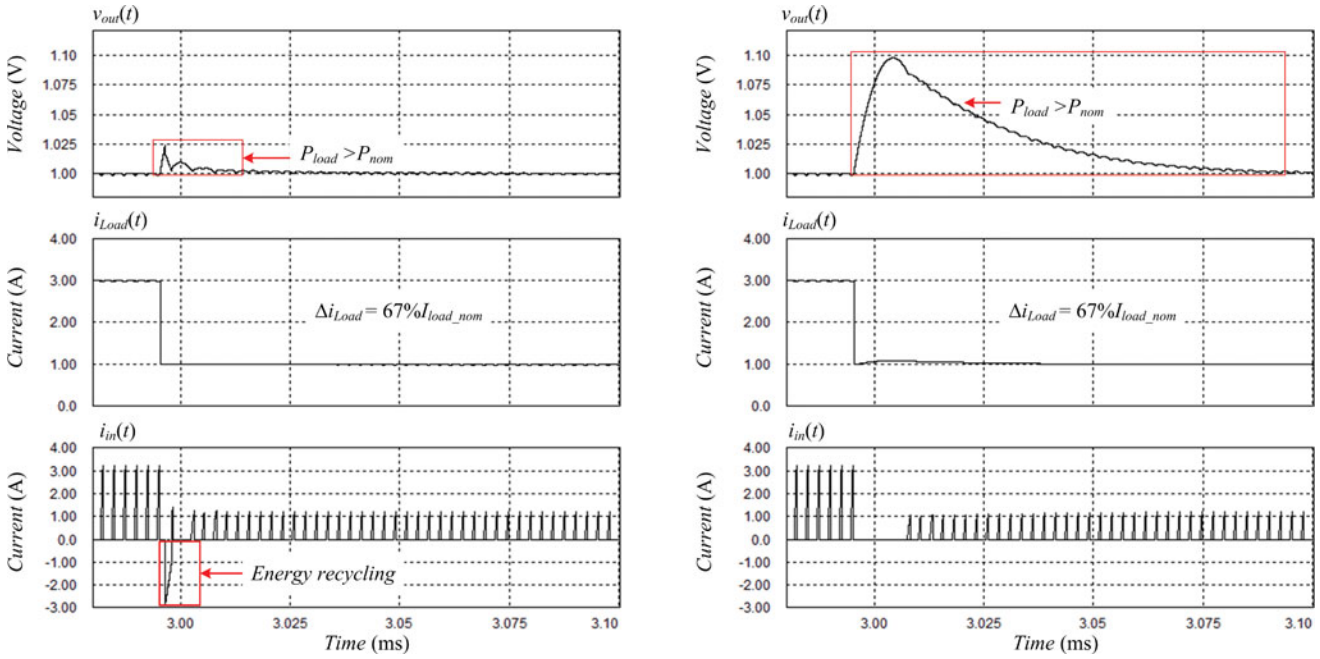

Fig. 10. Simulation results for a 100–33% load transient for (left) the FTBB converter and (right) a buck converter. Top waveforms: output voltages $v_{\rm out}(t)$. Middle waveforms: load currents $i_{\rm load}(t)$. Bottom waveforms: input currents $i_{\rm in}(t)$ of the converters.

represent extra energy consumed during the overshoot for both topologies.

It should be noted that, in order to find fairly accurate waveforms of $v_{\rm out}(t)$ and $i_{\rm neg}(t)$ during transients, the assistance of simulation tools or experimental testing might be needed. This is because both of these waveforms depend on the speed of controller, amplitude and slew rate of the load transient, operating conditions, and filter components. Most of these relations are highly nonlinear [18]. Furthermore, the waveforms are also affected by values of parasitic components and system delays that are often unknown.

On the other hand, the additional power loss caused by the auxiliary switches can be expressed as

$$P_{\rm Aux} = \sum_{n=0}^{3} R_{{\rm on}\_n} \times I_{{\rm rms}\_n}^2 + \sum_{n=0}^{3} P_{{\rm SW}\_n} \qquad (14)$$

where $\sum R_{\mathrm{on}\_n} \times I^2_{\mathrm{rms}\_n}$ represents the total conduction losses of switches S_0–S_3 and the term ΣP_{SW_n} accounts for all additional switching losses (including gate drive losses). In the first term, the conduction losses of S_0 are dominant, since this switch is inside the main current conduction path and is active most of the time. In the second term, the switching losses of S_2 and S_3 are dominant due to multiple switching actions during light-to-heavy load transients.

For frequent load changes, which are typical for PoL applications, the introduced FTBB converter is more efficient than the conventional buck converter if the following equation is satisfied:

$$W \cdot f_{\mathrm{load}} > P_{\mathrm{Aux}} \tag{15}$$

where f_{load} is the load changing frequency.

V. Experimental Verification

The functionality and performance of the FTBB converter are experimentally verified. The experiments are performed with a 6-to-1-V, 3-W, 390-kHz field-programmable gate array (FPGA)-based prototype that was designed based on the diagrams as shown in Figs. 1, 6, and 7. Also, for comparison, a conventional buck converter with identical components (excluding auxiliary circuit) was built and tested. The conventional buck converter is used as a reference in the study due to the fact that it is almost exclusively used in the targeted PoL applications [52], [53]. Operation of both converters in steady state is regulated with the identical CPM controllers and both converters utilize minimum-deviation control [16] during transients. In the experiments presented in the following sections, the transient detection error threshold $e_{\mathrm{TH}}[n]$ of both converters is set to 4 A/D quantization steps. In this case, due to unknown delays and parasitic components of the system, the threshold value is determined experimentally. Ideally, for a zero-delay FTBB converter with very small leakage inductance, the top threshold value could be the same as the maximum allowable voltage excitation during a heavy-to-light load transient.

Current sensing in both prototypes is performed by placing sensing resistors in the current paths of interest, where the sense resistors for $i_s(t)$ and $i_C(t)$ are well matched to provide accurate comparison. The voltages across the resistors are then amplified. To minimize the influence of current ringing due to the action of the switches, short blanking periods immediately following the switching actions are also introduced.

The design parameters of the prototypes are given in Table I. And the list of the key components is provided in Table II.

For a possible on-chip implementation, another challenge would be the requirement for a relatively large number of current-sensing circuits compared to the conventional buck. Since not all current-sensing circuits operate at the same time, a potential solution for minimizing their number could be task-based multiplexing. In this case, the sensing circuits for $i_p(t)$ and $i_s(t)$ would be replaced by sense FETs [54] in parallel with switches S_0 and S_2, respectively.

It should be noted that in the prototypes, the off-shelf buck inductor and the flyback transformer have almost identical magnetic cores [55], [56] and, consequently, very similar overall volumes. The flyback transformer has the magnetizing inductance of 4.3 μH and its leakage inductance is 0.4 μH. The conventional buck converter has a 4.7-μH filter inductor. Both power converters have a 200-μF output capacitor, with an ESR of 20 mΩ.

TABLE I
Summary of Design Parameters

Parameter	Value
V_{in}	6 V
V_{out}	1 V
i_{load}	max. 3 A
L_M+L_{LEAK} / L_{buck}	4.7 µH
C_{out}	200 µF
ESR	approx. 20 mΩ
Switching Frequency	390 kHz
Δi_{load}	±3 A

A. Transient Response

Figs. 11 and 12 compare the heavy-to-light load transient responses of the two topologies. Both converters are regulated by minimum-deviation controllers [16], resulting in the smallest possible output voltage deviation for a given power stage. The results show that the FTBB converter almost instantaneously reduces the primary current of the transformer, i.e., capacitor charging current, to zero. This drastically reduces the output voltage overshoot from 210 to 70 mV, allowing for a proportional reduction in the output capacitance value. In other words, to reduce the unacceptably high voltage overshoot in the buck converter to the level found in the FTBB converter, a capacitor of 600 μF would be needed in the buck converter prototype.

As described in Section II-B, the sudden reduction in the capacitor charging current is achieved by redirecting the magnetizing current back to the input voltage source, and in the same process, the energy stored in the inductor is recycled.

Figs. 13 and 14 demonstrate the responses of both converters for a 3 A light-to-heavy load transient verifying the fact that the FTBB converter produces a 25% smaller voltage deviation. It can be seen that, as described in Section II-C, the output voltage deviation is reduced by lowering the effective inductance of the primary side of the transformer to its leakage value and producing a set of current pulses that reverse the capacitor discharging process. It should be noted that for converters with relatively small step-down conversion ratios and/or higher output voltages, the improvement in transient response could be even larger.

TABLE II
KEY COMPONENT LIST OF THE EXPERIMENTAL PROTOTYPE

Name	Manufacturer, Part Number	Parameter
Power MOSFET	International Rectifier, IRF7821	On-resistance = 10 mΩ, total gate charge ≈ 9 nC
A/D	Analog Device Inc., AD9215	Effective quantization step = 8 mV
D/A	Analog Device Inc., AD9740	Effective quantization step = 2 mV
Comparators	Linear Technology, LT1719	4.5 ns propagation delay, 0.4 mV input offset
Flyback Transformer	Würth Elektronik, WE-DD 744873004	$L_M \approx 4.3$ μH, $L_{LEAK} \approx 0.4$ μH
C_{out}	Murata Manufacturing Co., GRM31CR60J	$R_{ESR} \approx 20$ mΩ, including the sense resistor for $i_C(t)$

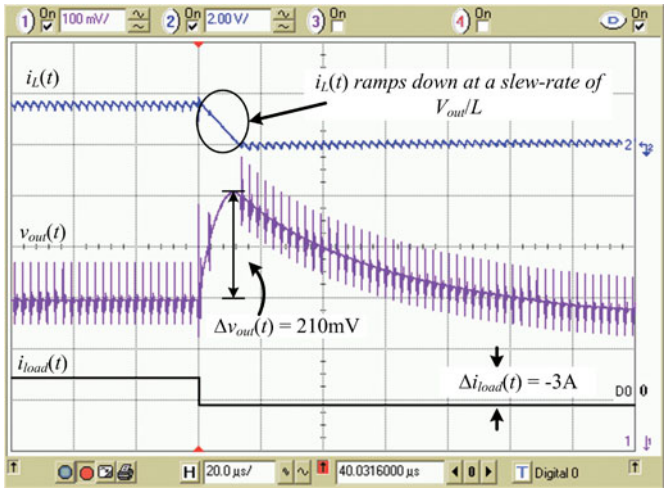

Fig. 11. Transient response of the conventional buck converter for a 3 A heavy-to-light load transient. (Top) Buck inductor current $i_L(t)$, scale 4 A/div. (Middle) AC component of the output voltage $v_{\rm out}(t)$, scale 100 mV/div. (Bottom) Load step command $i_{\rm load}(t)$. Time scale is 20 μs/div.

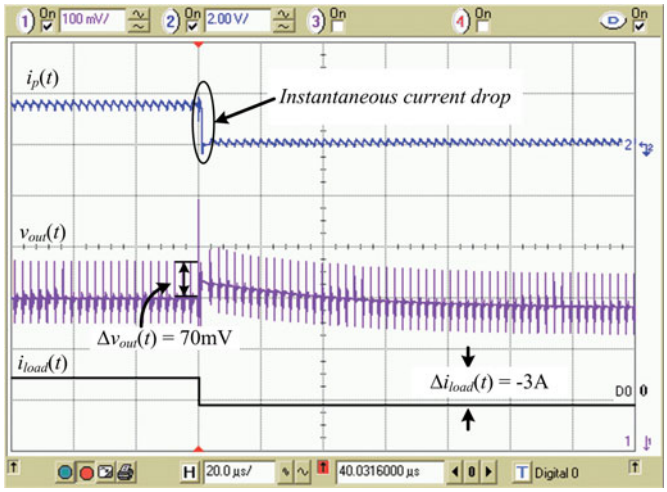

Fig. 12. Transient response of the FTBB converter for a 3 A heavy-to-light load transient. (Top) Primary current $i_p(t)$, scale 4 A/div. (Middle) AC component of the output voltage $v_{\rm out}(t)$, scale 100 mV/div. (Bottom) Load step command $i_{\rm load}(t)$. Time scale is 20 μs/div.

B. Efficiency Comparison

As discussed in Section IV, the proposed topology introduces extra conduction losses that can be compensated through the energy recycling capability. To verify these tradeoffs, the efficiency and power losses of the conventional buck and the FTBB converters are measured and compared both in steady state and for frequent load transients.

Fig. 15 shows an efficiency comparison over a 10–100% of the output load range, for both converters operating in steady state. It can be seen that the FTBB converter has lower power conversion efficiency, more noticeable at heavy loads, caused by the extra switch S_0 (see Fig. 1) in the main conduction path.

Figs. 16 and 17 confirm that, for frequently changing loads, the effect of additional conduction losses can be compensated by the energy recycling mechanism. The average input and output powers of both converters $P_{\rm in\_avg}$ and $P_{\rm out\_avg}$ for the case when the load current changes between 0.5 and 2.5 A with 50% duty cycle are measured. These measurements are obtained for each load changing frequency ranging from 100 Hz to 12.4 kHz over a 100-ms period. The power losses are estimated by comparing $P_{\rm in\_avg}$ and $P_{\rm out\_avg}$. The effective efficiency of both converters is calculated from

$$\text{Efficiency} = 100\% \times \frac{P_{\rm out\_avg}}{P_{\rm in\_avg}}. \tag{16}$$

The results show that for load changing frequency higher than 4 kHz, the losses of the FTBB converter are smaller than that of the conventional buck converter, fully compensating for the losses of the extra auxiliary elements. For a load changing frequency of 12.3 kHz, the FTBB converter achieves 7% reduction in power loss, thus 1.5% improvement in effective efficiency, compare to the buck converter prototype. For on-chip integrated PoL converters operating at much higher switching frequencies and undergoing more frequent load changes, it can be expected that this recycling mechanism can provide even greater energy savings.

The main factors that limit the switching frequency of the experimental prototype are the delays of discrete components. These include the delays of the current-sensing circuits, A/D converter, and the FPGA system. Possible on-chip implementation of this system would allow operation at much higher

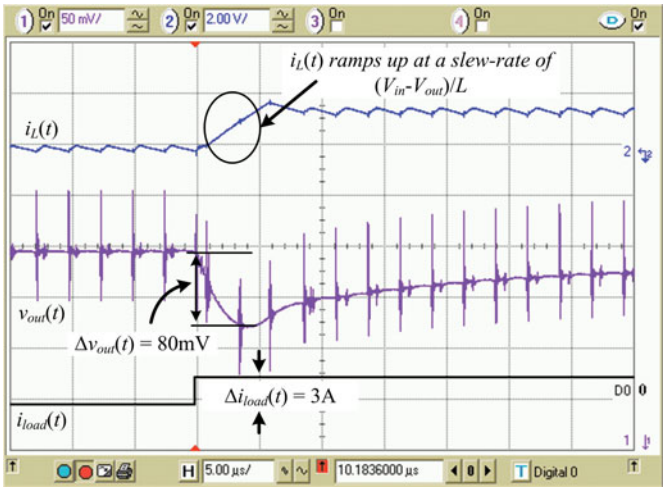

Fig. 13. Transient response of the conventional buck converter for a 3 A light-to-heavy load transient. (Top) Buck inductor current $i_L(t)$, scale 4 A/div. (Middle) AC component of the output voltage $v_{\rm out}(t)$, scale 50 mV/div. (Bottom) Load step command $i_{\rm load}(t)$. Time scale is 5 μs/div.

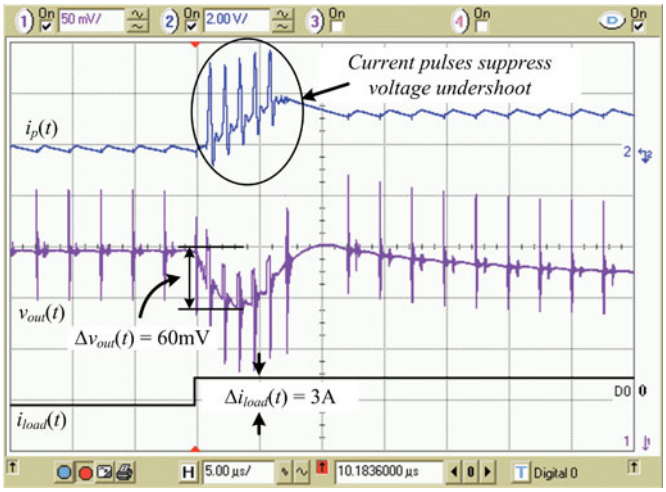

Fig. 14. Transient response of the FTBB converter for a 3 A light-to-heavy load transient. (Top) Primary current $i_p(t)$, scale 4 A/div. (Middle) AC component of the output voltage $v_{\rm out}(t)$, scale 50 mV/div. (Bottom) Load step command $i_{\rm load}(t)$. Time scale is 5 μs/div.

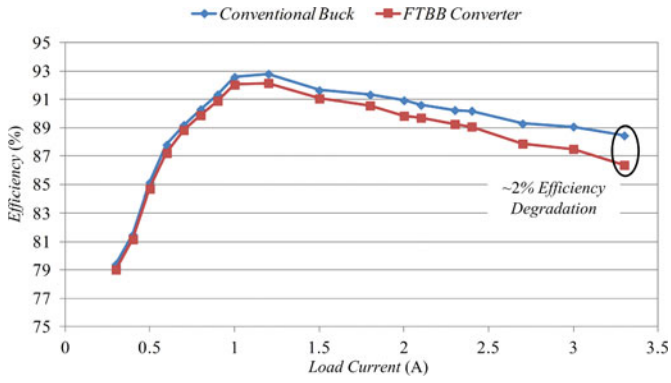

Fig. 15. Comparison of steady-state efficiency of the conventional buck and the FTBB converters.

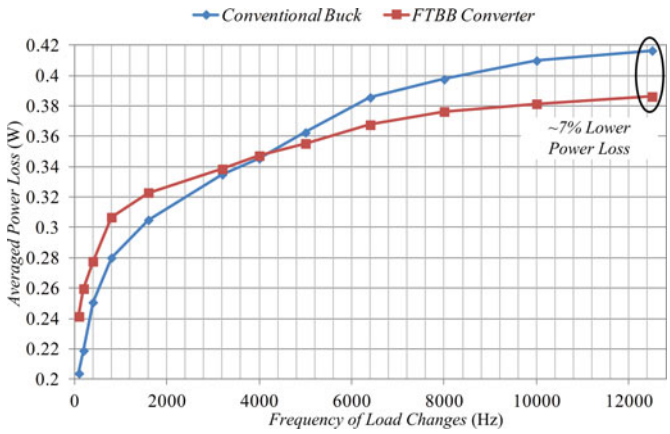

Fig. 16. Comparison of averaged power loss of the conventional buck and the FTBB converters under frequently changing load conditions.

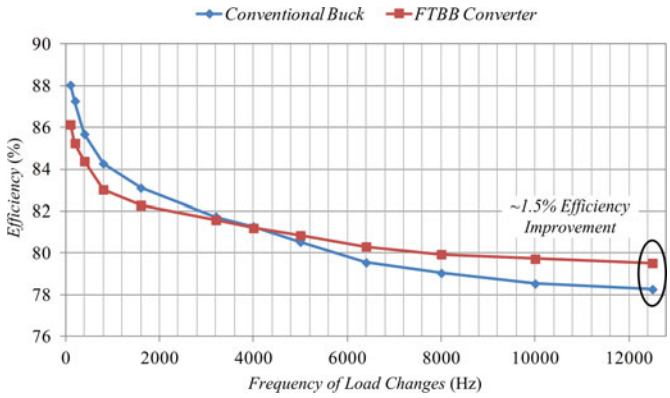

Fig. 17. Comparison of effective efficiency of the conventional buck and the FTBB converters under frequently changing load conditions.

switching frequency and minimize delay effects. It could be based on the architectural solutions presented in [57] demonstrating an on-chip integrated 10-MHz buck converter regulated by a mixed-signal CPM controller.

VI. Conclusion

This paper presented an FTBB converter and a complementary controller that can overcome the current slew-rate limitations of the conventional buck converter. In the FTBB converter, the conventional inductor is replaced with a flyback transformer, with approximately the same magnetic core size and a set of auxiliary switches. During heavy-to-light load transients, the magnetizing current is steered back to the input voltage source. In this way, the overcharging of the output capacitor is eliminated and the voltage overshoot is drastically reduced. At the same time, the energy stored in the magnetic component is recycled. Both of these improvements significantly reduce energy losses associated with the transient operation. The transient switching sequence is performed such that the maximum blocking voltage of all switching components in the circuit is no larger than the input voltage. The combination of limited blocking voltage and energy recycling ability makes the FTBB converter well suited for PoL applications. With a frequently changing load, the losses

caused by the additional switches can be partially or fully compensated. During light-to-heavy load transients, the equivalent inductance, seen at the transformer primary winding, is reduced to its leakage inductance value, allowing a significant increase in the current slew rate. The operation of the FTBB converter is governed by a modified mixed-signal CPM controller that provides minimum voltage deviation and seamless transitions between the modes. The smooth transition between steady state and transient modes is achieved through a simple transient current estimation, based on the analysis of the difference between the output voltage error samples. The effectiveness of the FTBB concept is verified through a comparison with an equivalent buck converter. The comparisons confirm that the FTBB converter results in a drastic improvement of transient performance and, for frequently changing loads, improved power conversion efficiency.

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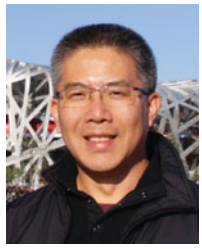

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