Minimum-Deviation Digital Controller IC for DC–DC Switch-Mode Power Supplies

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***Abstract*—This paper introduces a hardware-efficient digital controller integrated circuit (IC) for single- and two-phase dc–dc converters that recovers from load transients with virtually minimum possible output voltage deviation. In steady state, the IC behaves as a conventional voltage-mode pulsewidth modulation controller. During load changes, it enters transient suppression mode that utilizes a simple algorithm, requiring no knowledge of the converter parameters and virtually no processing power, to seamlessly recover back to the steady state without exposing components to a high-current stress. To further minimize the area and power consumption of the IC, an asynchronous track-and-hold analog-to-digital converter (ADC) is developed. The ADC utilizes only one preamplifier and four comparators having approximately ten times smaller silicon area and power consumption than a comparable windowed flash ADC. To compensate effects of converter losses and system delays on the controller operation, the IC also incorporates duty ratio correction logic and dual-extreme point-based detection. The entire IC is implemented in a CMOS 0.18-μm process on a 0.26-mm^2 silicon area, which is comparable to the state–of-the-art analog solutions. The functionality of the controller is tested with both single- and two-phase commercial 12–1.8 V, 500-kHz 60/120-W buck converter power stages. The results demonstrate seamless transition to the steady state with virtually minimum output voltage deviation. For the experimental system, this deviation is about four times smaller than that of a fast PID compensator having a one-tenth of the switching frequency bandwidth.**

***Index Terms*—Digital controller IC, fast response, low-power dc–dc converters, parameter insensitive.**

I. Introduction

HIGH-FREQUENCY low-power switch-mode power supplies (SMPS), used in consumer electronics, portable applications, and computers, are required to meet stringent voltage regulation requirements [1]–[3] using a cost-effective small-volume implementation. The regulation is usually achieved with an application-specific on-chip integrated controller (controller IC) occupying small silicon area [4]–[6]. The controller is often required to effectively minimize voltage deviations caused by load transients and, in that way, minimize requirements for the bulky output filter capacitor [7].

Conventional controller ICs [4]–[6] most frequently utilize constant-frequency voltage or current-programmed mode control [8], [9], where a linear PID compensator provides accurate output voltage regulation and system robustness over a wide range of operating conditions. To obtain fast response and, consequently, small output voltage deviations, a high-bandwidth control loop is usually designed. However, since the validity of the averaged converter models used in compensator designs is constrained to frequencies significantly lower than the switching frequency [7], the bandwidth of the feedback loop is quite limited.

Hysteretic-control-based analog IC solutions, which belong to the ripple-based class of controllers [10], have very simple structure and, generally, provide faster transient response. However, those systems usually operate at a variable switching frequency, which is not desirable in the targeted noise sensitive applications. Also, in these systems, as well as in other ripple-based solutions, great care is required to mitigate stability problems [10], such as jitter, high noise sensitivity, and fast-scale instability. Constant-frequency ripple-based systems [10], [11] eliminate the variable frequency and stability problems. The improvements are usually achieved by the introduction of an additional feedback loop that often slows down the transient response. Also, during transients, in the hysteretic systems, the switching components and the inductor are often exposed to currents significantly larger than nominal [23]. As a consequence, an overdesign of the power stage is usually required.

While the ripple-based solutions provide very fast transient response, they are still not able to recover the output voltage with the minimum possible deviation. Recently emerged digital controller ICs for high-frequency dc–dc converters [12], [13] have created possibilities of further improving transient response through advanced control laws. Among the most noticeable examples are time-optimal [13]–[22] and digital hysteretic [12], [23]–[28] controllers. For a given power stage, these solutions achieve virtually the fastest possible recovery time and, consequently, the smallest deviation. These advantages are most often demonstrated with large-scale prototypes consisting of discrete components and general-purpose digital logic. However,

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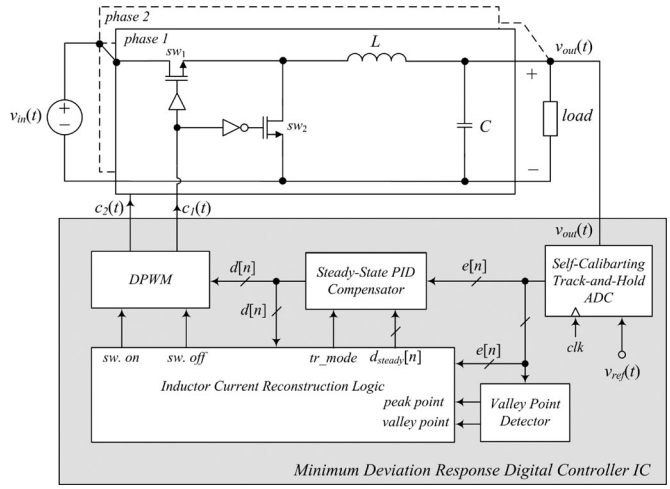

Fig. 1. Minimum-deviation controller IC regulating operation of a two-phase buck converter.

on-chip implementation of these controllers has not been widely adopted. This is mainly due to the challenges related to the complexity of the hardware needed for their implementation. The controllers require fairly demanding computational algorithms, to calculate the optimum switching sequence, and use complex analog-to-digital converters (ADCs) consuming relatively large power and silicon area. Furthermore, their operation is significantly affected by the imperfections of the converter circuit, i.e., converter losses and parasitic resistances, as well as by the system delays. All of these make the implementation of the on-chip minimum-deviation controllers challenging and overly expensive for the targeted cost-sensitive applications. As demonstrated in [12] and [13], an application-specific ADC for digital hysteretic and time-optimal controller occupies larger silicon area than an entire conventional controller IC [29]–[34].

The main goal of this paper is to introduce a simple minimum-deviation digital controller IC for single- and two-phase dc–dc converters that does not suffer from the previously mentioned drawbacks and can be implemented with simple hardware. Similar to solutions presented in [14]–[17], [19], and [22], the controller IC of Fig. 1 has two distinctive modes of operation. In steady state, the controller IC operates as a conventional constant-frequency pulsewidth-modulated voltage-mode controller. It uses a PID compensator to provide robust operation over a wide range of operating conditions. During transients, the controller provides recovery from load step changes with virtually minimum possible output deviation.

The entire controller is implemented on a silicon area that is comparable to conventional state-of-the-art single-phase controller ICs [29]–[34]. The cost-effective IC implementation is obtained by combining new minimum-deviation transient-mode control with a novel track-and-hold architecture of the ADC. The minimum-deviation controller utilizes a very simple algorithm that does not require any knowledge of the converter output filter parameters and virtually requires no processing power. It makes use of readily available data from the PID compensator and can be practically implemented through a single binary shifting operation, with no additional calculations. The asynchronous sampling track-and-hold ADC utilizes only four comparators and a low-gain preamplifier to accurately acquire information about the output voltage. The ADC also has a self-calibrating feature that automatically clears any accumulated error during its operation.

Furthermore, the new IC includes two elements for minimizing effects of the converter losses and system delays, allowing this chip to be used with realistic converters. Namely, the IC has a dynamic duty ratio correction block, which compensates for effects of duty ratio variations due to converter losses, and it also incorporates a dual valley/point detection mechanism for reducing the effects of system delays. The controller IC is designed for the targeted applications where the frequent load changes occur and the input voltage variations are relatively slow. Examples include point-of-load supplies and battery-powered systems.

This paper is organized as follows. In the next section, principles of the controller operation are described. Section III describes the ADC architecture. In Section IV, practical implementation problems related to the mode transitions and fast detection of the transients are addressed. Solutions for the aforementioned problems are also presented. In particular, the operation of the duty ratio correction logic and dual-extreme point detection method is described. That section also addresses effects of multiple transients and capacitor equivalent series resistance (ESR) on the controller operation and gives solutions for their minimization. Details of the on-chip implementation and experimental results verifying performance of the new controller IC are given in Section V.

II. Minimum-Deviation Controller Principle of Operation

The controller IC of Fig. 1 has two modes of operation, named steady state and transient suppression modes. In steady state [45], for output voltage variations smaller than a predefined threshold value $v_{\rm th}$, the IC operates as a conventional voltage-mode digital pulsewidth modulation regulator. The *self-calibrating track-and-hold ADC* compares the output voltage with a reference $V_{\rm ref}$ and produces a digital equivalent of the error signal $e[n]$. This value is then passed to the *steady-state PID compensator,* i.e., conventional compensator, which calculates an input value for the *digital pulsewidth modulator* (*DPWM*), labeled as $d[n]$. After a load transient is detected, the controller enters *suppression mode*. In this mode, the *inductor current reconstruction logic* reverses effects of the transient and seamlessly puts the system back into the steady-state mode of operation by only using information about the transient time instant and the steady-state duty ratio value before the transient.

A. Minimum-Deviation Controller

The principle of operation of the minimum-deviation controller is explained with the help of diagrams shown in Fig. 2, through a comparison with the operation of well-known time-optimal systems [13]–[22]. For simplicity, an ideal, i.e., lossless low-ESR single-phase power stage is initially considered. Later

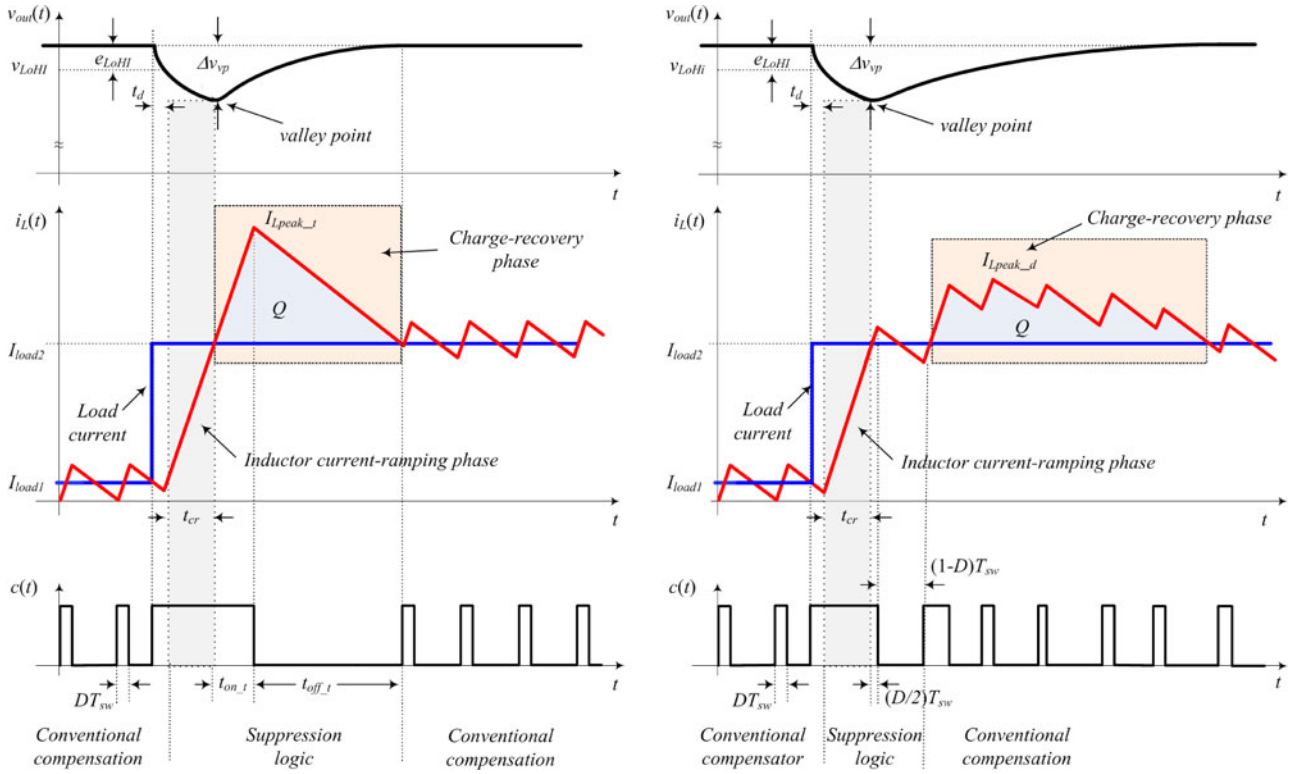

Fig. 2. Typical light-to-heavy transient waveforms of the time-optimal (left) and minimum-deviation (right) controllers.

on, implementations for a two-phase power stage and a realistic lossy converter will be described. The diagrams are also used to address the challenges of practical IC implementation of the conventional time-optimal systems.

Operation of a time-optimal controller for a light-to-heavy load transient (from a load value I_{load1} to I_{load2}) is shown in Fig. 2(a). In these systems, the control is commonly performed with two different functional blocks [13]–[22]. Before the transient, i.e., in steady state, the output is regulated with a conventional compensator [35] (a PID is usually used). After a voltage drop larger than the threshold value v_{thresh1} is detected, transient suppression logic is activated. To eliminate the delay between the load transient instant and activation of the controller (labeled as t_d in Fig. 2), in solutions proposed in [16]–[18], [21], and [25], the transient logic is activated after a large current in the output capacitor is detected. Such solutions require either a fast current sensor or, as discussed in Section IV-D, require a well-matched *RC* estimation circuit.

The time-optimal logic usually performs output voltage recovery through a two-phase process. In the first phase, i.e., the inductor current ramping phase, it brings the inductor current to the new load value, by keeping the main switch (SW_1 of Fig. 1) in on-state. During the second phase, the suppression logic recovers the lost capacitor charge Q through a single ON–OFF switching action. This, ideally, results in a seamless transition into the new steady state, where the conventional compensation mode is reactivated. In Fig. 2(a), the OFF and ON times, calculated during charge recovery phase, are labeled as $t_{\mathrm{on\_}t}$ and $t_{\mathrm{off\_}t}$, respectively. These times are usually computed based on the value and/or location of the maximum voltage deviation at the peak or valley point [13]–[22], Δv_{peak}, and on measurement (or estimation) of the capacitor current during transients [16]–[18], [21], [25].

The main challenge in implementing the time-optimal algorithms is related to charge recovery phase. It requires a fairly accurate calculation of the $t_{\mathrm{on\_}d}$ and $t_{\mathrm{off\_}d}$ times and timely generation of the switching sequence, to avoid severe mode transition stability problems. As addressed in [17] and [19], and shown in the sensitivity analysis of the following sections, even small inaccuracies in the timing sequence cause a large mismatch between the new load and the inductor current values at the end of the recovery phase and undesirable mode toggling.

In the practical sense, the need for an accurate optimal sequence generation transfers into requirements for a fast high-resolution processing unit and, as described in the following section, a very fast and accurate ADC for the output voltage measurement. The time-optimal algorithms often require a processing unit or a large look-up table (LUT), to perform divisions or calculations of square root values [13]–[22], which are fairly demanding tasks [17]. All of these make on-chip implementation of the proposed solutions challenging in the targeted cost-sensitive applications.

To achieve minimum possible deviation, in the controller of Fig. 1, the tasks between the transient suppression logic and the conventional compensator are divided differently compared to the time-optimal solutions. The transient suppression logic, here named *inductor current recovery logic*, only brings the current to its new steady state and the charge recovery task is passed to a conventional PID compensator. As it will be shown throughout this paper, for realistic systems, this rearrangement drastically

decreases computational requirements, as well as complexity of the ADC, allowing cost-effective implementation, at the price of a slight increase of the full-voltage recovery time. By looking at Fig. 2, it can be noticed that this increase in the recovery time can actually be beneficial in some cases, since it reduces the peak inductor current value exposing components to a lower stress.

It should be noted that the problem of large current stress in the time-optimal solutions was addressed in [36] and a theoretical solution for current limiting, based on the state-trajectory control, was proposed. In [22], the authors performed detailed analysis of the current overshoot problem and stressed its significance in high step-down ratio converters. Also, a multipulse solution for limiting the current that does not require knowledge of *LC* parameters was proposed. However, such a solution assumes that accurate information about instantaneous capacitor current during transients is available and requires a very fast and accurate measurement of the output voltage value during transients. Both of these requirements make the implementation of the previously proposed solution challenging in the targeted applications. As it will be described in the following sections, the minimum-deviation controller introduced here does not require current sensing and does not use the output voltage deviation value in determining the transient switching sequence.

B. Transient Operation—Inductor Current Reconstruction

During transients, the minimum-deviation controller performs very simple actions to create an inductor current wave shape corresponding to that of the new steady state. In this case, an accurate reconstruction of the entire current waveform, i.e., both the dc and ripple components, is very important. This is because, in modern converters, the ripple component can be as large as 40% of the maximum load current value [37], [38], and consequently, any ripple mismatch can have the same effect as a large load transient.

The operation of the controller during a sudden light-to-heavy load change can be explained by looking at the waveforms of Fig. 3. As soon as the output voltage drop exceeds the threshold value, i.e., a transient is detected, the controller turns ON the converter main switch (SW_1 of Fig. 1) causing the inductor current to ramp up. This process continues until the output voltage valley point is detected, by the track-and-hold ADC of Fig. 1. At this point, the initial on-time of the transistor control signal, $c(t)$, is extended by the time interval

$$t_{\rm on} = \frac{D \cdot T_{\rm sw}}{2} \tag{1}$$

followed by a turn-off period

$$t_{\rm off} = (1 - D) \cdot T_{\rm sw} \tag{2}$$

where D is the steady-state duty ratio value and $T_{\rm sw}$ is the switching period. Fig. 3 demonstrates that this switching sequence results in a current waveform practically identical to that of the new steady state. As soon as this current reconstruction period is completed, the PID compensator is reactivated, to perform charge recovery bringing the output voltage to the reference value.

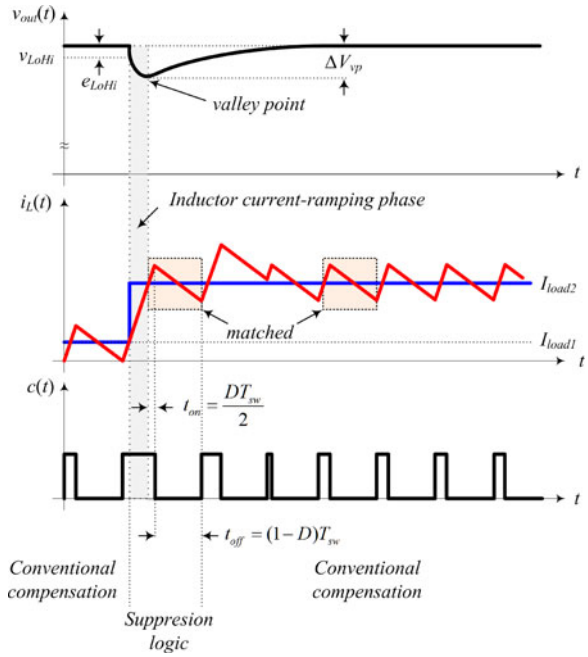

Fig. 3. Operation of the large–small signal digital controller during the light-to-heavy load transient with a single-phase buck converter.

It should be noted that the new operating conditions are well suited to the PID compensators, since the converter operates close to the steady state, where the small-signal assumption [7] is valid.

Equations (1) and (2) show that the transient suppression can be performed with very simple hardware, practically requiring no additional calculations or any knowledge of the converter *LC* parameters. For an ideal, lossless system, the digital equivalent of the duty ratio value D can be obtained by capturing the PID compensator output $d[n]$ prior to the transient. Subsequently, the division by two can be accomplished with virtually no processing power, through a right shift of the captured digital value.

It should also be noted that, unlike time-optimal and digital hysteretic solutions, the transient logic of the minimum-deviation controller requires no knowledge of the output voltage value and, thus, has reduced ADC requirements as well.

Operation of the minimum-deviation controller during a heavy-to-light load transient is shown in Fig. 4. It is based on the same principle of the inductor current reconstruction and is more straightforward than for the opposite transient. As soon as a transient is detected, i.e., the output voltage exceeds a predefined threshold voltage $v_{\rm HiLo}$, the controller turns ON SW_2 and turns OFF SW_1 (see Fig. 1) causing the inductor current to slope down.

After the inductor current reaches the new load value, i.e., the peak voltage is detected, the transistor off-time is extended by the time

$$t_{\rm off} = \frac{(1 - D)}{2} \cdot T_{\rm sw} \tag{3}$$

and, at the end of this interval, the PID compensator is immediately reactivated. As demonstrated in Fig. 4, in this case, a

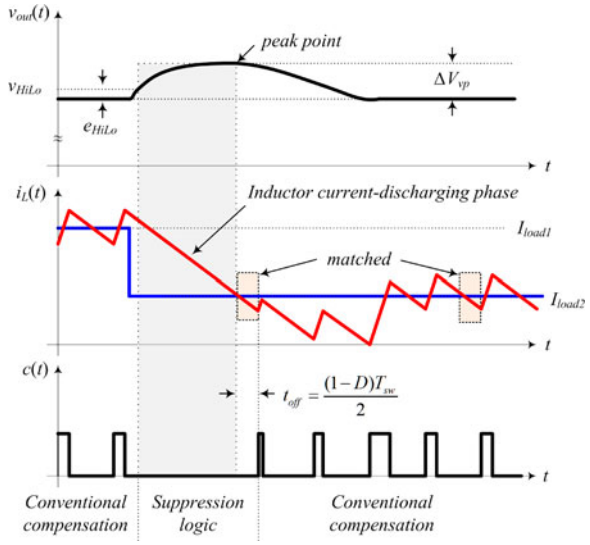

Fig. 4. Operation of the minimum-deviation digital controller during a heavy-to-light load transient with a single-phase buck converter.

simple extension of the off-interval is sufficient to reconstruct the new steady-state current waveform.

C. Extension to a Two-Phase Interleaved Buck Operation

The minimum-deviation controller IC is also designed to regulate the operation of two-phase interleaved buck converters with identical phases, allowing the power stage rating to be doubled. In the two-phase mode of operation, the same suppression logic is used, and the current reconstruction algorithm is slightly modified. In steady state, the same PID compensator regulates both phases through pulsewidth-modulated control signals $c_1(t)$ and $c_2(t)$ (see Fig. 1). The current sharing is implemented passively, by issuing the same $d[n]$ value to both phases, to ensure the highest power-processing efficiency [39]

The dual-phase operation of the controller during a transient is illustrated in Fig. 5. In this case, the sum of two phase currents is shaped by the transient suppression logic. The logic creates a sum whose dc and ripple values are identical to the sum of the two phase currents in the new steady state, as shown in Fig. 5.

After the transient is detected, the main switches of both phases are turned ON and kept in this state until the sum of the two phase currents becomes equal to the new load value. At this point, to reconstruct the sum, the on-time of the leading phase is extended by $t_{\rm on}$, defined by (1) and the lagging current is phase shifted, by applying $t_{\rm off}$ time equal to (2). As shown in Fig. 5, such a simple action results in the desired wave shapes.

D. Sensitivity Analysis

This section explains why the minimum-deviation controller is less sensitive to system nonidealities than the time-optimal counterpart. As discussed previously, the time-optimal controllers require either knowledge of *LC* parameters [16], [17], [21], [22] and input voltage value [15], [16], [20] and/or an extremely fast load transient detection circuit [13]–[22]. Fairly complex multiple calculations steps are also contributing to sensitivity, where each step is a source of potential error in the switching sequence timing.

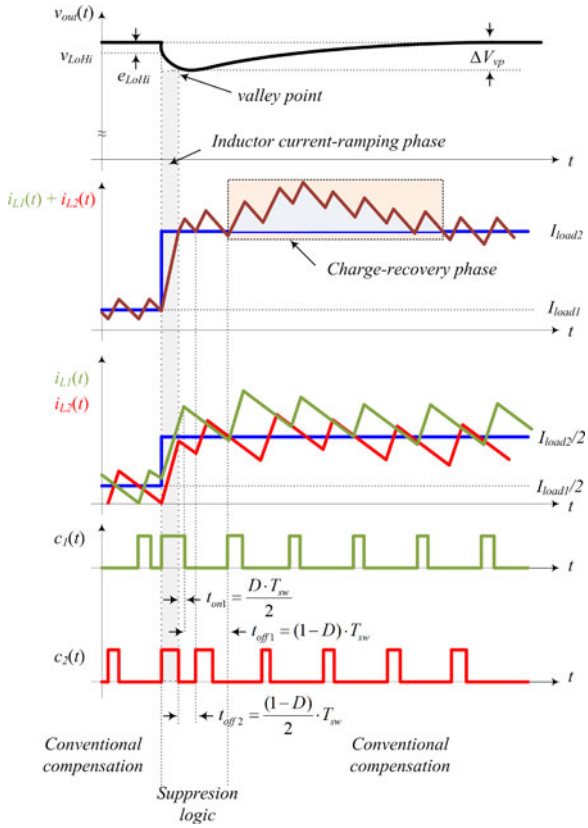

Fig. 5. Operation of the minimum-deviation controller during the heavy-to-light load transient with a dual-phase buck converter.

The following analysis shows how these timing errors affect the output voltage, potentially, causing undesirable mode transitions and stability problems. The worst case analysis can be performed using the diagrams of Fig. 6, showing a light-to-heavy load transient response in the presence of a delay, for a time-optimal and the minimum-deviation controllers. To simplify the analysis, all timing errors are lumped into a single parameter $t_{\rm delay}$, shown in the diagrams. It is also assumed that the total delay in both systems is the same.

The output voltage mismatch due to a delay can be calculated based on extra capacitor charge, from diagrams in Fig. 6. It can be seen that, for the time-optimal system, the delay results in extra charge ΔQ_1 and, consequently, a voltage mismatch

$$\Delta V_1 = \frac{\Delta Q_1}{C} = \frac{V_{\rm in} - V_{\rm out}}{LC} t_{\rm delay} \left(\frac{t_{\rm delay}}{2D} + \frac{t_{\rm on1}}{D} \right) \quad (4)$$

where $V_{\rm in}$ is the input voltage of the buck converter, $V_{\rm out}$ is its output voltage, and $t_{\rm on}$ is the main switch on-time during charge recovery phase [see Fig. 2(a)].

For the minimum-deviation case, the delay results in extra charge ΔQ_2 and the output voltage change of

$$\Delta V_2 = \frac{\Delta Q_2}{C} = \frac{V_{\rm in} - V_{\rm out}}{LC} t_{\rm delay} \left(\frac{t_{\rm delay}}{2D} + \frac{t_{\rm on2}}{D} \right) \quad (5)$$

where $t_{\rm on2} = DT_{\rm sw}/2$.

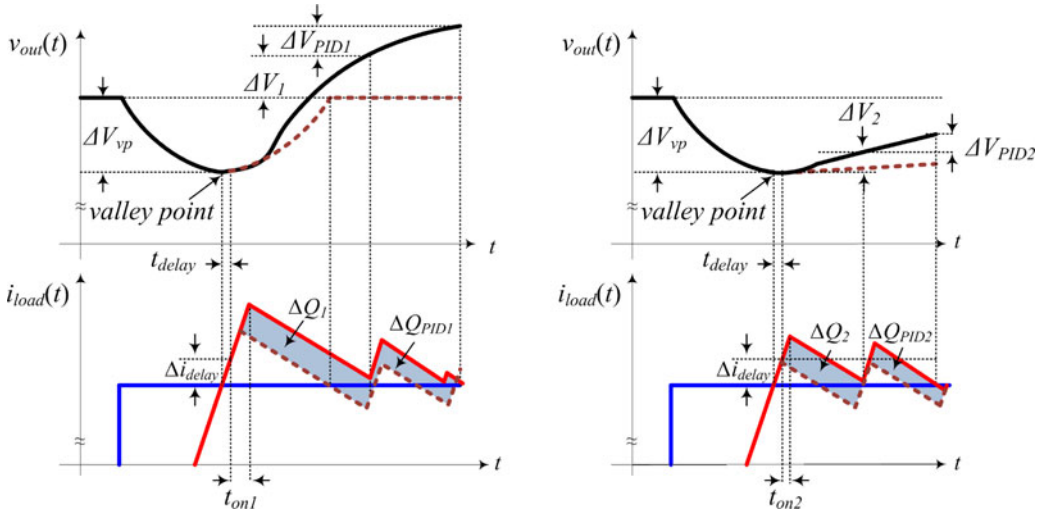

Fig. 6. Typical light-to-heavy transient of the time-optimal (left) and minimum-deviation (right) controllers illustrating the effects of nonidealities on the voltage overshoot.

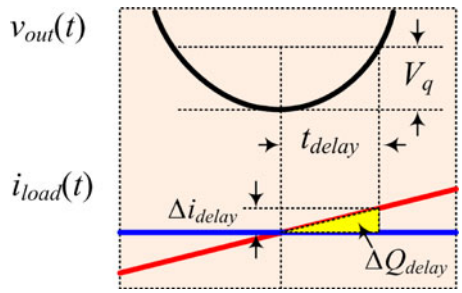

Fig. 7. Zoomed-in waveform of the valley point, illustrating the effect of the ADC quantization.

By comparing the principles of operation of both systems and looking at (1) and (2), it can be noticed that $t_{\rm on1}$ is significantly larger than $t_{\rm on2}$ causing a larger absolute voltage. It should also be noticed that, for Δv_2 smaller than the deviation at the valley point $\Delta v_{\rm vp}$, the time delay actually brings the voltage closer to the desired reference, decreasing the output voltage error, while for the time-optimal cases, the error is increased. This effect is worsened by the subsequent PID activation. As demonstrated in Fig. 6, the following synchronized action of the PID [13] further increases the voltage error of the time-optimal controller causing potential stability problems. On the other hand, in the minimum-deviation case, the PID reduces the output voltage error bringing it closer to the desired reference.

1) Quantization Effect of the ADC: Accurate detection of the valley point is important for both time-optimal and minimum-deviation controllers. In systems where an ADC is used to detect extreme points, finite quantization steps introduce additional delays that can potentially affect the system stability. The following analysis relates a quantization step of the ADC, V_q, to the valley point detection time delay. Fig. 7 shows zoomed-in waveforms of the output voltage, inductor current, and load current around the valley point. To detect the valley/peak point, the output of the ADC is usually monitored, and the point where the derivative of the error value changes sign sensed. In the case when the valley/peak point happens inside a quantization bin (as shown in Fig. 7), a delay in the detection occurs [17].

Utilizing graphical analysis of the waveforms of Fig. 7, the worst case valley point detection delay, $t_{\rm delay}$, can be calculated by combining the following equations:

$$\Delta i_{\rm delay} = \frac{V_{\rm in} - V_{\rm out}}{L} \cdot t_{\rm delay} \tag{6}$$

$$\Delta Q_{\rm delay} = \frac{\Delta i_{\rm delay} \cdot t_{\rm delay}}{2} = \frac{V_{\rm in} - V_{\rm out}}{2L} \cdot t_{\rm delay}^2 \tag{7}$$

and

$$V_q = \frac{\Delta Q_{\rm delay}}{C} = \frac{V_{\rm in} - V_{\rm out}}{2LC} \cdot t_{\rm delay}^2 \tag{8}$$

resulting in

$$t_{\rm delay} = \sqrt{\frac{2LCV_q}{V_{\rm in} - V_{\rm out}}}. \tag{9}$$

For the targeted applications [37], [38], the effect of quantization on the operation of the minimum-deviation systems can be significant [50].

III. Self-Calibrating Asynchronous Track-and-Hold ADC

The previous analysis indicates that fast transient response digital controllers [13]–[23], [26], [27] require fast and accurate analog-to-digital conversion to ensure prompt transient detection and seamless mode transitions. In [13], an application-specific 6-bit Flash ADC was presented, as a part of an optimal-time controller. The presented ADC provides fast conversion time and small quantization steps. However, it also consumes relatively large power and takes a significant silicon area, of about 0.5 mm^2, which is comparable to the size of an entire analog controller [34]. By looking at the operation of that ADC, as well as at other flash architectures, it can be noticed that comparators are poorly utilized, since only one of them is toggling during valley/peak point detection. Generally, the successive approximation register based ADCs (SAR-DAC) are more cost

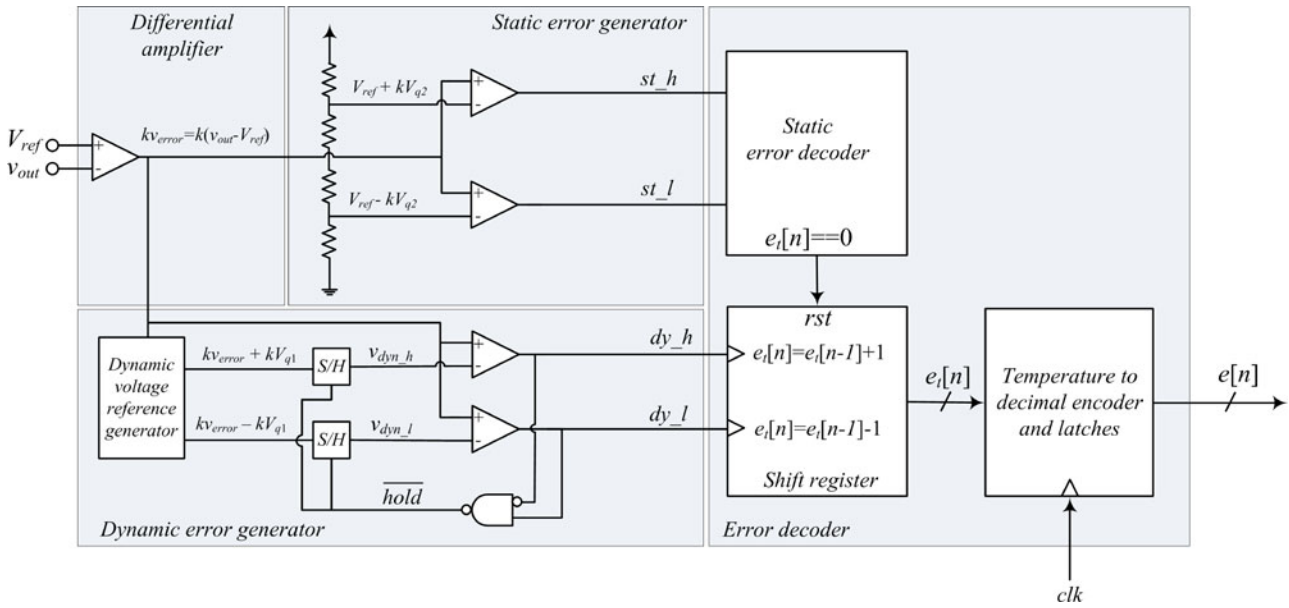

Fig. 8. Functional block diagram of the self-calibrated track-and-hold ADC.

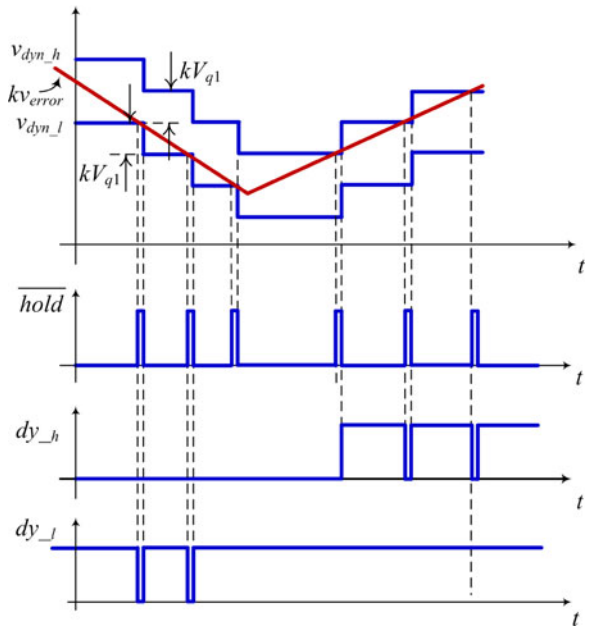

Fig. 9. Key waveforms of the asynchronous track-and-hold ADC.

effective. They can be implemented with only one comparator, a digital-to-analog converter, and a bank of registers [40]. Still, for the targeted applications, the previously presented general SAR-ADC architectures [40] are too slow and/or inaccurate. The self-calibrating asynchronous track-and-hold ADC architecture introduced in this section combines the two concepts to obtain high accuracy, fast conversion time, and implementation on a small silicon area. As described later, the ADC also incorporates self-calibration for reducing accumulated quantization errors.

The block diagram of the new ADC and its key waveforms are shown in Figs. 8 and 9, respectively. The ADC consists of a *static error generator* that produces an error signal during steady-state operation, a *dynamic error generator* creating the error during transients, a *differential amplifier* with a gain factor *k,* and error decoding logic. As shown in the figures, the complete ADC is implemented with only four comparators, a low-gain preamplifier, a voltage divider, and simple digital logic. The role of the differential stage is to amplify the output voltage error, i.e., $v_{\rm error}(t) = v_{\rm out}(t) - V_{\rm ref}$, and, in that way, reduce accuracy requirements for the comparators.

For small output voltage variations, the ADC behaves as a simple three-level asynchronous flash ADC [40], with effective quantization step V_{q2} (step seen at the input of the ADC). During transients, a digital error value $e_T[n]$ is formed by comparing the amplified analog error signal, $kv_{\rm error}(t)$, with a tracking window that is formed around it, as shown in Fig. 9. The window is created by a *dynamic voltage reference generator* and two sample and hold circuits *S/H*.

The dynamic voltage generator adds a positive and a negative offset to the signal $kv_{\rm error}(t)$ producing two outputs, whose values are $k(v_{\rm error}(t) + V_{q1})$ and $k(v_{\rm error}(t) - V_{q1})$, respectively, where V_{q1} is the effective quantization step at the input of the ADC during the dynamic mode of operation. In this implementation, the steady state and dynamic quantization steps are intentionally sized differently, so that $V_{q1} < V_{q2}$. As described in [41], such a selection improves voltage sensing during transients and, at the same time, eliminates potential limit cycling problems caused by overly small quantization steps around the reference point [39], [42].

The staircase-shaped reference window around the measured signal is created by the dynamic comparators and the sample and hold circuits. As shown in Fig. 9, each time the measured signal crosses the reference window, the sample and hold circuits are triggered and the outputs of the *dynamic voltage generator* captured. This results in an asynchronous change of the reference step by a value $\pm kV_{q1}$. At the same time, the error value is

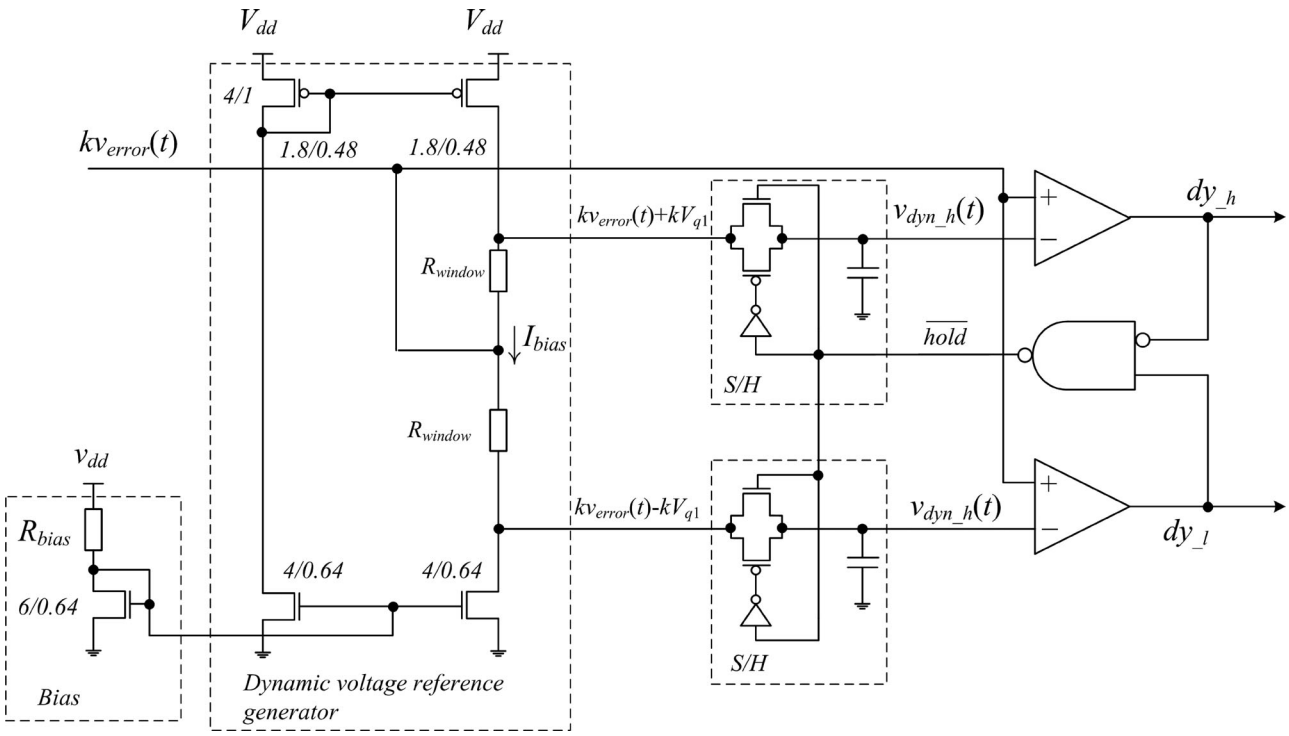

Fig. 10. Circuit level diagram of dynamic error generator.

updated. As shown in Fig. 8, the value is changed depending on the type of transient. If $kv_{\rm error}(t)$ exceeds the window $e_T[n]$ is increased by one and if it drops below it is reduced. In this way, a fast and accurate measurement with simple hardware is achieved. To eliminate potential metastability problems, the asynchronously captured error $e_T[n]$ is represented using a thermal code. This value is then converted to the binary-weighted equivalent $e[n]$ and synchronized with the rest of the system using bit pipelining [43].

A. Dynamic Error Generator

Fig. 10 shows a circuit level diagram of the dynamic error generator. It can be seen that the circuit implementation is very simple. The dynamic voltage reference generator consists of only four transistors forming a current mirror and an adder [40]. The dynamic quantization steps are adjusted by the biasing circuit and the sample and hold blocks, composed of transmission gates and capacitors.

B. Quantization, Delay Effects, and Self-Calibration

The operation of the track-and-hold ADC can be affected by the delays in the circuit. These effects can be described with the diagrams of Fig. 11, showing zoomed in ADC waveforms around a transient point for a realistic nonzero delay system. The diagrams show both the effects of the comparator delay, $t_{d\_\rm cmp}$, and the latency caused by a finite rise/fall time from one step level to another, labeled as $t_{d\_\rm tsh}$. By looking at the waveforms, we can see that the delay-caused error in quantization step to

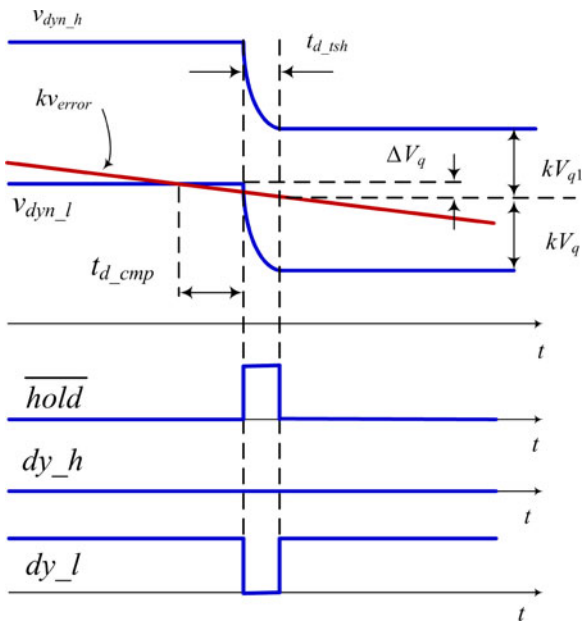

Fig. 11. Key waveforms of the realistic nonzero delay asynchronous track-and-hold ADC.

ΔV_q can be approximated as

$$\Delta V_q = \frac{dkv_{\rm error}}{dt}(t_{\rm d\_cmp} + t_{\rm d\_tsh}). \tag{10}$$

This equation indicates that the error is proportional to the rate of change of the error signal and linearly increases with the delays. In the targeted application, where the input signal can change at a fairly high rate, this error could accumulate and, consequently,

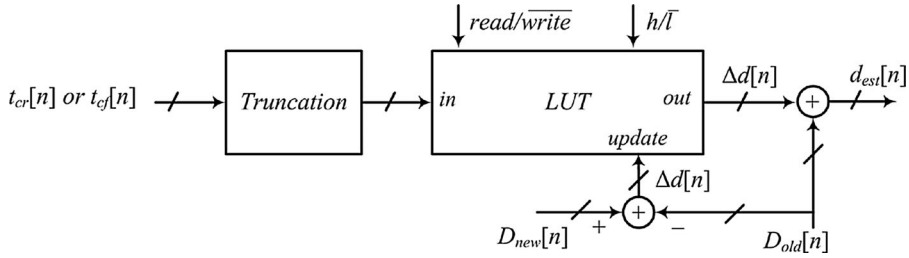

Fig. 12. Simplified block diagram of the duty ratio correction logic.

affect the controller operation. To minimize this accumulative effect, two techniques are applied. First, high-frequency noise, resulting in the high derivative of the error signal, is eliminated with the differential amplifier of Fig. 8. It is designed as a two-stage operational transconductance amplifier [40] that also acts as low-pass filter for the high-frequency noise.

The second technique is self-calibration. For this purpose, the *static error generator* from Fig. 8 is used. The self-calibration is based on the detection of zero-error bin crossing. Whenever the analog input signal enters the zero-error bin of the static comparators, the dynamic error generator is reset to zero and any accumulated error eliminated.

IV. Practical Implementation

This section describes how the converter losses and the ESR of the output capacitor affect the operation of the presented controller, as well as of the other fast response solutions. It also shows new methods and circuits that minimize the effects of these nonidealities. The delay in the peak/valley point detection is also further discussed and a dual detection method for reducing this negative effect is introduced. Accordingly, a modification of the originally presented control algorithm that incorporates a correction method is also shown.

A. Self-Adjusting Duty Ratio Corrector

In realistic, i.e., lossy, converters, the steady-state duty ratio value and small-signal dynamics change with load conditions. For a buck converter operating in a closed loop, this dependence can be calculated from the dc steady-state model [7] and described with the following equation [49]:

$$D_{\mathrm{steady}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \cdot \left(1 + \frac{R_{\mathrm{eq}} \cdot I_{\mathrm{load}}}{V_{\mathrm{out}}}\right) \tag{11}$$

where D_{steady} is the steady-state duty ratio value, I_{load} is the load current, and R_{eq} is a lumped sum of converter losses, obtained from the dc averaged model.

For this system, as well as for other fast transient response solutions where the generation of the optimal switching sequence relies on the information about the steady-state duty ratio value [13]–[22], this dependence can cause potential stability problems. Since the duty ratio values before and after a load transient are not the same, mode transient problems can occur due to an erroneous calculation of the optimal switching sequence.

To compensate for the duty ratio variations, systems shown in [13]–[22] use a high-bandwidth compensator. However, such solutions require accurate knowledge of the converter parameters and, as it will be demonstrated in the experimental section, still are not able to fully suppress subsequent voltage overshoots and undershoots. This is because, even though it is fast, the PID compensator is not able to change the duty ratio to the new steady value in a single switching cycle.

To reduce the influence of the converter losses and allow the use of a slower compensator, covering a wide range of the output filter component values, an online self-tuning duty ratio correction system is developed. The correction is performed through a repetitive two-step process. In the first step, a small LUT that relates changes in the load current, i.e., inductor current rise/fall time, and the corresponding loss-related duty ratio value increments are updated. In the second step, the stored values are used to instantaneously correct the duty ratio value. The operation of the duty ratio corrector can be explained with the help of Figs. 2(b) and 12.

For light-to-heavy load transients, the on-time of the converter main switch is measured during the inductor current ramp time, labeled as t_{cr}, in Fig. 2.(b). The obtained digital equivalent $t_{\mathrm{cr}}[n]$ is then used as the address input for the LUT of Fig. 12 producing a corresponding duty ratio correction factor $\Delta d[n]$. The correction factor is added to the old steady-state duty ratio $D_{\mathrm{old}}[n]$. This value, as described in Section II, is obtained by capturing the output of the PID compensator (see Fig. 1) before the suppression logic is activated. In this way, an estimate of the new duty ratio value $d_{\mathrm{est}}[n]$ is formed. This estimate, which takes into account converter losses, is now used during the current reconstruction phase to create the switching sequence, i.e., generate transistor on- and off-times. Once the system has returned back to the steady state and the output voltage is fully recovered, the correction factor in the LUT is updated. As shown in Fig. 12, the update is performed by comparing the actual new duty ratio value $D_{\mathrm{new}}[n]$ with the $D_{\mathrm{old}}[n]$ and storing the difference in the table. Again, the true duty ratio value is obtained by capturing the output of the PID compensator after the transient is completed.

For heavy-to-light load transients, the correction is performed in a similar manner. Now, the inductor current fall time is measured and the resulting digital value $t_{\mathrm{cf}}[n]$ is used for calibration. The indication of the type of transient is provided through h/l signal provided by the transient detection logic (see Fig. 1).

In order to minimize the size of the correction logic, a small LUT with only few entries is created. The number of entries,

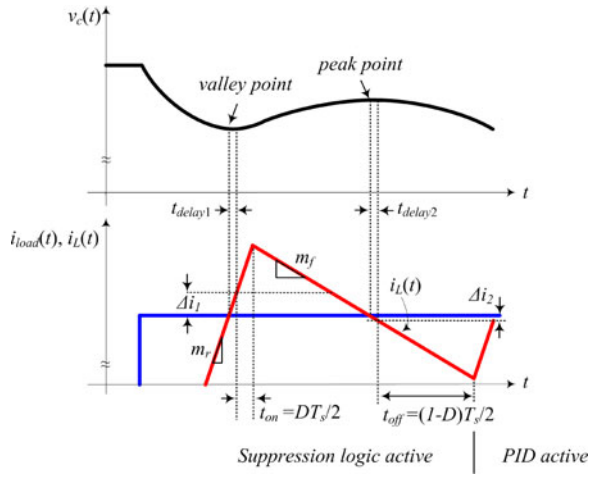

Fig. 13. Light-to-heavy load transient waveforms of a high-step down buck converter when the dual-extreme point-based delay compensation is applied.

i.e., input values to the table, is reduced through a truncation of the values $t_{\rm cr}[n]$ and $t_{\rm cf}[n]$. As it will be shown in the following section, this truncation does not have a significant effect on the performance of the correction logic and still provides seamless mode transitions. For the start up, the LUT can be initially populated with data obtained from data sheets, simulations, or from experimental testing.

B. Dual-Extreme Point-Based Delay Compensation

In Section II, it was indicated that the operation of the presented controller and other solutions relying on the detection of the peak/valley point [13]–[18], [21], [22] is sensitive to delays. As shown in the example of Fig. 13, for a buck converter with a high step down ratio, this problem is quite significant during light-to-heavy load transients.

Even a small delay in the detection of the extreme point, $t_{\rm delay1}$, causes a significant mismatch in the inductor current, Δi_1, due to a high inductor current slew rate, m_r.

To minimize this effect, a dual-extreme point detection algorithm is applied. For the case of Fig. 13, in addition to detecting the valley point, the peak output voltage during the main switch off-time is also detected. The switching sequence is then slightly modified. In this case, after the peak point is detected, the main switch off-time is extended by $(1 - D)T_s/2$. It can be seen that, now, the same delay results in a much smaller current mismatch at the end of the current reconstruction phase, Δi_2, due to the drastically lower current slew rate m_f.

The reduction in the current mismatch for a general case can be calculated from the following expression:

$$\frac{\Delta i_1}{\Delta i_2} = \frac{m_r \cdot t_{\rm delay1}}{m_f \cdot t_{\rm delay2}} \tag{12}$$

where $t_{\rm delay1}$ and $t_{\rm dealy2}$ are delays in the detection of the valley and peak point, respectively. This equation indicates as long as $t_{\rm dealy2}$ is not larger than $(m_r/m_f)*t_{\rm delay1}$, the dual point detection results in a smaller current mismatch. For most targeted applications, this condition is easily satisfied.

C. Detection of Successive Transients

In fast transient response controllers having two modes of operation, successive transients can cause toggling between the dynamic and steady-state modes. This can happen even when the disturbances following an initial large transient are small [20]. To prevent the undesirable toggling, the controller logic is slightly modified as described with the state diagram of Fig. 14. In this case, during transients, the threshold value for activating the suppression logic is dynamically adjusted. As soon as the inductor current ramping/falling phase (labeled as *HL*1/*LH*1 states in Fig. 14) is completed, the error captured at the peak/valley point, $\Delta v_{\rm peak}$, is set as the new triggering threshold. At the same time instant, the current reconstruction phase is initiated (states *HL*2/*LH*2). After the reconstruction is completed, the control task is passed to the PID compensator, which now operates with shifted threshold (state $S2$). In this state, consecutive small transients are not able to create a sufficiently large output voltage variation to reactivate suppression logic. Thus, the PID compensator remains active (stays in $S2$). For large load steps, the error value overpasses the new threshold and the suppression logic is activated again. In this way, toggle-free successive transient handling is performed. Once the voltage returns back to the steady state, the threshold is set back to its nominal value, and the PID returns to its regular state (state $S1$).

D. Transient Detector for Converters With Large Output Capacitor ESR

For the converters with relatively large output capacitor ESR, the detection of the zero capacitor current through a valley/peak point detection can be erroneous [17], [46]. In the presence of ESR, the output voltage of the converter might not coincide with that of the ideal capacitor and a premature detection of the valley/peak points can occur, as demonstrated in Fig. 15. To compensate for this and, at the same time, improve the detection of the transient instant through output capacitor estimation, solutions based on the utilization of a matched *RC* network have been proposed in [16], [17], [25], and [51]. A simple detection circuit introduced in this section utilizes the same principle as in the previous solutions. However, in addition to minimizing the ESR effects, the circuit of Fig. 16 also provides improved detection of load transients and the peak/valley points.

The operation of the detector is based on the generation of two thresholds, i.e., a threshold window, around a waveform identical to the $v_c(t)$ portion of the output capacitor (Fig. 16) and their comparison with the actual output voltage $v_{\rm out}(t)$. As soon as the output voltage exceeds one of the thresholds, a load transient is detected. The peak/valley points are detected at the point where the output voltage and $v_c(t)$ are the same. This point corresponds to the time instant at which the voltage drop across the ESR is zero, i.e., the output capacitor current is zero.

The detector consists of only three comparators, an *RC* circuit, and several transistors forming a threshold generator block. The capacitor C_1 and the resistor R_1 are selected such that, ideally, their time constant matches that of the large ESR capacitor, i.e., $CR_{\rm esr} = C_1R_1$, where $R_{\rm esr}$ is the ESR value. As shown

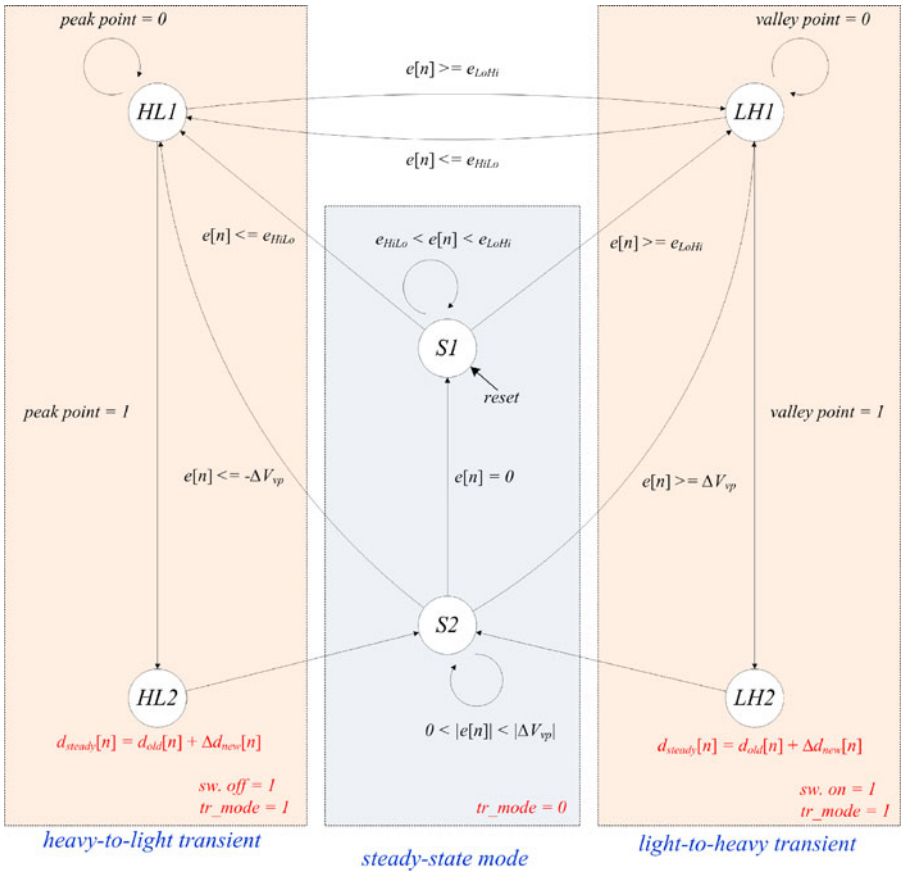

Fig. 14. Minimum-deviation controller state diagram.

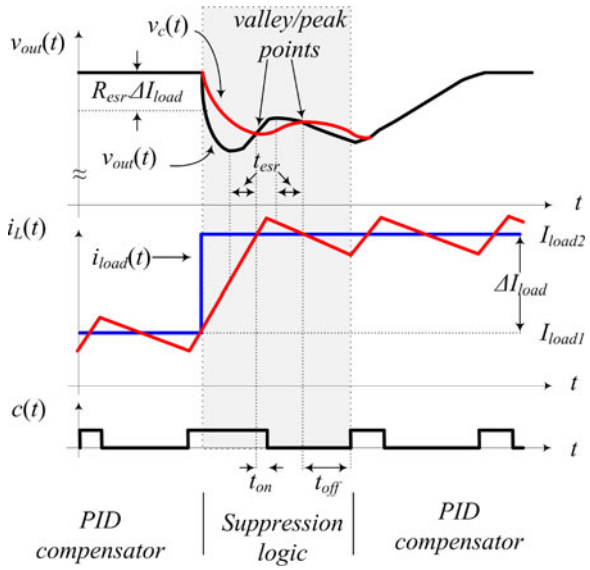

Fig. 15. Light-to-heavy load transient waveform of a buck converter with large output capacitor ESR.

in Fig. 17, for such a selection, the voltage across capacitor $C_1, v_{c1}(t)$, is identical to the $v_c(t)$ portion of the output capacitor. The threshold generation circuit operates in the same manner as the one for the track-and-hold ADC of Section III. It generates a threshold window around $v_{c1}(t)$, where the size of the threshold $\Delta V_{\mathrm{th}\_d} = R_{\mathrm{th}} I_{\mathrm{bas}\_d}$, can be adjusted with the bias circuit. In this case, the threshold steps are selected to be slightly larger than the steady-state voltage ripple, to eliminate undesirable mode transitions and, at the same time, allow a fast transient detection. The comparators detect load transients, when the output voltage exceeds the threshold point. They also detect the point where v_{c1}(t) and $v_{\mathrm{out}}(t)$ are the same.

In this case, the peak/valley point detection signals from the ADC are blanked. This is done because the presented detector does not suffer from quantization problems and, consequently, offers a better accuracy.

E. Controller Stability

The main stability concern of the minimum-deviation controller is related to the steady-state and transient mode transitions. For ideally operating transition logic, the overall stability of the system can be assumed if the PID compensator provides stable operation during steady state. This is because the current reconstruction logic used during transients reconstructs the new inductor current steady-state value. The output voltage deviation is the only remnant the PID must manage. For such a case, the small-signal assumptions are valid and stability is maintained [7].

However, as discussed through the paper, in a realistic converter, system delays and converter losses affect operation of the controller causing inductor current and duty ratio value

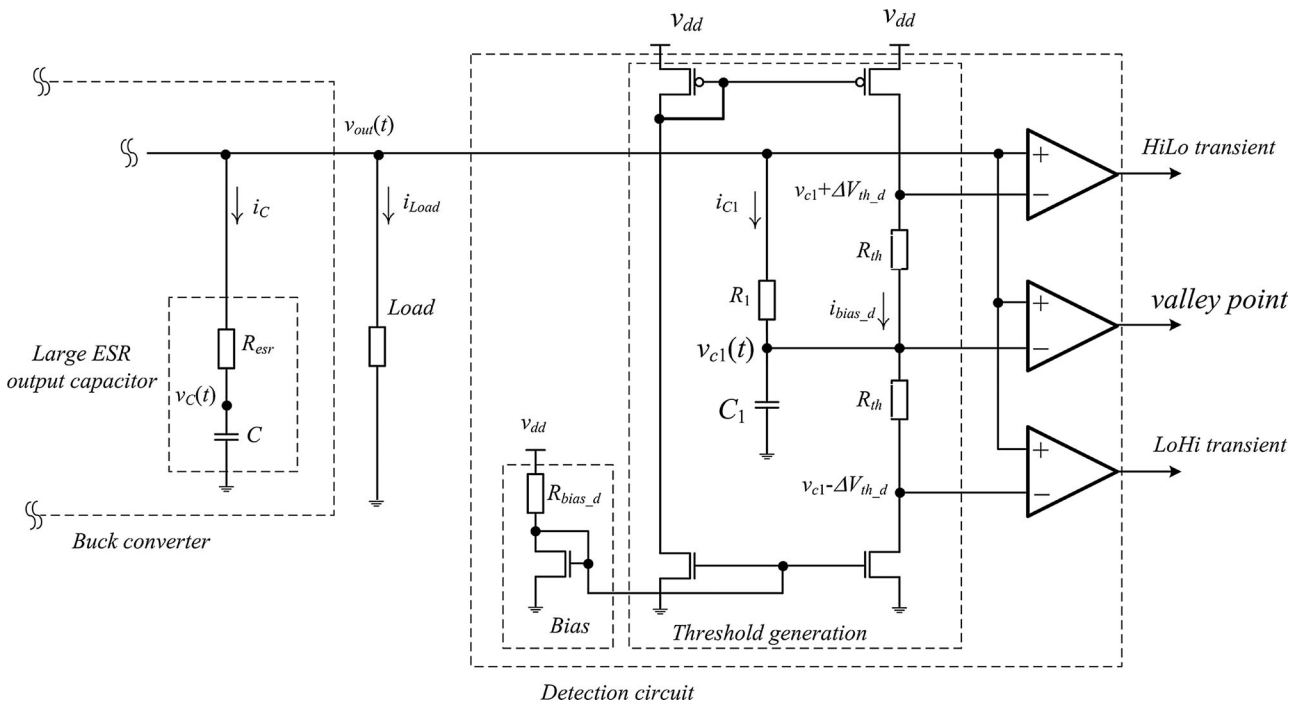

Fig. 16. Transient and valley point detection circuit for SMPS utilizing output capacitors with large ESR.

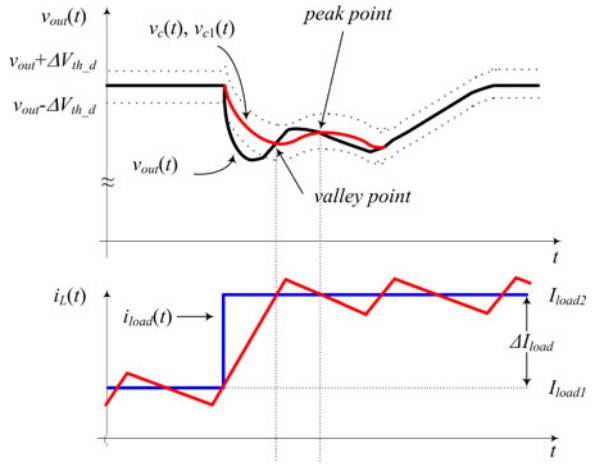

Fig. 17. Key waveforms of the large ESR transient detector.

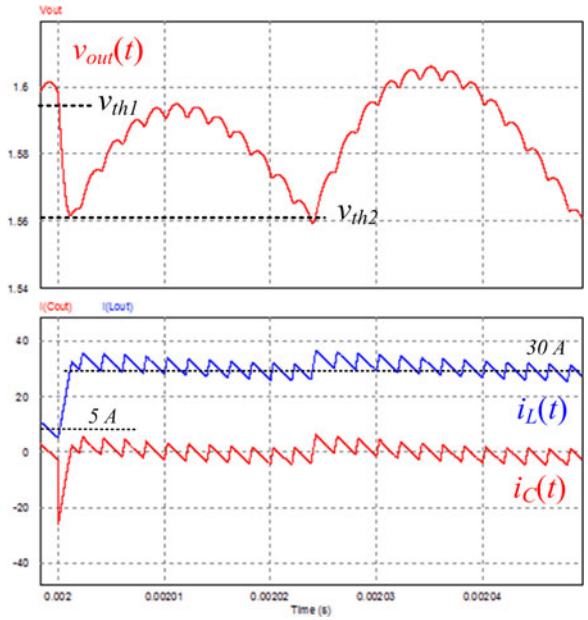

Fig. 18. Closed-loop simulations of an 80% efficient 12–1.6-V buck without duty ratio correction for a 5–30-A load transient. (Top) Output voltage. (Bottom) Inductor and output capacitor currents.

mismatches at the end of the current reconstruction phase and possible stability problems. From the PID compensator point of view, these mismatches have the same effect as load transients, causing undesirable additional transient logic activation, as shown in [44] for near-optimal controller. To eliminate these problems, the PID should be fast enough to limit the mismatch-caused voltage variation to a lower than the threshold value. In this way, undesirable toggling between the modes can be eliminated. This practically means that the accuracy of the current reconstruction logic determines the bandwidth requirement of the controller and that for a well-behaved transient logic, the PID bandwidth can be reduced.

The effect of errors in the current reconstruction is demonstrated in waveforms of Fig. 18. They are showing load transient response simulations of a lossy buck converter that is regulated with a minimum-deviation controller prior to the activation of the duty ratio correction logic.

It can be seen that a mismatch in the duty ratio values causes multiple transients even in the case when the adaptive threshold adjustment described in Section IV-C is applied. Such a scenario can be envisioned right after the start-up of the converter before the LUT of the duty ratio correction logic is populated or if the

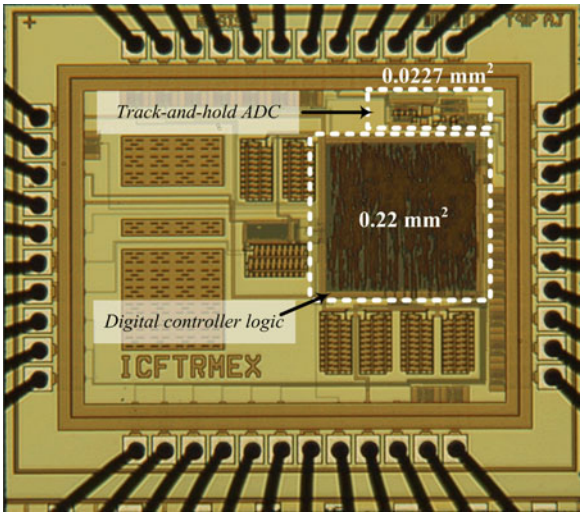

Fig. 19. Photograph of the minimum-deviation digital controller IC.

TABLE I
MINIMUM-DEVIATION DIGITAL CONTROLLER IC SUMMARY

Technology	*TSMC 0.18μm CMOS*
Supply Voltage (Digital / Analog)	1.8 V / 3.3 V
DPWM resolution	13 bits
DPWM nominal frequency	500 kHz
ADC area	0.02 mm^2
ADC current consumption	0.24 mA
Digital logic area	0.22 mm^2
Digital logic current consumption	0.2 mA
Total area	0.24 mm^2

table is not populated with correct values. The influences of other elements affecting the operation of the current reconstruction logic described in previous sections can have similar effects and hence affect the system stability.

V. CONTROLLER IC SIMULATIONS AND EXPERIMENTAL RESULTS

Based on the diagrams of Figs. 1, 9, 10, 12, and 13, a minimum-deviation digital controller IC was designed and fabricated in a 0.18-μm CMOS process. The operation of this circuit is experimentally verified with a commercial two-phase buck converter module [47] having low ESR output capacitor. The module provides up to 35 A per phase. The PID compensator and the dual output DPWM of Fig 1 utilize a hybrid architecture, whose detailed description is found in [35]. The complete digital logic takes about 4500 gates and is fully implemented through the Verilog hardware description language and automated design tools. Besides the previously described controller, the digital logic of the prototype IC also includes additional testing and debugging blocks that, out of the total number, take about 500 digital gates. A photograph of the prototype IC is shown in Fig. 19 and its characteristics are listed in Table I.

It can be seen that, even with the extra digital logic occupying about an 11% of the digital part, the IC takes only 0.24 mm^2 of the silicon area, which is comparable to state-of-the-art analog solutions [34]. In the following section, the results of the post-layout simulations and experimental verifications of the chip are presented.

A. Analog-to-Digital Converter

To maximize the speed of the ADC comparators, shown in Fig. 15, their outputs are not connected to the output pins. In this way, a significant capacitive loading of the comparators, which slows down transitions, is avoided. Hence, to verify the functionality of the ADC, postlayout simulations are used.

Fig. 20 shows Cadence Hspice postlayout simulation results of the self-tuning track-and-hold flash ADC with the preamplifier gain $k = 5$ and the quantization step of $V_q = 4$ mV. The simulations are shown for a 250-kHz, 100-mV peak-to-peak triangular input. The results verify that the tracking window, described in Section III, follows the output voltage and proper operation of the static and dynamic comparators (see Fig. 8). It can be seen that the tracking signal has 24 levels covering a 96-mV range and, thus, confirming about 4-mV quantization steps.

In order to reduce the transmission gate charge feedthrough and leakage current, minimum-size transistors are utilized in the construction of the transmission gates of Fig. 15. Also, to speed up charging and discharging of the sample and hold capacitors, while ensuring stable voltage during the hold period, minimum values of the capacitors for this design are selected. The capacitors values of 2 fF were selected through simulations, using readily available information about the CMOS process. Also, the leakage currents of the transmission gate and comparator inputs were taken into account. Through this design, the (dis)charging delays, t_{d_tsh}, are kept below 2 ns and the capacitor leakage current is reduced to practically negligible values (about 1 fA), maintaining one-bin accuracy during the hold period of several seconds. The simplicity (low-transistor count) of the dynamic error generator allows for tight layout over a small silicon area and, thus, low transistor mismatch, in accordance with state-of-the-art practices [40].

The area and current consumption of the new ADC are measured from the fabricated prototype. To demonstrate hardware efficiency, the results are compared with a 7-bit flash ADC [48]. The flash ADC is fabricated in the same technology, has approximately the same quantization steps, and covers the same operating range. The results of the comparison are shown in Table II. It can be seen that the track-and-hold ADC has about ten times smaller silicon area and power consumption making it much better suited for the targeted cost-sensitive applications.

It should be noted that the 15-ns conversion time allows this ADC to be used with other converters operating at significantly larger switching frequencies than 500 kHz. The actual range of applications is defined by the output voltage slew rate during transients. To function properly, the ADC should be able to create a tracking window around the output voltage under all transient conditions. The ADC is able to track the output voltage

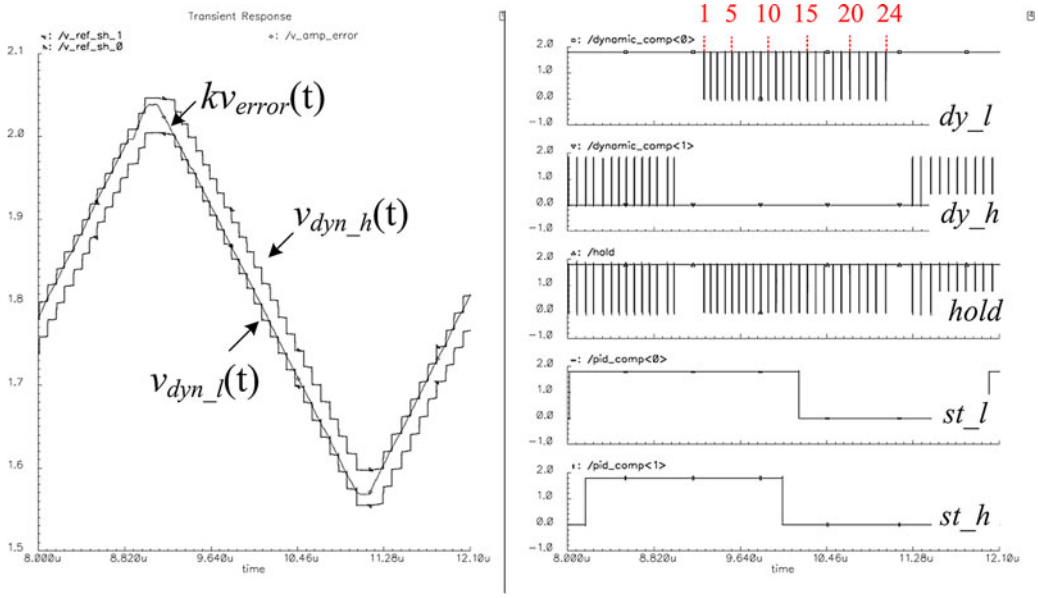

Fig. 20. ADC Simulation result: amplified input voltage and tracking window (left) and comparator outputs (right).

TABLE II
COMPARISON OF THE TRACK-AND-HOLD ADC AND A CONVENTIONAL 7-BIT FLASH ADC

	Track-and-hold ADC	*Flash ADC*
Quantization voltage (mV)	4	4
Conversion time (ns)	15	15
Area (mm^2)	0.0227	0.2
Current Consumption (mA)	0.24	2

as long as the voltage slew rate is smaller than the ratio of the quantization step and conversion time, which for this design is approximately 0.26 V/μs.

The implementation of this ADC requires custom designed comparators for a given voltage slew rate. The complexity of its design is affected by the input voltage slew rate and the speed requirements. For a given accuracy, the comparator design simplifies as the voltage slew rate at its input increases [40]. On the other hand, it becomes more complex for faster conversion times [40]. Taking that into account, it can be assumed that the presented architecture will be usable in upcoming converters operating at tens of megahertz. This is because it can be expected that the increased speed requirements for the comparators will be partially or fully be nullified with a larger output voltage slew rate that is also likely to occur.

B. Closed-Loop Verification

The closed-loop verification of the minimum-deviation controller IC was performed with a state-of-the-art industrial two-phase, 12–1.8-V, 500-kHz, buck converter module, providing 35 A per phase [37], [47]. The ESR of the 400-μF output capacitor is just 0.5 mΩ and each phase uses a 0.47-μH inductor. The performances of the IC are tested for the case when one of the phases is disabled and in the two-phase interleaved modes of operation.

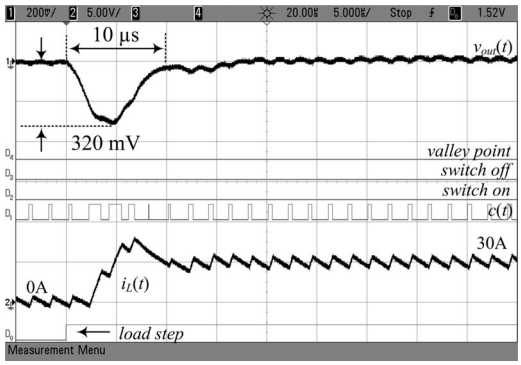

Fig. 21. Transient response waveforms for a 0–30-A load step (wide-bandwidth conventional compensator): Ch1: Output converter voltage (200 mV/div); Ch2: actual inductor current $i_L(t)$ 30 A/div; D0: load transient triggering signal; D1: pulse-width modulated control signal; D2: main switch control signal created by suppression logic; D3: synchronous rectifier control signal created by the suppression logic; D4: peak valley point detection; Time scale is 5 μs/div.

1) Load Transient Response and Comparison With a Conventional High-Bandwidth Controller: To verify transient performance of the minimum-deviation controller, its response is compared to that of a conventional wide-bandwidth controller, where both systems regulate operation of the single-phase buck. To create a conventional controller, the same IC was used. In this case, the transient suppression logic was disabled and the PID compensator designed to have the bandwidth of a one-tenth of the switching frequency. The tests were performed with an ultra fast load transient circuit reaching the maximum load current of 35 A in 20 ns, i.e., having the current slew rate of 1.75 A/ns.

The experimental waveforms of Fig. 21 show the transient response results of the conventional controller. In Fig. 22, the suppression logic is active. In this case, the duty ratio correction logic is not employed.

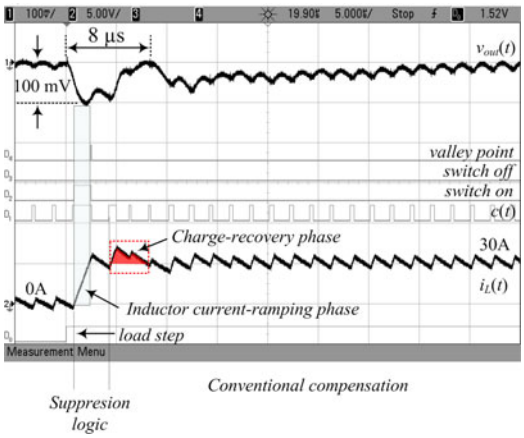

Fig. 22. Transient response waveforms for a 0–30-A load step (minimum-deviation controller IC): Ch1: output voltage (200 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; D0: load transient triggering signal; D1: pulse-width modulated control signal; D2: main switch control signal created by suppression logic; D3: synchronous rectifier control signal created by the suppression logic; D4: peak/valley point detection; Time scale is 5 μs/div.

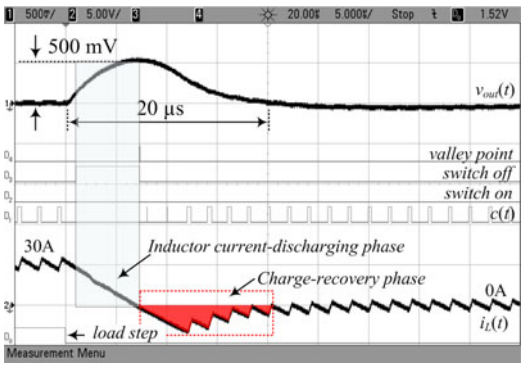

Fig. 23. Transient response waveforms of the minimum-deviation controller IC for a 30–0-A load heavy-to-light load transient: Ch1: output voltage (500 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; D0: load transient triggering signal; D1: pulse-width modulated control signal; D2: main switch control signal created by suppression logic; D3: synchronous rectifier control signal created by the suppression logic; D4: peak valley/point detection signal; Time scale is 5 μs/div.

The results demonstrate that the activation of the suppression logic results in about three times smaller deviation, allowing for a proportional reduction of the output capacitor. Fig. 23 shows operation of the minimum-deviation controller IC during a heavy-to-light load step.

2) Consecutive Load Transients: The minimum-deviation controller behavior in the presence of two consecutive load transients, a 0–12 A followed by a 12–30 A, is shown in Fig. 24. It can be seen that the controller seamlessly moves between the transient suppression and PID modes of operation.

3) Operation With a Dual-Phase Buck: The waveforms of Fig. 25 show the response of the controller with the two-phase buck. It can be seen that the minimum voltage deviation is obtained with a very low inductor current overshoot, i.e., low current stress.

4) Duty Ratio Corrector and Parameter-Insensitive Operation: The experimental results shown in the previous sections are obtained with the utilization of a high-bandwidth PID compensator, which partially compensates for the loss-related duty ratio variations. As mentioned in Section IV-A, such an approach requires a fairly accurate knowledge of the converter *LC* parameters and, as can be seen from the experimental waveforms of Figs. 22 and 24, still causes a slight undershoot after the current reconstruction phase. The experimental results shown in this section demonstrate that, by utilizing duty ratio correction logic, the requirements for the PID compensator bandwidth can be drastically reduced. This allows for a slower and more robust compensator design that can operate with a very wide range of the output filter *LC* values, practically allowing parameter-insensitive operation.

To demonstrate the effectiveness of the duty ratio corrector, the bandwidth of the PID compensator is set to be about a 1/50th of the switching frequency, i.e., reduced five times, and the performance of the IC are compared with and without duty ratio correction logic. Fig. 26 shows the transient response of the controller IC for a load step from 0 A to a half of the nominal load current without correction logic. It can be seen that, even at this load level, a subsequent voltage undershoot larger than the one caused by the original transient occurs.

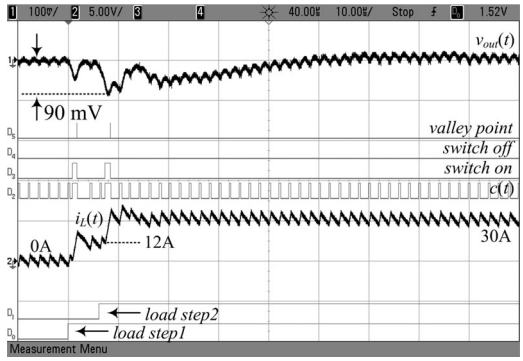

Fig. 24. Consecutive light-to-heavy load transients: Ch1: output voltage (100 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; D0, D1: load transient triggering signals; D2: pulse-width modulated control signal; D3: main switch control signal created by suppression logic; D4: synchronous rectifier control signal created by the suppression logic; D5: peak valley/point detection signal; Time scale is 10 μs/div.

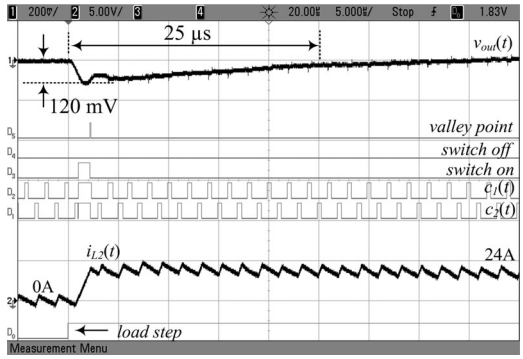

Fig. 25. Operation with a dual-phase buck: Ch1: output voltage (200 mV/div); Ch2: inductor current of one phase 30 A/div; D0: load transient triggering signals; D2, D3: pulse-width modulated control signals; D4: main switch control signal created by suppression logic; D4: synchronous rectifier control signal created by the suppression logic; D5: peak valley/point detection signal; Time scale is 5 μs/div.

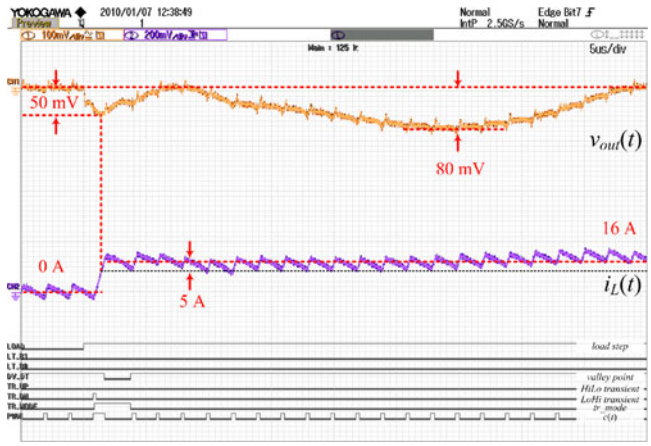

Fig. 26. Transient response for a 0–16-A load step for the case when a slow PID compensator without duty ratio correction logic is used. Ch1: output voltage (100 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5 μs/div.

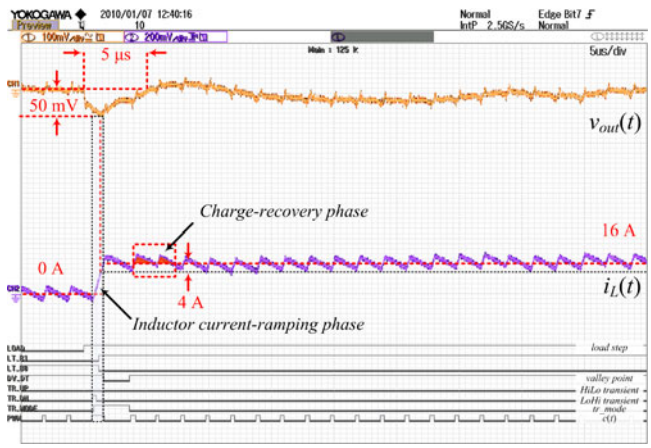

Fig. 27. Transient response of the controller IC for a 0–16-A load step with a slow PID compensator when the duty ratio correction logic is active. Ch1: output voltage (100 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5 μs/div.

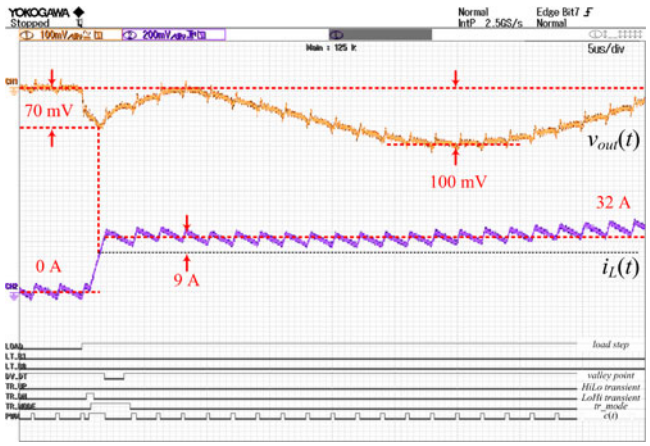

Fig. 28. Transient response for a 0–32-A load step for the case when a slow PID compensator without duty ratio correction logic is used. Ch1: output voltage (100 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5 μs/div.

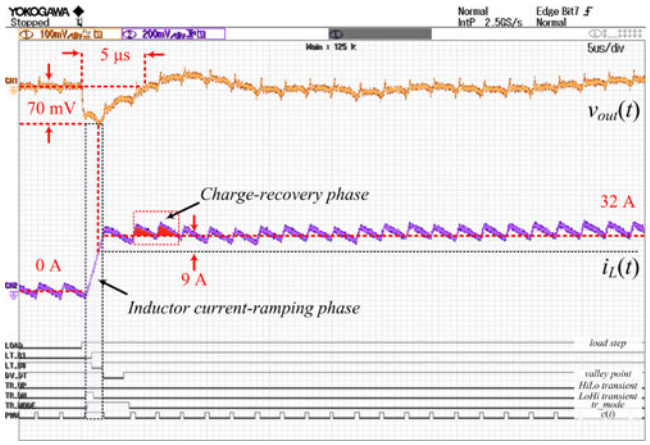

Fig. 29. Transient response for a 0–32 A with a slow PID compensator when the duty ratio correction logic is active. Ch1: output voltage (100 mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5 μs/div.

Fig. 27 shows operation with the slow PID compensator when the duty ratio corrector is active. It can be seen that the correction logic not only eliminates the subsequent transient but also results in virtually seamless mode transition. Even though a slow PID compensator is utilized, the consequent undershoot existing in the previous case is eliminated.

Fig. 28 and 29 demonstrate operation of the system with the same slow PID compensator for a load step from 0 A to a 90% of the full load. In this case, the low ESR output capacitor is replaced with a one that has four times larger ESR value and, to compensate for that, an off-chip transient detector, which was described in Section IV-D, was used. The performances are again verified through a comparison of the operation with and without the duty ratio corrector.

It can be seen that the duty ratio correction logic eliminates subsequent transients caused by the duty ratio variations. Also, a comparison with the waveforms of Fig. 22 shows that the detection circuit further reduces voltage deviation, even when the output capacitor with a much larger ESR is used. This is because of the reduction of the delay in the detection of the load transient instant. In this case, for triggering, estimate of the output capacitor current is used and, as discussed in Section II, the delay existing in the voltage-threshold triggered systems is practically eliminated. A wider adoption of this detection method, and consequent practical on-chip implementation, will probably depend on solving the problems related to the mismatch in the time constants [51], which is characteristic for all *RC*-based methods [16], [17], [25].

VI. Conclusion

A practical minimum-deviation digital controller IC for single- and dual-phase high-frequency dc–dc switching converters is introduced. The IC combines a very simple parameter-insensitive transient suppression algorithm with a novel architecture of the ADC to obtain cost-effective implementation.

In steady state, the IC operates as a conventional digital pulsewidth-modulated voltage-mode controller. During transient, it activates the suppression logic. The suppression logic

reconstructs the inductor current such that both its dc and ripple components match those in the new steady state. The full voltage recovery task is then passed to the steady-state compensator. Such an arrangement results in a very simple hardware implementation. The suppression logic only utilizes a readily available duty ratio value and performs a single division by two, through binary shifting.

The self-calibrating asynchronous ADC only uses four comparators, a low-gain amplifier, and several transistors. Its operation is based on the track-and-hold principle and the construction of a moveable comparison window around the amplified error signal. To cancel any accumulated error, the ADC utilizes a self-calibration process that is performed during the input signal zero-voltage crossings.

The IC also incorporates two new elements that minimize effects of the power stage losses and system delays. The first is adaptive duty ratio correction logic. The corrector compensates for the duty ratio variations due to the converter losses, which can cause mode transition-related stability problems. It uses a simple dynamically updatable LUT to estimate changes in the duty ratio value, based on the size of the current step, and, accordingly, corrects the switching sequence. The second element is a dual peak/valley detection block. It minimizes the effects of system delays during transients. The detection block captures the capacitor current zero crossings when the inductor current slew is the lowest and, consequently, the effect of the system delays minimized.

Also in this paper, a circuit that reduces the effects of the output capacitor ESR and, at the same time, improves detection of the load transient and peak/valley point is proposed.

The IC is implemented in a 0.18-μm CMOS process on a silicon area no large than that of the state-of-the-art analog solutions. Experimental results obtained with the IC verify minimum-deviation response and stable mode transitions for various operating conditions.

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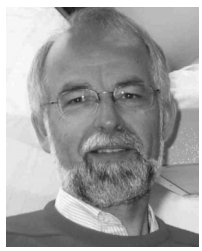
Dr. Prodic is a recipient of an IEEE Power Electronics Transactions Paper Award, 2012 University of Toronto Inventor of the Year Award, and multiple IEEE conference paper prizes. He is especially proud of two Excellence in Teaching Awards, elected and given by the University of Toronto undergraduate students.



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