High-Frequency Digital PWM Controller IC for DC–DC Converters

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***Abstract*—This paper describes a complete digital PWM controller IC for high-frequency switching converters. Novel architecture and configurations of the key building blocks are A/D converter, compensator, and digital pulse-width modulator, are introduced to meet the requirements of tight output voltage regulation, high-speed dynamic response, and programmability without external passive components. The implementation techniques are experimentally verified on a prototype chip that takes less than 1 mm^2 of silicon area in a standard 0.5 μ digital complementary metal oxide semiconductor (CMOS) process and operates at the switching frequency of 1 MHz.**

***Index Terms*—DC–DC switch-mode power conversion, digital control, digital pulse width modulation.**

I. Introduction

DIGITAL controllers can offer a number of advantages in dc–dc power converters, and various analysis, design and implementation aspects of this emerging area are receiving increasing attention [1]–[17]. Advanced power management techniques rely on integration of power control and conversion functions with digital systems [2]–[5]. Compensator and protection features can be programmable, reducing or eliminating the need for passive components for tuning. As a result, the same digital controller hardware can be used with a range of power converter configurations and power-stage parameter values. Digital controllers have inherently lower sensitivity to process and parameter variations. Furthermore, it is possible to implement control schemes that are considered impractical for analog realizations. For example, the ability to precisely match phase-shifted duty ratios has been applied to develop a simple, robust control for voltage-regulator modules (VRMs) implemented in a dedicated digital controller IC [7], [8]. In transformer-isolated dc–dc converters, digital signal transmission through the isolation can be used to address limited bandwidth and/or large gain variations associated with standard analog approaches. In general, more sophisticated control methods can be applied to achieve improved dynamic responses.

Manuscript received February 1, 2002; revised September 24, 2002. This work was supported by the National Semiconductor Corporation through the Colorado Power Electronics Center. Recommended by Associate Editor S. B. Leeb.

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Digital Object Identifier 10.1109/TPEL.2002.807121

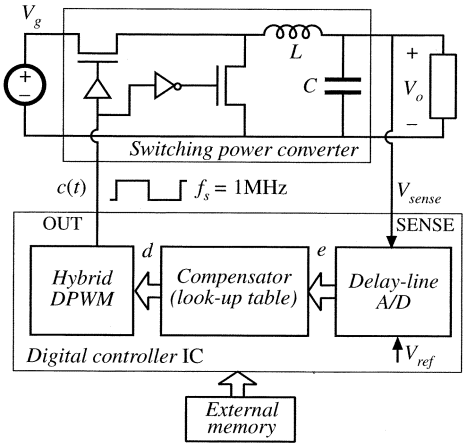

Fig. 1. Block diagram of the digital PWM controller IC for a dc–dc switching converter.

From the standpoint of the controller integrated circuit (IC) design, the main advantage of the digital approach is that well-established and automated digital design tools can be applied to shorten the design cycle. The design is described at the functional level using a hardware description language (HDL). Starting from HDL-based design, synthesis, simulation and verification tools are available to target the design to standard-cell ASIC or FPGA implementation. The design can then be easily moved to a different process, integrated with other digital systems, or modified to meet a new set of specifications. In contrast to analog IC controller realizations, the digital controller design scales well, and can thus take advantages of advances in fabrication technologies.

In spite of the apparent potential benefits, broader acceptance of digital techniques in high-frequency low-to-medium power dc–dc applications is still hampered by a combination of issues including cost/performance, availability, and/or ease of use. Available DSP systems or micro-controllers either lack the performance to even match what is readily available with standard analog controller ICs, or are exceedingly complex for the intended application.

The purpose of this paper is to describe implementation techniques aimed at constructing complete, programmable digital controller ICs capable of operating at high switching frequencies (100 KHz to MHz range) and having silicon area, power consumption, and complexity comparable to or lower than standard analog ICs. A block diagram of the digital PWM controller IC around a synchronous buck converter is shown in Fig. 1 [14]. This IC implements the constant-frequency PWM control by

1) sampling the output voltage using a novel delay-line A/D converter;

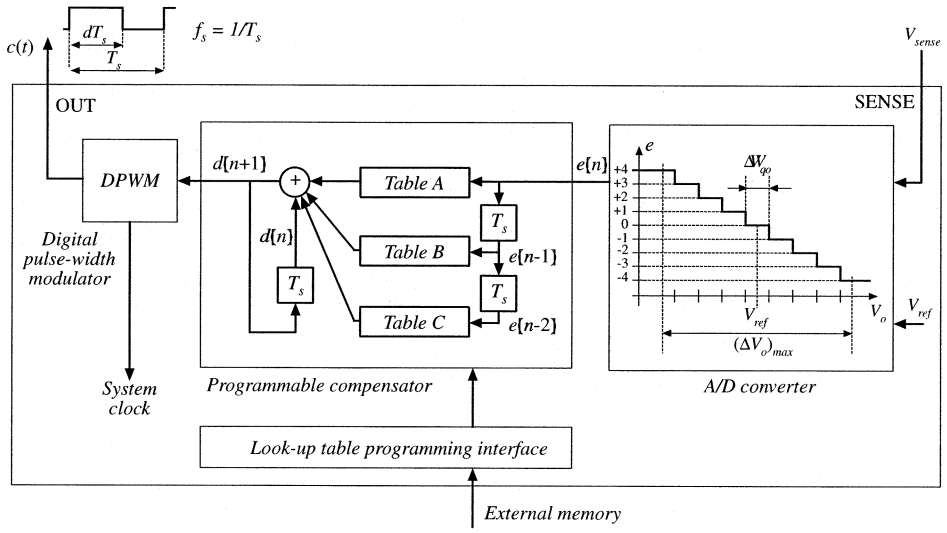

Fig. 2. Architecture of the digital PWM controller IC.

2) processing the error signal through a programmable digital compensator based on look-up tables;
3) generating a constant-frequency PWM waveform to control the power switches using a hybrid digital pulse-width modulator (DPWM).

The paper is organized as follows: the controller architecture is described in Section II. Architecture and realization of the hybrid DPWM are described in Section III, together with experimental results obtained from the fabricated prototype chip. The delay-line A/D converter and experimental results illustrating its operation are presented in Section IV. The controller design and experimental results obtained with the buck voltage regulator are summarized in Section V.

II. Digital Controller Architecture

The power converter and the controller form a closed-loop feedback system, the purpose of which is typically to regulate the output voltage V_o to match a precise, stable voltage reference V_{ref} (or a scaled version of the reference) over a range of input voltage values and load currents, and over a range of process and temperature variations. In the basic voltage-mode PWM control method, the output voltage is sensed and compared to the reference. The error signal is passed to the compensator (i.e., the "error amplifier"). The output of the compensator is the input to the pulse-width modulator, which in turn produces the constant-frequency variable duty-ratio signal to control the switching power transistors. In the voltage-mode architecture, analog compensator design is usually based on averaged converter models and standard feedback techniques [18]. The proposed digital controller architecture to implement the voltage-mode PWM control scheme is shown in Fig. 2.

In general, the sensed voltage is a scaled version of the output voltage, $V_{sense} = HV_o$, but in this paper we assume $H = 1$. The output voltage is sampled by an analog-to-digital (A/D) converter, to produce the digital error signal $e[n]$. The sampling occurs once per switching period T_s. Here, the index n refers to the current switching period. To justify the A/D conversion characteristic shown in Fig. 2, it is useful to examine typical voltage regulation requirements. The dynamic voltage regulation requirement implies that output voltage $V_o(t)$ must always (including load or input voltage transients) stay in a specified range around reference V_{ref}, from $V_{ref} - (\Delta V_o)_{\max}/2$ to $V_{ref} + (\Delta V_o)_{\max}/2$. In addition, the static voltage requirement usually means that in steady state the dc output voltage must equal the reference voltage, with some allowed tolerance, $V_o = V_{ref} \pm \Delta V_o/2$. To meet these requirements, we conclude that the analog equivalent V_q of the least significant bit (LSB) in the A/D characteristic must not be greater than the specified ΔV_o, but also that the conversion range must include only a relatively small range $(\Delta V_o)_{\max}$ of voltages around the reference. In practice, the specifications for ΔV_o and $(\Delta V_o)_{\max}$ are such that only a few digital values are needed to represent the values of the error signal $V_{ref} - V_o$. For example, in Fig. 2, the digital representation of the error signal takes one of only nine possible values, from -4 to $+4$ (decimal). In general, although the A/D converter must have a fine voltage resolution to maintain the ability to regulate the output voltage precisely, only a few bits are needed to represent the digital error signal $e[n]$. A flash A/D converter that meets these requirements is proposed in [8]. A novel delay-line A/D configuration that takes advantage of the required static A/D characteristic, and lends itself to a simple digital implementation is described in Section IV.

In addition to relaxing the requirements for the A/D converter itself, the fact that the error signal can be represented with only a few bits leads to a simpler implementation of the next building block—the compensator. The purpose of the compensator is to take the current ($e[n]$) and previous ($e[n-1]$, $e[n-2]$, etc.) samples of the error signal and compute the new value of the duty ratio d, which is the variable that controls the power converter through the pulse-width modulator. The computation (i.e., the control law) in the compensator can be designed according to digital control theory well described in literature (see [20], for example). However, standard implementation of linear control laws in the compensator requires digital adder(s) and digital multiplier(s), which increases the area and/or the clock frequency requirements in a practical chip implementation. If

the compensator coefficients are restricted to multiples of 2, or 1/2, simpler logic shifters can be used instead of multipliers [6], but this approach puts restrictions on the realizable control laws. Taking advantage of the fact that only a few bits are used to represent the error signal e, we instead implement the required computation using three look-up tables and an adder, as shown in Fig. 2. The current and the previous values of the digital error signal serve as addresses to the corresponding locations in the look-up tables. Since the error signal e can take only a few different values, the number of entries in the look-up tables is relatively small, and the implementation area is also small. In addition, the computation can be done in a single or in a few clock periods, so that the clock frequency requirements are also low. Complete details of the compensator implementation on the prototype test chip can be found in [14].

The look-up table compensator can be programmed to perform different control laws simply by programming the entries in the look-up tables. The most general control law supported by the configuration shown in Fig. 2 is given by

$$d[n+1] = d[n] + \alpha(e[n]) + \beta(e[n-1]) + \gamma(e[n-2]) \quad (1)$$

where $\alpha(\cdot)$, $\beta(\cdot)$ and $\gamma(\cdot)$ are linear or nonlinear functions of the digital error signal. A variety of control laws can be implemented. For example

$$d[n+1] = d[n] + ae[n] + be[n-1] + ce[n-2] \quad (2)$$

where a, b, and c are constants, corresponds to the basic PID controller. Similar discrete-time control laws have been used in other applications of digital control for switching power converters [1], [7], [8], [19].

In the table-based controller implementation, once the coefficients a, b and c are selected (to achieve a desired closed-loop bandwidth and adequate phase margin, for example), the products $(a \cdot e)$, $(b \cdot e)$, and $(c \cdot e)$ are precomputed for all possible values of the error e and programmed into the look-up tables. On the prototype chip, upon start-up, the tables are loaded from an external memory. As alternatives to the external memory, the tables could be easily preprogrammed and hard-wired on the chip at design time, or programmed from other system components via a suitable interface at run time.

The programmable feature of the compensator means that the same controller hardware can be used with different power-stage configurations and parameters, without need for external passive components to tune compensator response. In addition, using the same configuration, it is possible to explore the use of various nonlinear control laws.

The digital pulse-width modulator (DPWM) completes the controller architecture. The DPWM takes the digital value d of the duty ratio and produces the pulsating waveform $c(t)$ that controls the power transistor(s) in the power converter. A high-resolution, high-frequency DPWM is needed to achieve the required operation at high switching frequency and tight regulation of the output voltage. Our implementation of the DPWM is described in Section III.

III. Hybrid Digital Pulse-Width Modulator

In the system where a power converter and a digital controller form a feedback loop, the digital pulse-width modulator serves the purpose of a digital-to-analog (D/A) converter. The discrete set of duty ratios and ultimately the discrete set of achievable output voltages depends on the DPWM resolution. If the DPWM resolution is not sufficiently high, an undesirable limit-cycle oscillation can occur [7], [16], [17]. In particular, if none of the achievable output voltages fall into the range of ΔV_o around the reference, in steady state the duty ratio must oscillate through a range of two or more values. A necessary condition to avoid the limit-cycle oscillation is that the output voltage increment that corresponds to the least-significant bit of the duty ratio command d must be smaller than ΔV_o [16]. This condition has been evaluated as a function of the steady-state input and output voltages for different converter configurations [17]. The requirement for a high-resolution, high-frequency DPWM is an important consideration in practical realizations of digitally controlled high-frequency power supplies.

A high-resolution, high-frequency digital pulse-width modulator (DPWM) can be constructed using a fast-clocked counter and a digital comparator [2], [6], [7]. To achieve n-bit resolution at the switching frequency f_s, the required clock frequency is $2^n f_s$. This can easily result in more difficult timing constraints, and increased power consumption. For example, an 8-bit resolution at the switching frequency of $f_s = 1$ MHz would require a clock frequency of 256 MHz. It has been shown that the fine time resolution and much lower power consumption can be achieved using a tapped delay-line scheme similar to a ring oscillator that operates at the switching frequency [4], [8]. However, this implementation requires a larger-area digital multiplexer. The DPWM architecture we selected is based on a hybrid delay-line/counter approach similar to the design described in [5]. In this approach, an n-bit resolution is achieved using an n_c-bit counter ($n_c < n$), whereas the remaining $n_d = n - n_c$ bits of resolution are obtained from a tapped delay line.

Fig. 3 shows a simplified diagram and operating waveforms of the hybrid DPWM, for the case where 4-b ($n = 4$) resolution is obtained using a 2-b counter ($n_c = 2$) and a four-cell ring oscillator ($n_d = 2$, $2^{n_d} = 4$), which consists of resettable flip-flops as delay cells.

At the beginning of a switching cycle, the output set-reset (SR) flip-flop is set, and the DPWM output pulse $c(t)$ goes high. The pulse that propagates through the ring at the frequency $2^{n_c} f_s = 4 f_s$ serves as the clock for the counter. The complete switching period is divided into $2^{n_d} 2^{n_c} = 16$ slots. At the time when the counter output matches the top n_c most significant bits of the digital input (i.e., the duty ratio command) d, and a pulse reaches the tap selected by the n_d least significant bits of d, the output flip-flop is reset and the output pulse goes low. In the example waveforms of Fig. 3, the duty ratio of the output pulse is 11/16. The basic delay cell in the ring oscillator of Fig. 3 consists of a single resettable flip-flop. The cell delay and the number of cells in the ring determine the switching frequency f_s. To adjust switching frequency, the cell can be modified by inserting additional delay elements between flip-flop output and the next

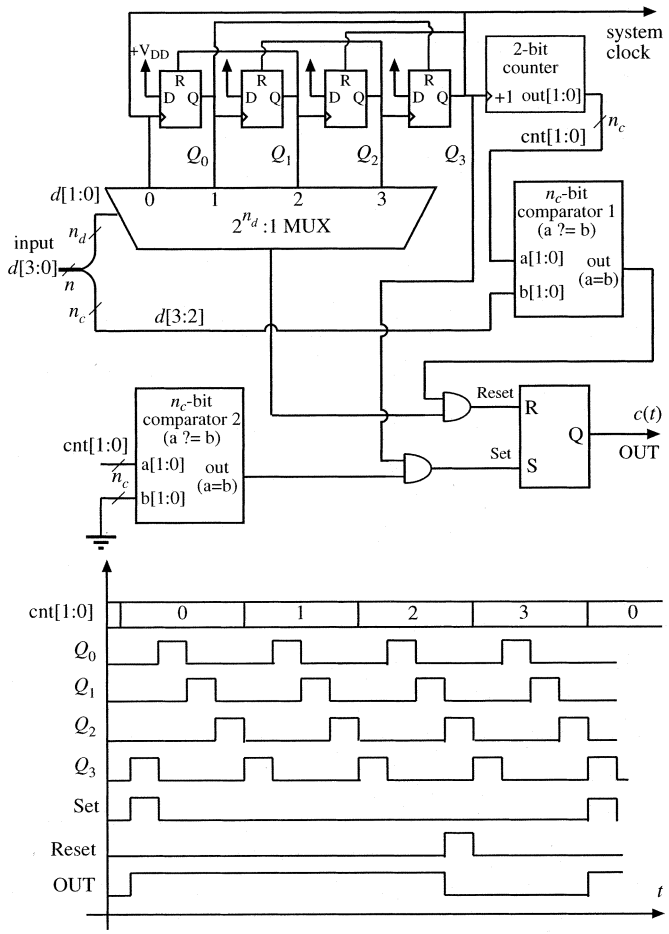

Fig. 3. Simplified diagram of the 4-b hybrid DPWM, together with operating waveforms.

cell. The additional delay elements can be standard logic gates, or gates with adjustable delay, if switching frequency tuning or synchronization with an external clock are desired.

The self-oscillating DPWM implementation shown in Fig. 3 has several desirable properties: it is a simple HDL-based design with an even number of time slots in a period, and it offers the ability to stop and restart the oscillations on command (by gating the propagation of the signal through the ring).

In the experimental prototype chip, the DPWM was designed for 8-b resolution ($n = 8$) using a 3-b counter ($n_c = 3$), and a 32-cell long ring ($n_d = 5$). The DPWM operates at the switching frequency $f_s = 1$ MHz. The ring oscillates at $2^{n_c} f_s = 8$ MHz. This 8 MHz signal is used as the system clock for the entire prototype chip.

Experimental results of Fig. 4 show the measured duty ratio of the output pulses as a function of the 8-b digital input d. The minimum (3.1%) and the maximum (97.3%) duty ratios are set by design [14].

IV. Delay-Line Analog-to-Digital Converter

As discussed in Section II, static and dynamic output voltage regulation capabilities depend on the characteristics of the A/D converter. Conventional high-speed, high-resolution A/D converters consume power and chip area, and require precision

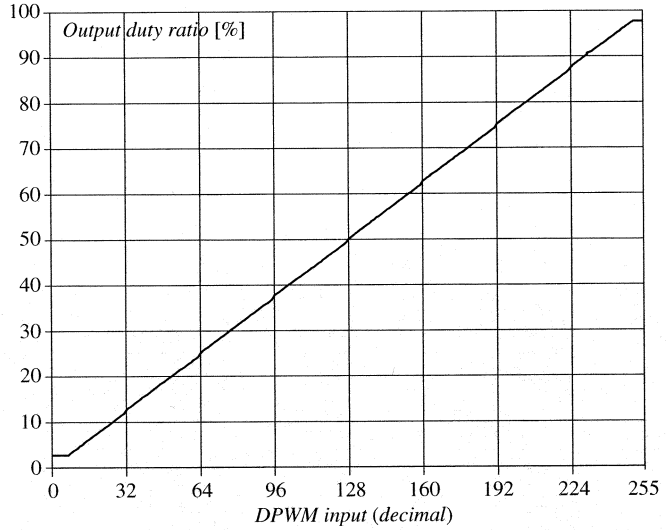

Fig. 4. Measured duty ratio of the output pulses as a function of the digital input d for the experimental prototype controller chip.

analog components. Also, in the switching power supply, the sensed analog voltage V_{sense} comes from the output of a switching power converter. This signal usually has significant switching noise, which can be a problem for many conventional A/D converters such as the basic flash configuration.

Taking into account the specific requirements discussed in Section II, we introduce a novel delay-line A/D configuration shown in Fig. 5. The delay-line A/D converter is based on the principle that the propagation delay of a logic gate in a standard CMOS process increases if the gate supply voltage is reduced. To the first order, the propagation delay t_d as a function of the supply voltage V_{DD} is given by [22]

$$t_d = K \frac{V_{DD}}{(V_{DD} - V_{th})^2} \tag{3}$$

where V_{th} is the MOS device threshold voltage, and K is a constant that depends on the device/process parameters, and the capacitive loading of the gate. It can be observed that increasing V_{DD} results in a shorter delay. For the supply voltages higher than the threshold V_{th}, the delay is approximately inversely proportional to V_{DD}.

As shown in Fig. 5, a string of delay cells (consisting of logic gates) forms a delay line supplied from the sensed analog voltage, $V_{DD} = V_{sense}$. Each delay cell has an input, an output, and a reset R. When the reset input is active high, the cell output is reset to zero. A possible implementation of the delay cell is shown in Fig. 6. To control the cell delay, additional gates can be added to the cell implementation. Also, in the configuration of Fig. 5, the taps do not have to be taken from consecutive cells, giving an additional degree of freedom in designing the A/D conversion characteristic.

Typical timing waveforms in the delay-line A/D converter are shown in Fig. 7. To perform a conversion, at the beginning of a switching cycle, a test pulse *test* is propagated through the delay line. After a fixed conversion-time interval, which is equal to $(6/8)T_s$ in the example waveforms of Fig. 7, the taps (t_1 through t_8) are sampled by the signal *sample*, which is the clock for the

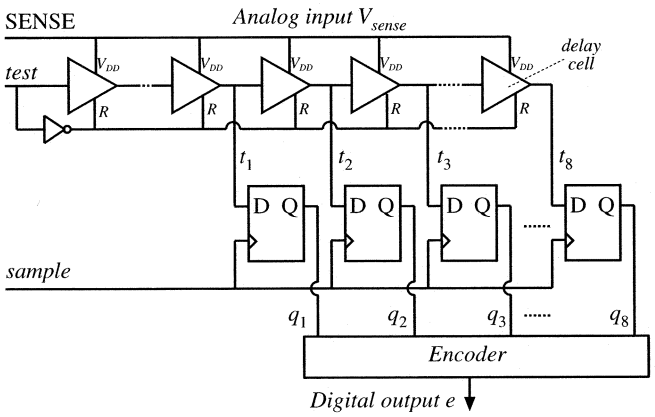

Fig. 5. Basic delay-line A/D converter configuration.

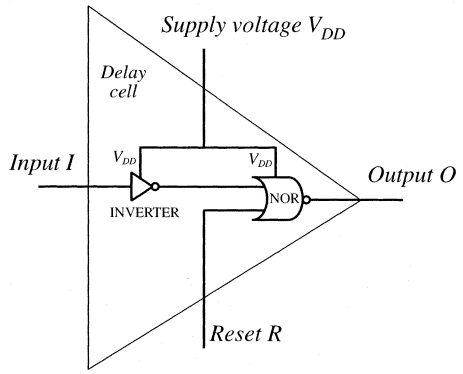

Fig. 6. Possible implementation of the delay cell for the delay-line A/D converter.

D-type flip-flops. The result at the output of the flip-flops (signals q_1 to q_8) is passed to a digital encoder to produce the digital output signal e. The last portion of the switching cycle is used to reset all cells in the delay line, to prepare for the next conversion cycle.

If the analog input voltage (i.e., the sensed converter output voltage V_{sense}) is lower, the cell delay t_d is longer, and the test pulse propagates to fewer taps along the delay line. For a higher sensed voltage, the cell delay is shorter and the test pulse propagates further along the delay line. The sampled tap outputs (q_1 to q_8) give the A/D conversion result in the "thermometer" code, similar to the output of the well-known flash A/D converter. For example, for the case illustrated by the waveforms of Fig. 7, the test pulse propagates to the taps t_1 through t_6, but not to the taps t_7 and t_8, so that the flip-flop outputs are $(q_1, q_2, \ldots, q_8) = 11\,111\,100$. Ideally, when the sensed voltage V_{sense} equals the reference V_{ref}, the test pulse propagates to the first half of the tapped delay cells. In the delay-line A/D converter of Fig. 5, this zero-error case corresponds to the flip-flop outputs equal to $(q_1, q_2, \ldots, q_8) = 11\,110\,000$. The encoder is used to produce the output e in the desired code. The digital output e gives the digital error between the sensed voltage and the reference. The desired steady state operation of the power supply corresponds to the digital error signal equal to zero. Details of the encoding scheme implemented on the prototype chip can be found in [14].

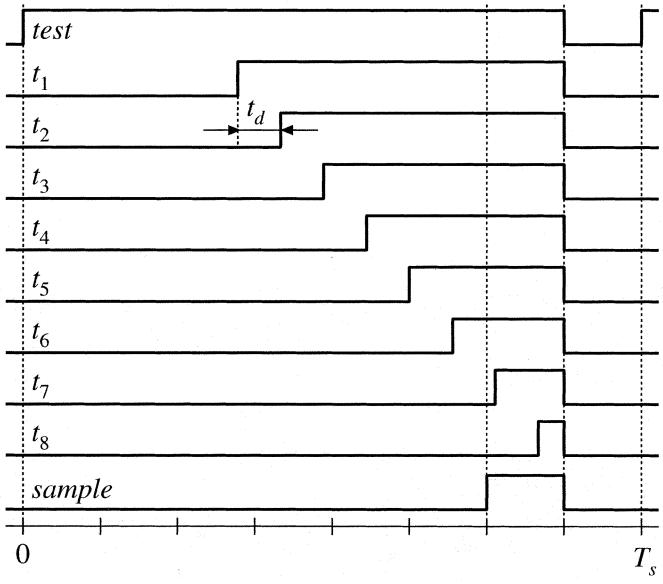

Fig. 7. Timing waveforms in the basic delay-line A/D converter.

In the delay-line A/D converter design, the length of the delay line effectively determines the reference value V_{ref} around which the A/D conversion characteristic is centered. The number of taps and the tap delay determine the range $(\Delta V_o)_{\max}$ and the effective LSB resolution V_q of the A/D converter. In the experimental prototype chip, the delay-line length and the tap delay were designed (by simulation) to result in $V_{ref} \approx 2.5$ V, and $V_q \approx 40$ mV. Eight taps are used to result in the A/D voltage conversion range $(\Delta V_o)_{\max} = (8+1)V_q \approx 360$ mV.

A unique advantage of the proposed delay-line A/D converter is that it's basic configuration does not require any precision analog components, and that it can be implemented using standard logic gates. Therefore, it scales well, and can be based on HDL code. Sampling at high switching frequencies (in the range from hundreds of KHz to several MHz) can be easily accomplished in modern sub-micron CMOS processes. Furthermore, the configuration has a built-in noise immunity: the sampling can extend over a portion of the switching period over which the input analog signal V_{sense} is effectively averaged. Therefore, the digital output is not affected by sharp noise spikes in the output voltage of a switching converter.

The delay-line A/D conversion characteristic measured on the experimental prototype chip is shown in Fig. 8. The shaded portions of the characteristic indicate the voltages where the output code is flipping between the adjacent values. It can also be observed that the A/D characteristic exhibits some nonlinearity. Most importantly, however, the conversion characteristic is monotonic, and the widths of the code "bins" are approximately equal to the desired V_q value. In a power supply application, the observed A/D imperfections (code flipping, and nonlinearity) have very little effect on the closed-loop operation. In steady state, the output voltage simply converges to the zero error bin ($e = 0$). On a set of 10 prototype chips, we measured the average of the zero-error bin width to be equal to 53 mV, with a standard deviation of 3.6 mV. The measured reference voltage is $V_{ref} = 2.7$ V, while the measured current consumption of the A/D converter is only about 10 μA.

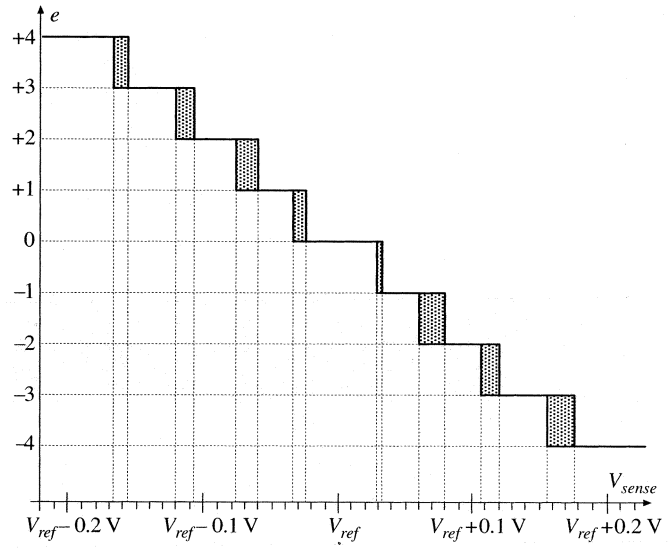

Fig. 8. Measured static characteristic of the delay-line A/D converter in the experimental prototype controller IC.

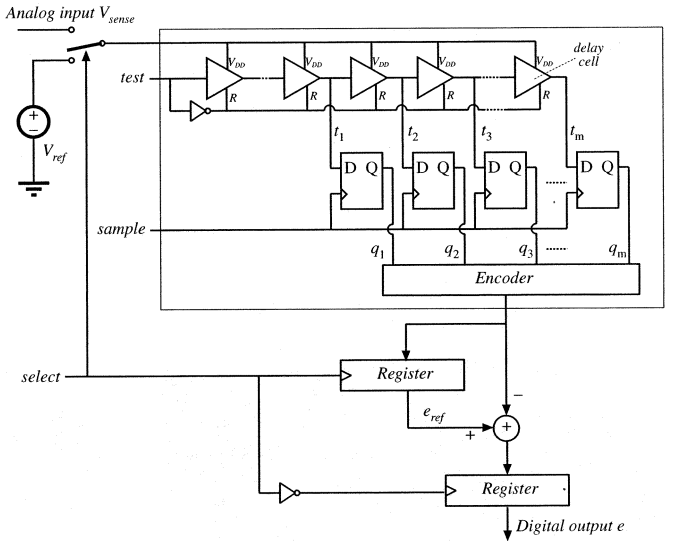

Fig. 9. Delay-line A/D converter configuration with digital calibration.

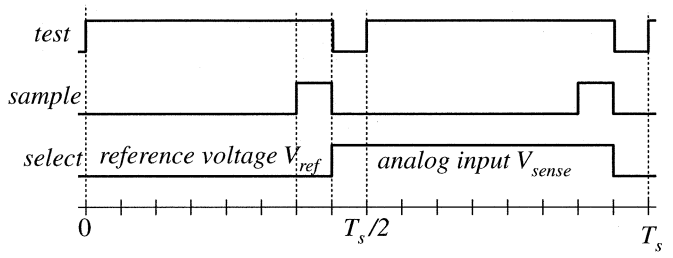

Fig. 10. Timing waveforms in the delay-line A/D converter with digital calibration.

A. Calibration of the Delay-Line A/D Converter

The basic delay-line A/D converter results in a reference voltage V_{ref} that is indirectly determined by the length of the delay line and by the delay versus voltage characteristic of the delay cell. In practice, because of process and temperature variations, the reference value obtained by the basic delay-line A/D configuration cannot be precisely controlled. Variations in the effective V_{ref} result in variations of the regulated output voltage, and the power supply may fail to meet the specified static and dynamic voltage regulation. Precise calibration of the delay-line A/D converter against process and temperature variations can be accomplished in a number of ways. One possible approach is to apply a stable, precise V_{ref} (generated using standard bandgap techniques) to the input of the A/D converter, and to subtract (digitally) the conversion result from the value obtained when the actual analog input voltage V_{sense} is applied. The delay-line A/D converter with this digital calibration scheme is shown in Fig. 9, together with possible timing waveforms in Fig. 10.

Two conversions are performed in each switching period. In one half of the switching period, the reference voltage V_{ref} is applied to the A/D converter. The result of the reference conversion e_{ref} is ideally 0, but the actual value can be different because of process and temperature variations. The reference conversion result e_{ref} is stored in a register. In the second part of the period, the input analog voltage V_{sense} is applied to the A/D converter, and the result is subtracted from e_{ref} to obtain the (precisely calibrated) value of the error signal. If desired, the reference conversion for the purpose of calibration of the delay-line A/D converter does not have to be performed in every switching period.

V. Experimental Results

The digital PWM controller described in Sections II–IV, was designed and implemented in a standard 0.5 μ CMOS process. The results obtained with the prototype chip used as the controller for a closed-loop PWM voltage regulator are summarized in this section.

A. Prototype Controller IC

The chip design was described in Verilog HDL. Synopsys synthesis and timing verification tools were used to reduce the design to standard-cell gates. Digital and mixed-signal simulations were performed using Cadence tools. Given the standard-cell based digital design, it was possible to use automated (Avanti) place and route tools to produce the chip layout.

The chip layout is shown in Fig. 11. The chip has 84 pins, most of which are used only for test purposes. The only I/O pins essential for operation are OUT, SENSE, the supply and ground, as well as the pins needed to interface with the external memory. Less than 0.2 mm^2 is taken by the delay-line A/D converter. The total active chip area is less than 1 mm^2. With further optimization of HDL-based design and the synthesis process, it is expected that this area can be reduced further. It should also be noted that the design scales with the technology so that the overall area can be significantly reduced by moving it to a deeper sub-micron process.

As described in Section II, the compensator includes 3 look-up tables [addressed by $e(n)$, $e(n-1)$, and $e(n-2)$]. The error signal generated by the delay-line A/D converter can have nine possible values. The outputs of the three tables are

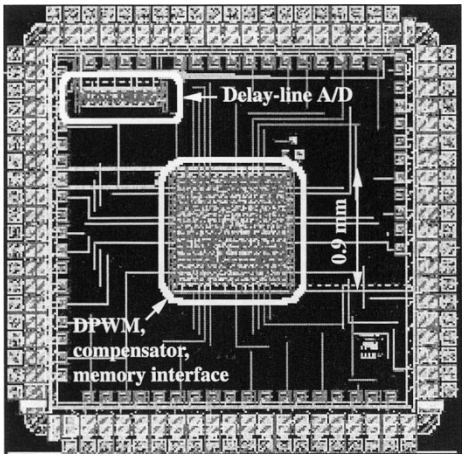

Fig. 11. Layout of the prototype chip.

8, 9 , and 8-b values, respectively. Therefore, the total on-chip memory storage is 225 b. The bit-lengths of the table entries are determined by the range of error signal values ($-4 \leq e \leq 4$), and by the desired precision of pole-zero placement [17]. The adder produces a 10-b signed value which is reduced to the 8-b duty ratio command ($0 < d < 255$) by limiting the value to unsigned, and by truncating the least significant bit. When the converter is powered up, it loads the compensator table entries from the external memory, and then starts to sample the output voltage and produce the pulsating waveform $c(t)$.

B. Voltage Regulator Example

To demonstrate closed-loop operation, the controller chip is used with low-power synchronous buck converter shown in Fig. 1. The input voltage V_g is between 4–6 V, the output voltage is regulated at $V_o = 2.7$ V, the load current is from 0–1.5 A, and the switching frequency is 1 MHz. The filter components are $L = 1$ μH and $C = 22$ μF. Another voltage regulator example with the same controller IC is shown in [15].

The digital compensator design was based on a discrete-time model of the power converter. Note that the synchronous buck converter shown in Fig. 1 always operates in continuous conduction mode (CCM). The small-signal linearized model derivation follows the steps described in [21] to obtain the following discrete-time control-to-output transfer function:

$$G_{vd}(z) = \frac{\hat{v}_o}{\hat{d}} = \frac{(T_s^2/LC)V_g}{z^2-(2-T_s/RC)z+(1+T_s^2/LC-T_s/RC)}. \quad (4)$$

For the purpose of designing the compensator, the complete discrete-time model of the voltage regulator is shown in Fig. 12. In the controller part of the model, all signals are represented as signed integers. The A/D converter is modeled as a gain and a delay. The A/D gain is equal to $1/V_q$, where $V_q \approx 50$ mV is the A/D resolution, i.e., the analog equivalent of the least significant bit. The delay, which is approximately equal to one switching period, is from the sampling time to the time when the updated duty cycle of the output gate-drive waveform $c(t)$ affects the converter operation. The PID compensator transfer function in Fig. 12 follows from (2), except that the delay has been taken into account as the separate block. Using the root-locus technique [20], the coefficients $a = 32$, $b = -62$ and $c = 31$ are found so that:

1) stable operation with sufficient margin is obtained for all operating conditions;
2) the table entries $(a \cdot e)$, $(b \cdot e)$, and $(c \cdot e)$ can fit into the controller memory for all possible values of the error $-4 \leq e \leq 4$;
3) limit cycle oscillations do not occur [16].

Fig. 13 shows load transient waveforms obtained by MATLAB/Simulink simulation of the complete voltage regulator model, including the effects of sampling, discretization, saturation limits of the A/D and the DPWM, and switching in the power stage.

Experimental load transient responses are shown in Figs. 14 and 15. It can be observed that the output voltage stays regulated inside the $(\Delta V_o)_{\max}$ range, and that the output voltage returns to

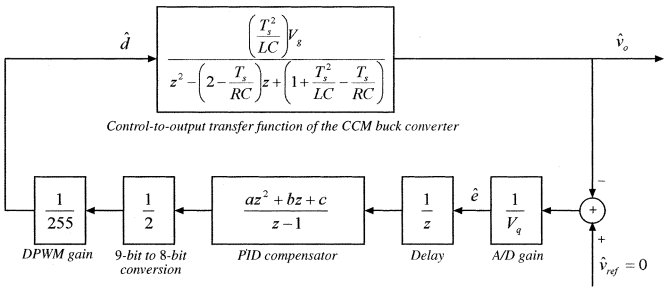

Fig. 12. Small-signal discrete-time model of the voltage regulator of Fig. 1.

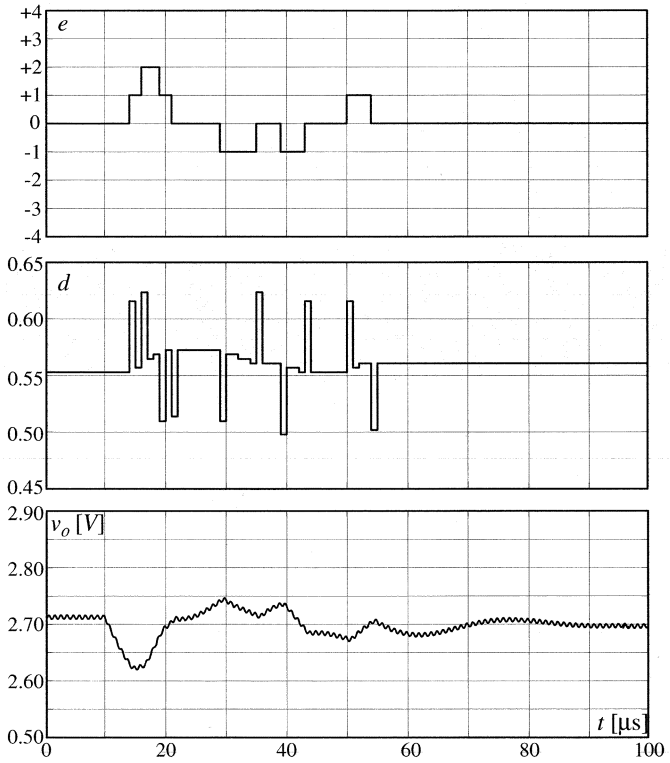

Fig. 13. Load transient (0.5 A to 1.0 A) waveforms obtained by MATLAB/Simulink simulation of the closed-loop voltage regulator of Fig. 1: $V_g = 5$ V, $V_o = 2.7$ V, $L = 1$ μH, $C = 22$ μF, $f_s = 1$ MHz.

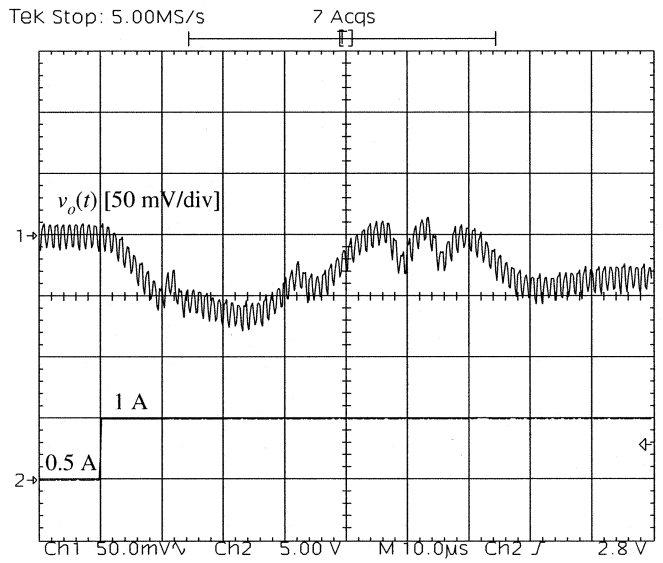

Fig. 14. Experimental 0.5 A to 1.0 A load transient response for the closed-loop voltage regulator of Fig. 1: $V_g = 5$ V, $V_o = 2.7$ V, $L = 1$ μH, $C = 22$ μF, $f_s = 1$ MHz.

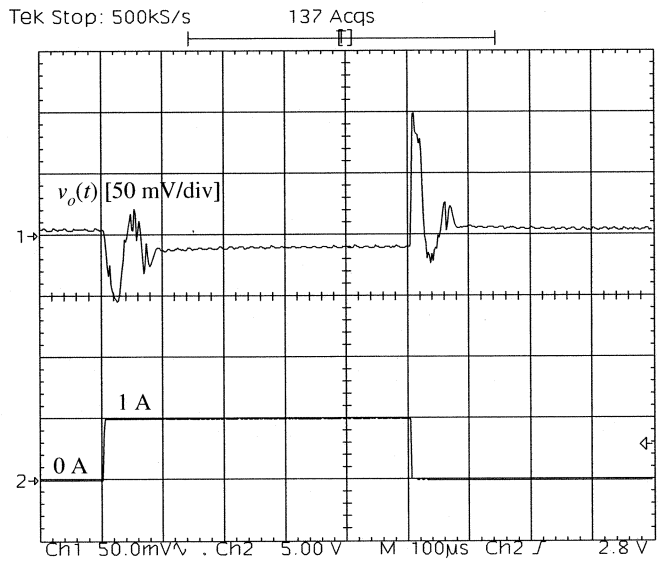

Fig. 15. Experimental 0 A to 1.0 A load transient response for the closed-loop voltage regulator of Fig. 1: $V_g = 5$ V, $V_o = 2.7$ V, $L = 1$ μH, $C = 22$ μF, $f_s = 1$ MHz.

regulation (ΔV_o around the reference) within tens of microseconds even under large (0 A to 1 A) load transients.

Measured static load and input voltage regulation results are shown in Fig. 16. It can be seen that steady-state output voltage stays within the zero-error bin around the reference value.

VI. Conclusion

This paper describes a complete digital controller IC for high-frequency dc–dc switching converters. Novel controller architecture and configurations of the key building blocks: the A/D converter, the compensator and the digital pulse-width modulator (DPWM), are introduced to meet the requirements

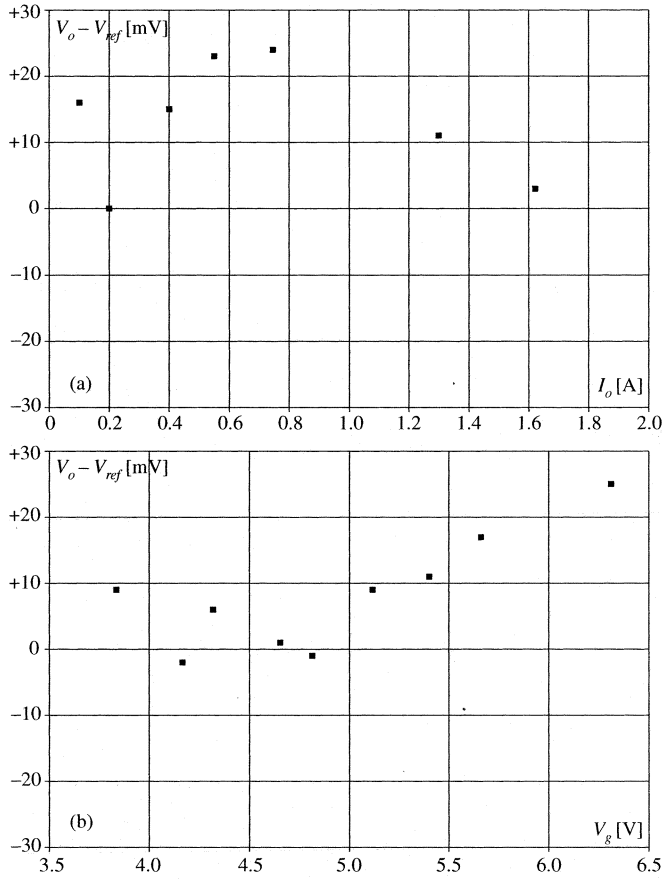

Fig. 16. Measured (a) load and (b) line voltage regulation in the closed-loop voltage regulator of Fig. 1.

of high-speed dynamic response, tight output voltage regulation and programmability without external passive components. The DPWM has 8-b resolution and generates the switching frequency of 1 MHz, and a system clock frequency of 8 MHz. The delay-line A/D converter has 1 MHz sampling rate, a 50 mV resolution, high noise immunity, and a small-size, low-power implementation based on digital logic gates without the need for precision analog components (other than a bandgap reference). The control law is implemented in a small-area, low-power compensator with look-up tables. The table entries are programmable so that the control law can be redesigned for various converter configurations and parameters without the need for external passive components. The complete chip design is based in hardware description language (HDL), and takes advantage of modern tools for digital ASIC design.

The controller architecture and the implementation techniques are experimentally verified on a prototype IC that takes less than 1 mm^2 of silicon area in a standard 0.5 μ digital CMOS process and operates at switching frequency 1 MHz.

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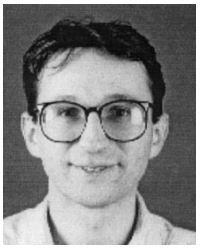

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