Self-Tuning Digitally Controlled Low-Harmonic Rectifier Having Fast Dynamic Response

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***Abstract*—This paper describes a completely digitally controlled high-performance low-harmonic rectifier. It is shown that the dynamics of the outer voltage loop can be significantly improved using a self-tuning digital comb filter. Low input current harmonics and fast voltage transient responses are experimentally verified on a 200 W universal-input boost rectifier operating at the switching frequency of 200 kHz.**

***Index Terms*—Digital control, PFC, STCF.**

I. Introduction

A TYPICAL low-harmonic rectifier [i.e., power factor corrector (PFC)] based on a boost converter is shown in Fig. 1. The current loop is designed so that the converter input current follows the waveform of the input voltage. In the ideal case these two waveforms have the same waveshape and are in phase: thus the rectifier presents a resistive load to the system. The outer loop regulates the voltage across the energy-storage capacitor. This voltage always has ripple at even harmonics of the line frequency f_L. To maintain low input current harmonics, the output $u(t)$ of the voltage regulator must not have significant line frequency harmonics [1]. Consequently, the bandwidth of the voltage loop in conventional designs is usually limited to frequencies (typically 10–20 Hz) significantly lower than the line frequency.

Analog controllers based on dedicated PFC control ICs that implement average current-mode or other control techniques are readily available and used in practice. More recently, partially or completely digital controllers based on microcontroller or DSP systems have been proposed for PFC applications. A controller that uses an analog compensator in the current loop and an adaptive digital compensator for the voltage regulation is described in [2]. A completely digitally controlled PFC rectifier operating at 20 kHz and implemented using a relatively simple hardware is presented in [3]. A PFC system with digital implementation of both current and voltage control loops, and an improved sampling scheme that avoids errors due to switching noise is presented in [4]. In this case, the converter operates at 33 kHz. Another example of a completely digitally controlled power factor rectifier circuit is given in [5]. This converter operates at 50 kHz and uses a high-resolution digital pulse width modulator.

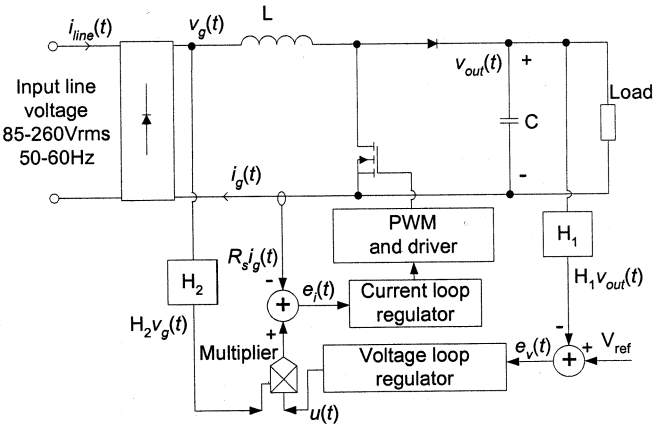

Fig. 1. Low-harmonic PFC rectifier based on a boost converter.

In Section II of this paper we present design of a high-performance, completely digitally controlled PFC rectifier capable of operating at high switching frequencies comparable to the switching frequencies commonly used in conventional designs based on analog controllers (100 KHz or more). The design is based on the use of a low-resolution digital pulse width modulator and an improved current sampling method. The second objective in this paper is to show how the same digital controller hardware can also be used to implement a wide-bandwidth voltage loop.

Several methods for improvement of the voltage loop bandwidth are conceptually described in [6], [7]. Practical implementation of an analog controller that provides wider bandwidth of the voltage loop is presented in [8]. The method is based on active ripple cancellation with a fast controller that has variable gain. A method based on a phase locked loop (PLL) in the system is described in [9]. In these cases, to tune the controllers and precisely adjust the gain, the authors used measurement of the output current. A technique for ripple cancellation that does not require sensing of the load current and has a simple implementation is presented in [10]. However, in this method, it is assumed that the output capacitor value and the converter efficiency are known.

In Section III, we present a new method for elimination of the ripple component from the voltage loop. Significant improvement of the output voltage transient response is obtained by implementation of a self-tuning digital comb filter (STCF) in the feedback loop. This relatively simple method does not require load current measurements, and is capable of universal-input

Manuscript received February 1, 2002; revised September 24, 2002. This work was supported by Philips Research through Colorado Power Electronics Center (CoPEC). Recommended by Associate Editor S. B. Leeb.

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Digital Object Identifier 10.1109/TPEL.2002.807141

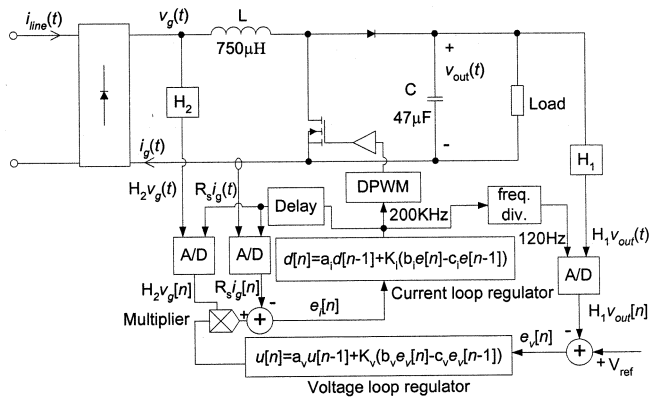

Fig. 2. Completely digitally controlled low-harmonic rectifier.

operation with automatic tuning for operation in 50 Hz or 60 Hz power systems.

Experimental results obtained on a 200 W, 200 KHz boost PFC prototype with the self-tuning digital controller resulting in high-performance current and voltage loops are given in Section IV.

II. Digital PFC Controller

Fig. 2 shows a block diagram of the complete digital controller for a 200 W boost-based PFC operating in continuous conduction mode at the switching frequency of $f_s = 1/T_s = 200$ kHz. The prototype is designed for universal input (ac line voltage between 85 Vrms and 260 Vrms) and the dc output voltage is regulated at 385 V.

A. Selection of the Switching Frequency and Resolution of the Digital Pulse Width Modulator

In the design of digital controllers for switching converters, a trade off exists between resolution of the digital pulse width modulator (DPWM) and the operating frequency. To allow smaller components and faster control, it is desired to operate the converter at higher switching frequency. As the switching frequency increases, the resolution of the conventional, counter-based DPWM decreases [11]. In dc–dc voltage regulators, limited resolution of the DPWM can result in undesirable "limit-cycle" oscillations [12], [13]. In PFC applications, the current reference is not a constant value. The time-varying current reference serves as an inherent "dither" that tends to reduce the possibility of limit-cycle oscillations and allows the use of a lower-resolution DPWM.

In our experimental prototype, the DPWM resolution is only 6 b, which allows operation at the switching frequency of 200 KHz using the Analog Devices DSP system ADMC-401 [11]. Furthermore, 8-b fixed-point arithmetic is used in the computational unit and 8-b analog-to-digital converters are applied; these choices contribute to the objective of implementing a high-performance PFC using relatively modest hardware configuration.

B. Selection of the Sampling Instants

The input current and the input voltage are sampled at the switching frequency. To avoid sampling the noise around switching transitions [4], and to obtain values approximately equal to the average of the input current during one switching cycle, the sampling instants are selected using an adjustable delay t_D from the beginning of a switching period at the time when the power switch is turned on. This delay depends on the current discrete value of the duty cycle $d[n]$ as

$$t_D = \frac{d[n]}{2} \cdot T_s \qquad \text{if } d[n] \geq 0.5$$

and

$$t_D = \frac{1+d[n]}{2} \cdot T_s \qquad \text{if } d[n] < 0.5. \tag{1}$$

As a result, the sampling occurs in the middle of the switch on-time if the current duty cycle is greater than 0.5, or in the middle of the switch off time if the current duty cycle is lower than 0.5.

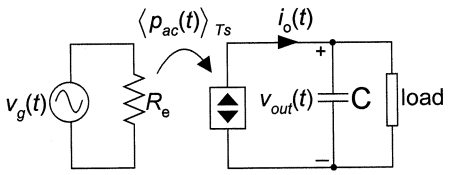

Fig. 3. Equivalent circuit of the ideal low-harmonic rectifier.

C. Current Loop Regulator Design

To find the dependence of the input current on the control variable (the duty cycle $d(t)$ variation), the averaged model [14] is employed. This model gives the control-to-input-current $i_g(t)$ transfer function as

$$\frac{\hat{i}_g(s)}{\hat{d}(s)} = \frac{V}{sL} \tag{2}$$

where V is the dc output voltage.

The current loop regulator design is based on digital redesign, using the pole-zero matched transformation technique [15]. A high switching (and current sampling) frequency in this case offers an additional advantage of simple implementation of the high-bandwidth current loop using a low-resolution computational unit [15], [16]. The limitations caused by sampling and processing delay are insignificant because of the high sampling frequency. The bandwidth of the current loop is approximately 20 kHz.

D. Design of a Low-Bandwidth Voltage Loop

The current loop regulator forces the input current to follow the input voltage wave-shape, and as a result the input port of the rectifier behaves as an emulated resistor R_e. The power apparently "consumed" by this emulated resistor is transferred to the rectifier dc output. Based on this, the equivalent model of the ideal rectifier is derived and illustrated in Fig. 3 [1], [14].

In this averaged model, the output port is represented by a controlled power source. If the input voltage is sinusoidal, the instantaneous power delivered to the power source $p_{ac}(t)$ is

$$p_{ac}(t) = \frac{2V_{g,rms}^2}{R_e}\sin^2(\omega_L t) = \frac{V_{g,rms}^2}{R_e}(1-\cos(2\omega_L t)). \tag{3}$$

As a result, the voltage across the output energy-storage capacitor must have ripple at $2f_L$, where f_L is the line frequency. To regulate the output voltage, a voltage feedback loop is needed. This feedback cannot attempt to remove the capacitor voltage ripple at the second harmonic of the line frequency; the capacitor must be allowed to store and release energy as necessary to interface the pulsating power of the single-phase ac input to the constant power drawn by the load. Removal of the second-harmonic voltage through feedback would cause distortion of the reference for the input current signal, and would consequently result in significant distortion of the ac line current.

For design of the digital voltage loop controller shown in Fig. 2, the approach based on sampling the output voltage at twice the line frequency can be used [6], [7]. Sampling at this frequency provides filtering of the second harmonic component. However, this low sampling frequency also limits the bandwidth of the voltage loop to less than the ac line frequency.

The low frequency model, based on averaging over one half of the line period, results in the following control-to-output transfer function [14]

$$\frac{\hat{v}_{out}(s)}{\hat{u}(s)} = \frac{V_{out}}{2 \cdot U \cdot H} \frac{1}{1 + sC\frac{R_{out}}{2}} \tag{4}$$

where, $u(t)$ is the output of the voltage regulator, and U is its steady-state value. Using the digital redesign method, a slow PI regulator that provides 20 Hz bandwidth is designed.

In the experimental system based on the diagram shown in Fig. 2, the measured THD of the input current is below 3%, and essentially unity power factor over the universal input range (85–260 $V_{\rm rms}$) is obtained. It is worth noting that the measured performance of this completely digitally controlled PFC equals or exceeds performance of standard analog implementations based on averaged current control.

III. Digital Controller With Improved Output Voltage Dynamic Response

Because of the low bandwidth of the output voltage feedback loop, components within the rectifier and a downstream converter must be designed to handle substantial transients in the capacitor voltage induced by load current or ac line voltage transients. Voltage dips can cause loss of regulation or reduced hold up time in the downstream converters, while over-voltages require increased voltage ratings of the energy storage capacitor and other elements. These issues require that conventional designs operate over an increased dynamic range, leading to increased cost and reduced efficiency.

A faster voltage loop would provide smaller variations of the output voltage, and consequently better optimization of the design of the low-harmonic rectifier and the converter stages supplied from the rectifier output. In this section, we show how these benefits can be realized using a self-tuning, digital comb filter that is capable of "recognizing" the system frequency, and automatically adjusting the parameters to maintain optimal characteristics. The filter is implemented in software, without any changes in the hardware configuration of the prototype PFC system.

A. Digital Comb Filter

The idea of using a notch filter to eliminate the second harmonic component from the output voltage loop is discussed in [6], [7]. A practical implementation with a digital notch filter is described in [17], showing that the bandwidth of the voltage loop can be expanded above $2f_L$. However, the 4th and higher harmonics of the input voltage are still present, limiting the achievable outer voltage loop bandwidth. In addition, any line voltage harmonics may result in the output voltage harmonics that cannot be eliminated using a fixed-frequency notch filter.

In this section we introduce a digital comb filter to eliminate higher-order harmonics and open the possibility of further expanding the bandwidth of the voltage loop. Ideally, a comb filter has infinite attenuation at the notch frequencies (which are multiples of the center frequency), unity gain at all other frequencies, and no effects on the phase of the signal. Clearly, these characteristics cannot be approached using analog implementation, but a practical digital implementation is quite feasible, as we show in this section.

The discrete transfer function of a conventional digital comb filter is given by [18]

$$H(z) = \frac{1}{M} \frac{1 - z^{-M}}{1 - z^{-1}}. \tag{5}$$

For example, the filter's magnitude and phase characteristics for $M = 40$ and the voltage sampling frequency $f_{vs} = 4.8$ kHz are given in Fig. 4. It can be seen that the filter has zeros at the frequencies

$$f_{zk} = \frac{f_{vs}}{M} \cdot k = f_c \cdot k \tag{6}$$

where, $k = 1, 2, \ldots, M$.

The zeros can be used to provide the desired attenuation at the even harmonics of the line frequency. However, other aspects of the comb filter's magnitude and phase response do not meet the stated requirements for use in the PFC voltage loop.

B. Modified Comb Filter

Introduction of "weaker" poles p_k at the frequencies of the zeros can modify the comb filter. The z-plane, pole-zero pattern of the modified filter for the case $M = 4$ is shown in Fig. 5.

In the modified comb filter, in addition to the zeros placed at the unit circle in the complex z-plane

$$z_k = e^{j2\pi(k/Mf_{vs})}, \qquad k = 1, 2, \ldots, M \tag{7}$$

an additional set of poles is placed at

$$p_k = r \cdot e^{j2\pi(k/Mf_{vs})}, \qquad k = 1, 2, \ldots, M \tag{8}$$

where, $r \in [0 \div 1)$.

The discrete transfer function of the modified comb filter now can be written as

$$\begin{aligned} H_{mc}(z) &= \frac{1 - z^{-M}}{1 - z^{-1}} \frac{1 - (r \cdot z)^{-1}}{1 - (r \cdot z)^{-M}} \\ &= \frac{(z - z_1) \cdot (z - z_2) \cdots (z - z_k)}{(z - p_1) \cdot (z - p_2) \cdots (z - p_k)}. \end{aligned} \tag{9}$$

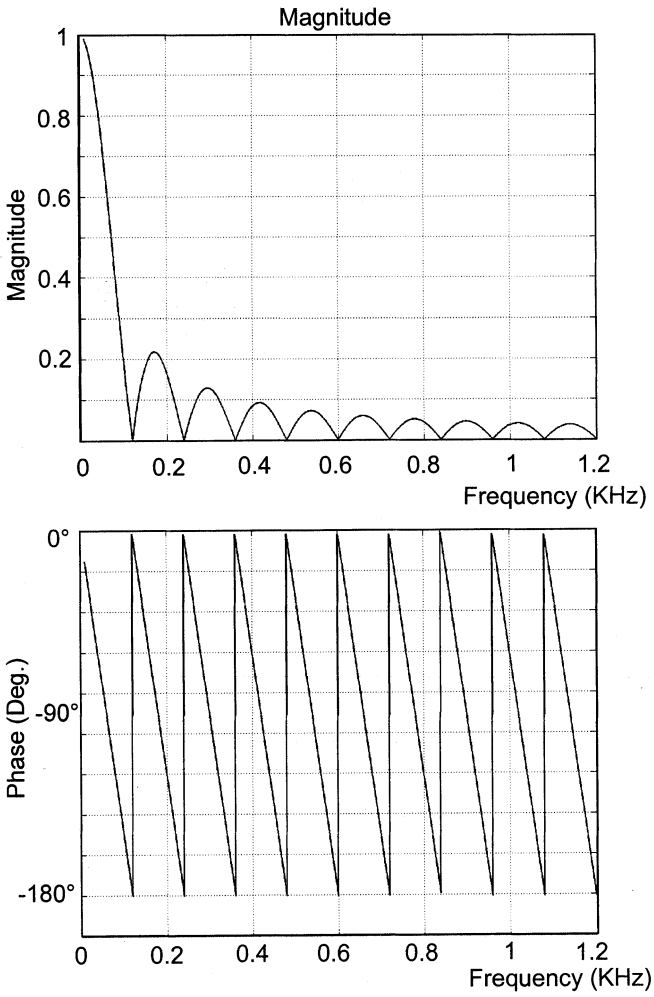

Fig. 4. Magnitude (top) and phase characteristic (bottom) of the conventional digital comb filter.

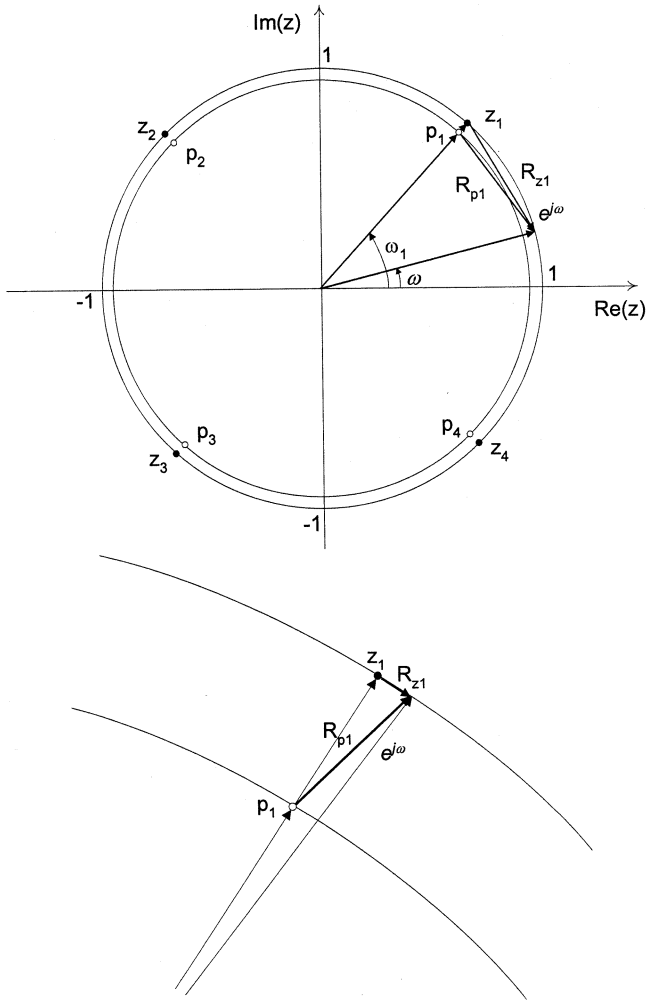

Fig. 5. Z-plane, pole-zero pattern of the modified comb filter. Top: position of the vectors for the case when the input signal frequency is far from the frequency of a pole/zero $\omega \neq \omega_k$. Bottom: a magnified section of the unit circle around the pole/zero for the case when $\omega \approx \omega_1$.

The frequency response of the filter is obtained by substituting z with $e^{j\omega}$, where $\omega = 2\pi f/f_{vs}$ and f is the signal frequency

$$H_{mc}(\omega) = \frac{(e^{j\omega}-z_1)(e^{j\omega}-z_2)\cdots(e^{j\omega}-z_{M+1})}{(e^{j\omega}-p_1)(e^{j\omega}-p_2)\cdots(e^{j\omega}-p_{M+1})} = \frac{|r_{z1}|e^{j\varphi 1}|r_{z2}|e^{j\varphi 2}\cdots|r_{zk}|e^{j\varphi(M+1)}}{|r_{p1}|e^{j\gamma 1}|r_{p2}|e^{j\gamma 2}\cdots|r_{pk}|e^{j\gamma(M+1)}} = \frac{R_{z1}R_{z2}\cdots R_{z(M+1)}}{R_{p1}R_{p2}\cdots R_{p(M+1)}}. \quad (10)$$

Here, the vectors R_{zi} and R_{pi} are the differences between the vectors z_i, p_i and the vector $e^{j\omega}$, respectively.

Let us examine the case when the coefficient r in (9) is close to one. From Fig. 5 it can be seen that when the frequency of the input signal is far from one of the pole/zero frequencies, the vectors R_{zi} and R_{pi} have approximately the same magnitude and phase. Consequently, the magnitude and phase of the input signal remain almost unchanged. From Fig. 5, we can also see that for frequencies close to one of the pole/zero frequencies ω_i the dominant factor in the frequency response becomes the ratio of R_{zi} and R_{pi}. When the frequency of the input signal is equal to one of the pole/zero frequencies, the input signal is completely attenuated.

Fig. 6 shows the magnitude and phase responses of the digital comb filter for two different values of the factor r. It can be seen that the characteristics become closer to ideal as the factor r approaches one. In the digital implementation with fixed-point arithmetic, the maximum value of the factor r is limited by the resolution of the computational unit. Also, in the design of this filter there is a tradeoff between the value of r and the order M of the filter. The higher order of the filter requires more memory, but because of the exponential decrease of the factor r^M (9), the filter can be implemented using a lower-resolution computational unit. The parameter r of the comb filter can be selected to obtain large attenuation at the line frequency and at frequencies in close vicinity of the line frequency. This allows strong attenuation of the second harmonic even in the case when the line frequency is not exactly 50 Hz or 60 Hz, but close to one of the two standard frequencies.

C. Voltage Loop With the Modified Comb Filter

Fig. 7 shows the equivalent circuit of a low-harmonic rectifier that incorporates the modified comb filter in the voltage

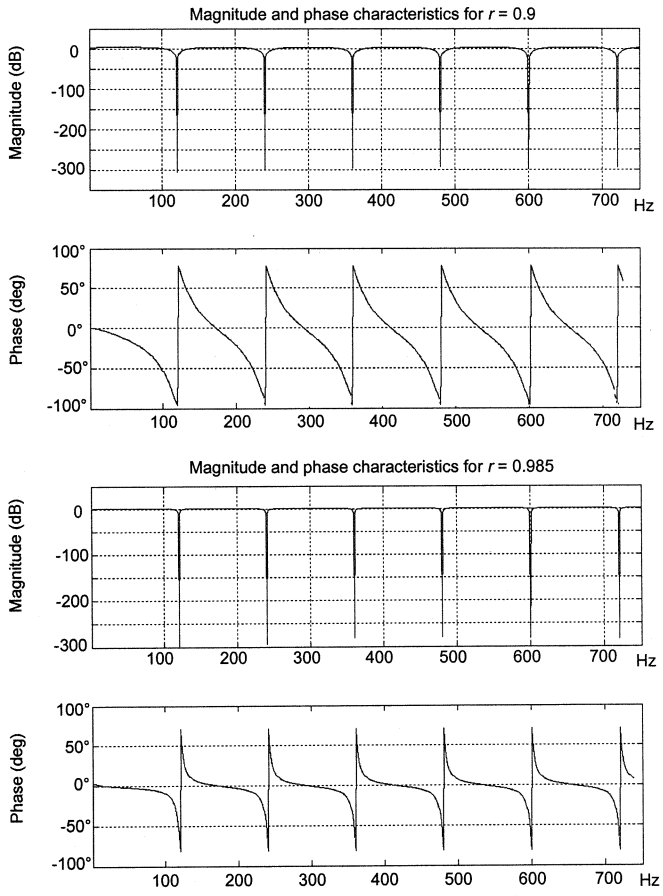

Fig. 6. Magnitude and phase characteristics of the modified comb filter for $r = 0.9$ (top) and for $r = 0.985$ (bottom).

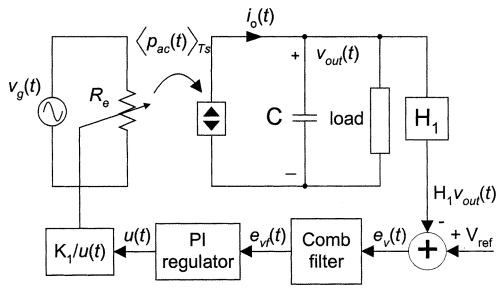

Fig. 7. Equivalent circuit of a low-harmonic rectifier with the modified comb filter in the voltage loop.

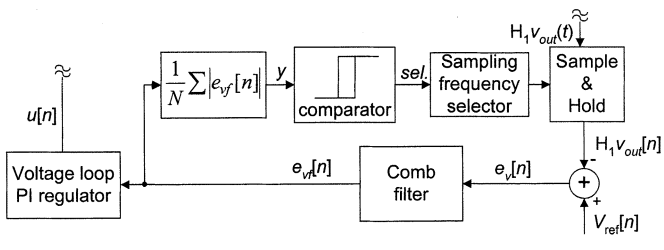

Fig. 8. Block-diagram of the self-tuning system with the comb filter (STCF).

loop. The attenuated output voltage is compared with a reference voltage to generate the error signal

$$e_v(t) = V_{ref} - H_1 V_{out}. \tag{11}$$

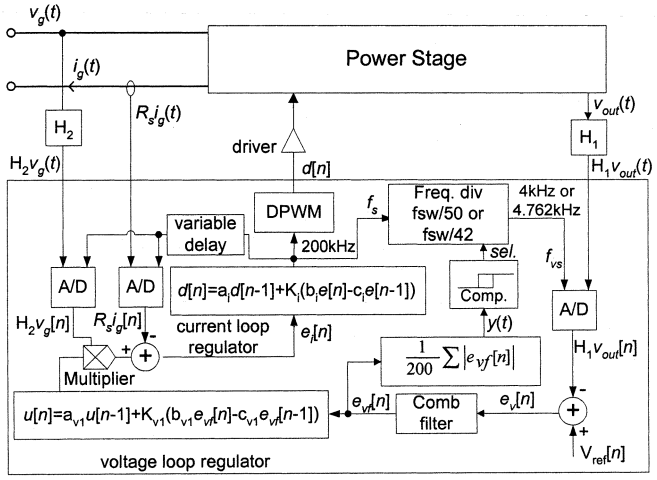

Fig. 9. Block diagram of the prototype system with the self-tuning comb filter in the voltage loop.

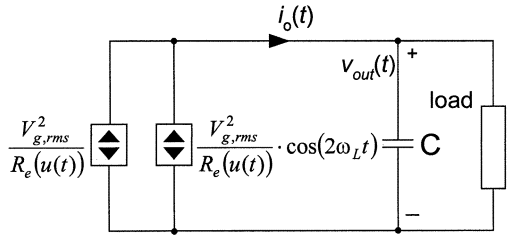

Fig. 10. Equivalent circuit of power stage for the design of a high-bandwidth voltage loop.

The output voltage $v_{out}(t)$ can be expressed as the sum of the voltage ripple at the second harmonic of the line frequency and the remaining component $v_1(t)$

$$v_{out}(t) \approx v_1(t) + \frac{P_{load}}{2\omega C V_{C,\,rms}} \sin(2\omega_L t + \varphi). \tag{12}$$

For the case when the center frequency of the comb filter is equal to the second harmonic of the line frequency, the component at the frequency of $2\omega_L$ is eliminated and the signal $e_{vf}(t)$ (filtered voltage error signal) contains only the difference between the reference voltage and $H_1 v_1(t)$

$$e_{vf}(t) = V_{ref} - H_1 v_1(t). \tag{13}$$

Equation (13) shows that the emulated resistance R_e is not affected by the second harmonic of the line frequency. Therefore, the bandwidth of the voltage loop can be expanded to frequencies higher than $2f_L$.

D. Self-Tuning Comb Filter (STCF)

A universal-input rectifier should be able to maintain performance not only over a range of line voltages (85–260 $V_{\rm rms}$) but also for both standard line frequencies (50 Hz and 60 Hz), including small frequency variations allowed by standards. To meet these criteria, the PFC with the modified comb filter should be able to "recognize" the line frequency and adjusts the frequency of the "notches" to match the even harmonic of the line frequency. A self-tuning realization capable of performing this adjustment automatically is shown in Fig. 8. All components in this block diagram are realized in software.

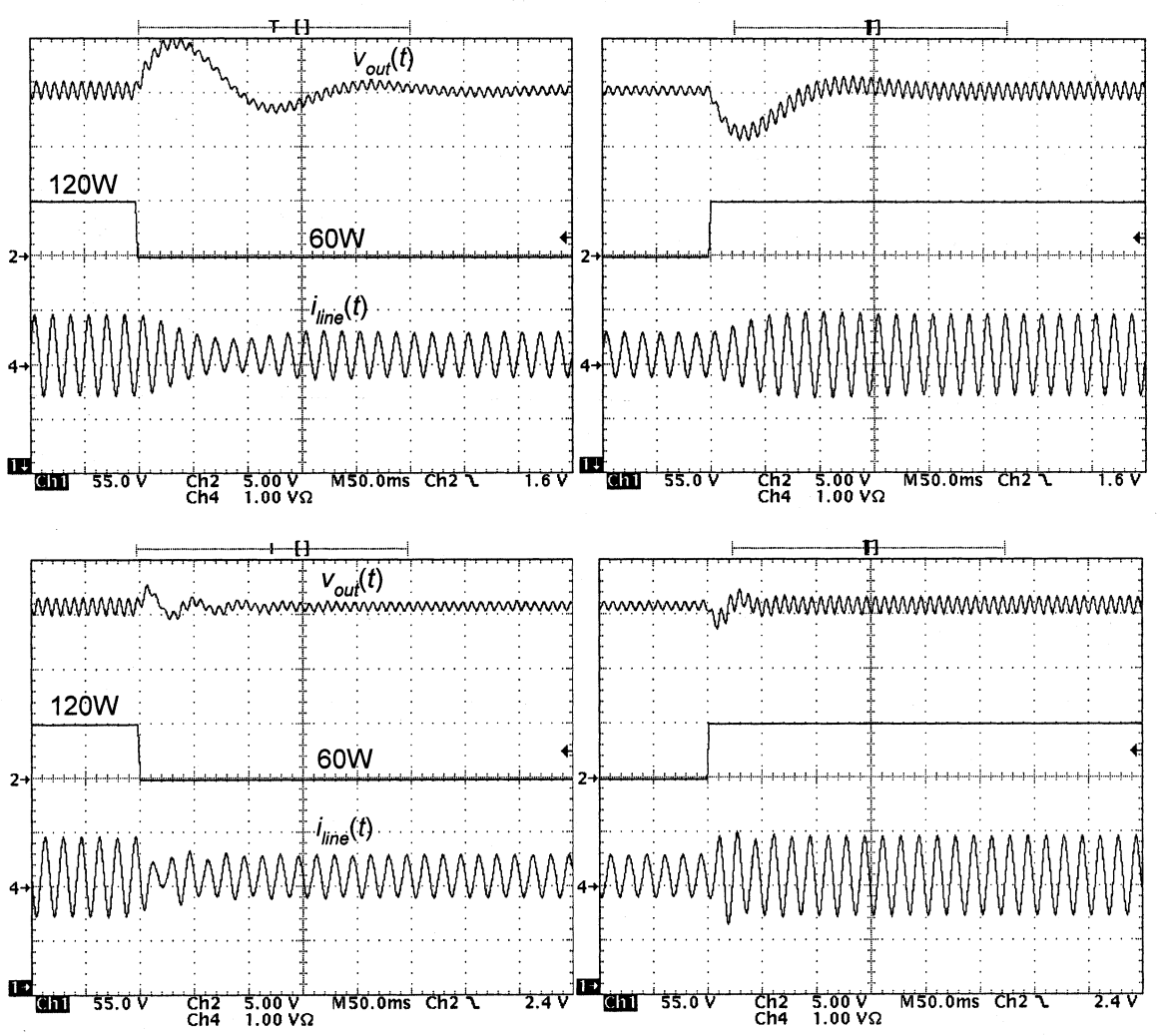

Fig. 11. Transient responses for the load changes from 120 W to 60 W and from 60 W to 120 W. Ch1—Output voltage $v_{out}(t)$, Ch2—Load change, Ch4—Line current $i_{line}(t)$. Top: with standard voltage loop having the crossover frequency of 20 Hz. Bottom: with the fast voltage loop and the digital comb filter.

From (6), it can be seen that the frequencies of the zeros (and the poles) of the comb filter are linearly proportional to the sampling frequency.

In the implementation of Fig. 8, the sampling frequency can be one of two possible values: for one of the two frequencies the filter notches are at the multiples of 100 Hz, for the other sampling frequency the notches are the multiples of 120 Hz. The operation of the system designed to automatically select the proper sampling rate is as follows: suppose that the line frequency is 60 Hz, but the sampling frequency is such that the comb notches are at the multiples of 100 Hz (instead of 120 Hz). In this case, the output signal $e_{vf}[n]$ of the comb filter includes significant components at the multiples of 120 Hz. The signal $e_{vf}[n]$ is the input to the block that performs rectification and averaging over a number (K) of line periods. The output y of this block is found as

$$y = \frac{1}{N}\sum_{1}^{N}|e_{vf}[n]| \approx \frac{1}{KT_L}\int_{0}^{KT_L}|e_{vf}(t)|\,dt. \qquad (14)$$

A comparator detects the higher value of y, and initiates a change in the sampling frequency to the new value such that the comb notches become multiples of 120 Hz. Note that the change in the sampling rate automatically results in the changes of the filter and the regulator parameters appropriate for the line frequency. Once the sampling rate is changed so that the filter notches match the multiples of 120 Hz, the output y of the rectification/averaging block becomes low and the sampling frequency remains unchanged. The number of samples N (the number of periods K) taken in averaging is selected to ensure that transient output voltage variations do not cause spurious changes in the sampling frequency. It should be noted that for proper operation of the STCF the voltage loop regulator must include integral action that results in zero steady-state (dc) error.

E. Self-Tuning Comb Filter Implementation

To design the filter defined by (9), the output voltage sampling frequencies and the factor r are selected based on the following objectives: to significantly increase the voltage-loop bandwidth, to provide strong attenuation at the $2f_L \pm 2$ Hz frequency, and to perform all processing using 8-b fixed-point arithmetic with relatively low memory requirements. For the prototype design example, the following choices were made:

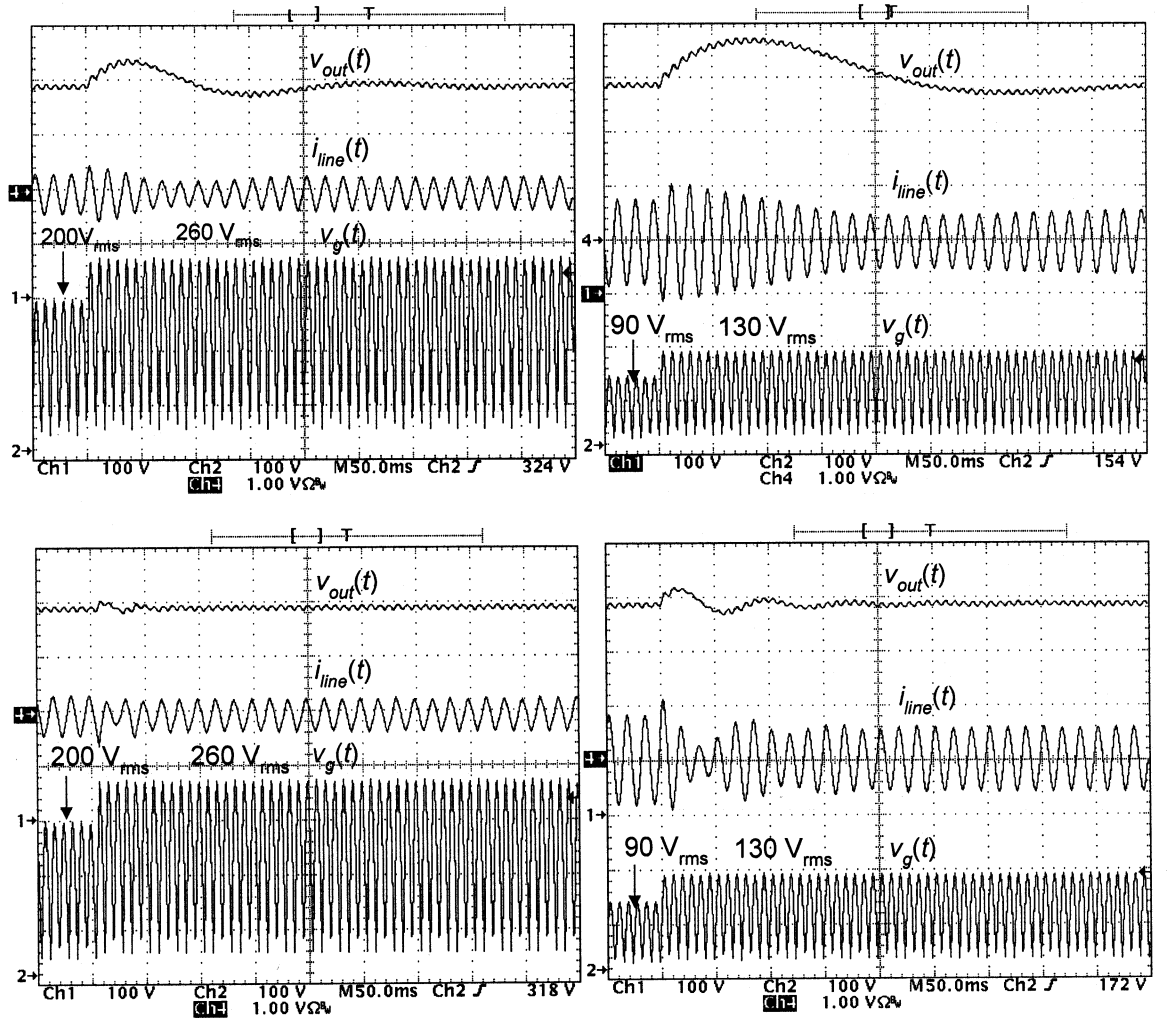

Fig. 12. Transient responses to the change of the input line voltage. Ch1—Output voltage $v_{out}(t)$, Ch2—Rectified input line voltage $v_g(t)$, Ch4—Line current $i_{line}(t)$. Top: with standard voltage loop having the crossover frequency of 20 Hz. Bottom: with the fast voltage loop and the digital comb filter.

the parameter M is 40, the factor r is 0.985, while the sampling frequencies are 4 kHz and 4.8 kHz, corresponding to the filter center frequencies of 100 and 120 Hz, respectively.

The resulting comb filter transfer function is given by

$$H(z) = \frac{1 - 0.985 \cdot z^{-1} - z^{-40} + 0.985 \cdot z^{-41}}{1 - z^{-1} - 0.546 \cdot z^{-40} + 0.546 \cdot z^{-41}}. \quad (15)$$

Implementation of this filter structure requires eighty-two 8-b memory locations to store the previous values of the input and output signals.

The complete system prototype is shown in Fig. 9. This prototype is formed from the system shown in Fig. 2 by adding the STCF in the voltage loop regulator software. To obtain two sampling frequencies the switching frequency signal of 200 kHz is divided either by 50 or 42 of, resulting in 4 kHz and 4.762 kHz. The switching frequency signal is derived from a 26 MHz crystal oscillator used as the system clock for the DSP. The frequency tolerances of this signal are insignificant. Averaging is performed over $N = 200$ sampling cycles, which corresponds to $K = 2.5$ line periods. In addition, compared to the design described in Section II, the parameters of the PI regulator are modified in order to achieve a higher bandwidth for the voltage loop.

F. Design of a High-Bandwidth Voltage Loop

The design and stability analysis of the voltage loop are complicated by two factors:

1) presence of the comb filter in the loop
2) the nonlinear, time-varying nature of the power stage model as shown in Fig. 10.

The instantaneous powers of both power sources in the model depend on the time-varying value $u(t)$, which controls the emulated resistance R_e.

In the experimental prototype, a simple PI regulator was designed based on the "frozen coefficients" method [19]. The regulator is designed to provide bandwidth above $2f_L$ for the worst case in the circuit, at the moment when the instantaneous input power has the maximum value. Stability and achieved performance are experimentally verified as documented in Section IV.

IV. Experimental Results

The experimental system was designed around the Analog Devices ADMC-401 DSP Evaluation Board [11], which offers more than sufficient performance for implementation of the controllers described in Sections II and III. In the prototype realiza-

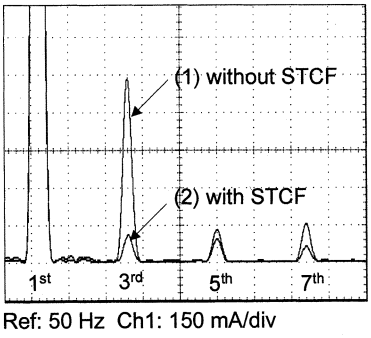

Fig. 13. Harmonic content (first through seventh harmonics) of the input current with wide-bandwidth voltage regulator: 1) without the self-tuning digital comb filter (STCF), THD $>$ 20% and 2) with the STCF, THD $<$ 5%.

tion, the A/D resolution was purposely limited to 8 b (although the system has 12-b A/D converters) and all computations were performed in 8-b fixed-point arithmetic (although the system is 16 b). The objectives were to show that it would be possible to realize the system using even simpler hardware.

Fig. 11 shows step load (between 60 W and 120 W) transient responses measured for two cases: with a standard, slow voltage loop as described in Section II, and with the comb filter and the faster voltage regulator as described Section III. Fig. 12 shows responses to the input line voltage change for the prototypes with and without self-tuning comb filter.

It can be observed that the overshoots in the standard low-bandwidth implementation cause additional voltage stresses on the capacitor. Moreover, in the case of a light-to-heavy load change, the voltage dip is significant so that the stages that follow must be designed to avoid possible loss of regulation. Also, for a high-line input, the peak of the input line voltage may exceed the output voltage during the dip, causing loss of regulation and peaking in the input current. To cope with these problems, the standard solution is to operate the output at an increased dc voltage, to use larger filter capacitance, and/or to over-design the downstream converters. The waveforms obtained with the STCF implementation show significantly improved dynamic responses which enable a less conservative design of the PFC rectifier and the downstream stage.

Fig. 13 compares the input line current harmonics for the case when the wide-bandwidth voltage loop was applied in the systems with and without the digital comb filter. Without the comb filter, the wide-bandwidth voltage regulator results in significant input current harmonic distortion (THD of more than 20%), while with the comb filter the input current THD is about 4.3%.

Experimental results in Fig. 14 show the error signal at the output of the self-tuning comb filter of Fig. 9 for a change of the line frequency from 50 Hz to 60 Hz. After the frequency change occurs, second harmonic component can be observed at the output $e_{vf}(t)$ of the filter. The condition characterized with the presence of the second harmonic continues for several line cycles, until the self-tuning structure "recognizes" the new state, asserts the high level of the signal y at the output of the rectifying/averaging block, triggers the comparator signal $sel(t)$, and adjusts the filter. Once the proper sampling frequency is selected, the second harmonic from the filtered error signal is

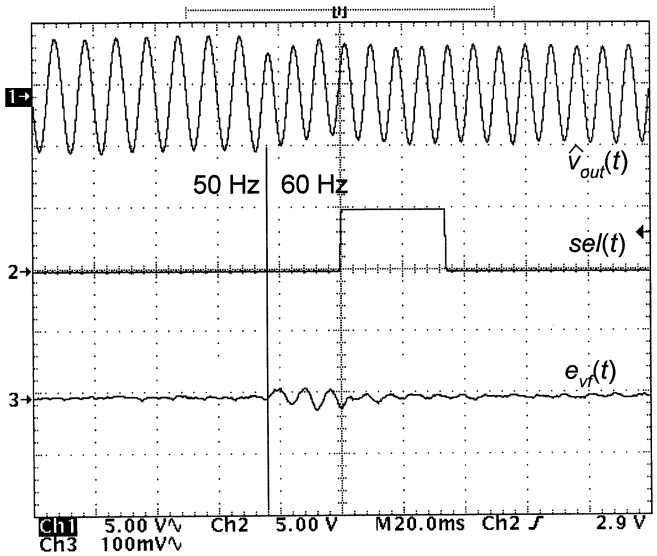

Fig. 14. Response of the self-tuning comb filter for the 50 Hz to 60 Hz line frequency change: Ch.1—output voltage capacitor ripple $v_{out}(t)$; Ch.2—output of the comparator $sel(t)$; Ch.3—filtered voltage error signal $e_{vf}(t)$.

eliminated, causing the low value of $sel(t)$ and the sampling frequency remains the same as long as the line frequency does not change.

To verify operation of the self-tuning comb filter we also performed measurements of the input current THD for different line frequencies. For all line frequencies in the ranges: 50 ± 2 Hz and 60 ± 2 Hz, the current THD is lower than 4.3%. For frequencies between 53 Hz and 57 Hz, the measured THD is between 4.3% and 10%. As expected, significant current distortion was observed outside the ranges of interest, for frequencies lower than 46 Hz and higher than 64 Hz.

V. Conclusion

This paper describes design and implementation of high-quality low-harmonic rectifiers (i.e., power factor correctors, PFC) using relatively simple digital control hardware. First, a 200 W, 200 KHz completely digitally controlled boost PFC that matches or exceeds performance of standard analog implementations is demonstrated. Furthermore, it is shown how the output voltage dynamic response can be significantly improved by adding a self-tuning digital comb filter in the feedback loop. The addition of the filter is performed in software, without any change in hardware of the prototype PFC. This PFC system is capable of universal-input operation by adjusting automatically to the input line frequency. Much improved voltage-loop dynamic response enables a less conservative design of the PFC and the downstream converters by reducing the output voltage variations due to load or input voltage transients. The main results, including low current THD and fast transient responses are experimentally verified on the DSP-controlled boost rectifier.

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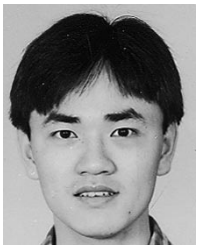

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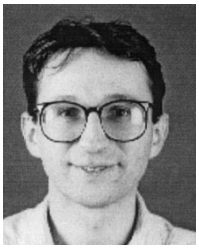

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