Dead-Zone Digital Controllers for Improved Dynamic Response of Low Harmonic Rectifiers

Aleksandar Prodić, *Member, IEEE*, Dragan Maksimović, *Member, IEEE*, and Robert W. Erickson, *Fellow, IEEE*

***Abstract*—This paper introduces a simple digital control method that enables fast regulation of the output voltage in low harmonic rectifiers with power factor correction (PFC). The method is based on the use of an insensitive region, i.e., "dead-zone," in analog-to-digital conversion, for elimination of the output capacitor voltage ripple in the feedback loop. The dead-zone can either be fixed and larger than the maximum ripple magnitude, or it can be dynamically adjusted in accordance with the output load. Simple implementations of these two dead-zone controllers are shown on an experimental completely digitally controlled 250-W boost PFC operating at 200-kHz switching frequency. The experimental results show that this control method results in low current harmonics and improved load transient responses, which are significantly faster than in low-harmonic rectifiers with conventional low-bandwidth voltage-loop controllers.**

***Index Terms*—Analog-to-digital conversion, low-bandwidth voltage-loop controllers, power factor correction (PFC).**

I. Introduction

DIGITAL control of switch mode power supplies (SMPS) is becoming increasingly common not only in high-power, low-frequency supplies, but also in low-to-medium power high-frequency applications, including dc/dc converters and single-phase low-harmonic rectifiers with power factor correction (PFC rectifiers, or PFCs).

Recent publications [1]–[16] demonstrate not only that completely digitally controlled experimental PFCs with performance comparable to state of the art analog implementations are feasible, but also that further enhancements of dynamic characteristics can be achieved through digital control [2]–[7]. Some of the reported experimental systems also include new interesting features such as multimode operations [6], [7], [13], simple paralleling [9], [10], or implementation of controllers with a smaller number of active and passive components [6], [11]. In addition, the digitally controlled PFCs have improved flexibility and programmability.

Although the advantages of digital control have been recognized, dedicated analog controllers are still dominant in single-phase PFCs, mostly due to a higher complexity and overall cost of digital systems. In order to successfully utilize advantages of digital control in practice, our focus is on system improvements without penalties in the system complexity or cost. With this goal in mind, in this paper we introduce a simple digital control method for dynamic response improvements in digitally controlled PFCs. In comparison with conventional solutions, the proposed method significantly improves dynamic responses using a simple hardware, which can result in less conservative design of the PFC power stage and a downstream dc/dc converter.

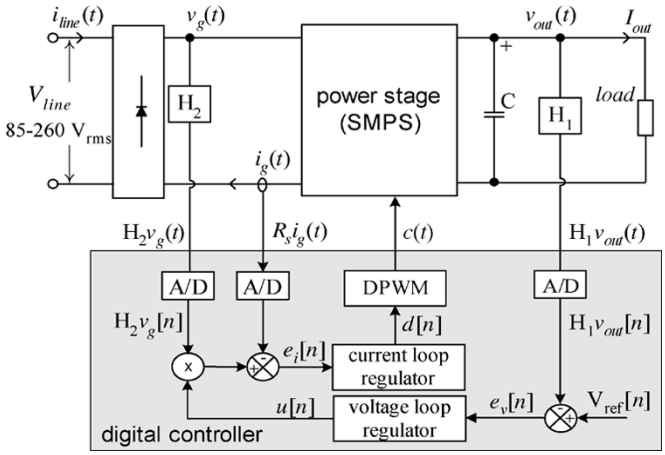

Fig. 1. Digitally controlled PFC rectifier.

Fig. 1 shows a block diagram of a digitally controlled PFC rectifier. The switching converter is controlled by two loops: an inner, current loop that forces the rectified input current $i_g(t)$ to follow the rectified input voltage waveform $v_g(t)$ according to:

$$i_g(t) = \frac{v_g(t)}{R_e} = kv_g(t) \tag{1}$$

and an outer voltage loop, which regulates the output voltage by changing the factor k, the ratio of the input voltage and the input current, i.e., the emulated resistance R_e.

In order to maintain a low distortion of the input current, the change of the emulated resistance must not be influenced by the output capacitor ripple at even harmonics of the line frequency [17], [18]. In conventional designs, the elimination of the even harmonics' influence is accomplished through a slow voltage loop [17], the bandwidth of which is usually 10–20 Hz. By closing the loop at a crossover frequency significantly lower than the frequency of the second line harmonic and by providing a strong attenuation at frequencies higher than the crossover, the emulated resistance is kept nearly constant during a line period. However, the dynamic response of the low-bandwidth

Manuscript received July 28, 2004; revised May 5, 2005. This work was presented in part at the IEEE Applied Power Electronics Conference (APEC'03), Miami, FL, February 2003. Recommended by Associate Editor P. Mattavelli.

A. Prodić is with the Laboratory for Low-Power Management and Integrated SMS, Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: prodic@power.ele.utoronto.ca).

D. Maksimović and R. W. Erickson are with the Colorado Power Electronics Center, Department of Electrical and Computer Engineering, University of Colorado, Boulder, CO 80309-0425 USA (e-mail: maksimov@colorado.edu; rwe@colorado.edu).

Digital Object Identifier 10.1109/TPEL.2005.861157

0885-8993/$20.00 © 2006 IEEE

voltage controller is poor and over-design of the power stage and a downstream dc/dc converter may be required to account for increased voltage overshoots and dips during transients.

A number of analog and digital methods for improvement of voltage loop characteristics that include ripple cancellation, filtering, and regulation band circuits have been proposed [2], [3], [7], [15], [19]–[23]. In the ripple cancellation techniques, an estimation of the output voltage ripple is performed and the estimated ripple is subtracted from the error signal of the voltage loop. The voltage loop controller presented in [21] uses a phase locked loop (PLL) as the ripple estimator. The magnitude of the ripple is estimated from the output current measurement, where it is assumed that the output capacitance is constant. A method for ripple cancellation that does not require the output current measurement and can be used in systems with constant output capacitance is introduced in [3]. A method that allows ripple cancellation even when the output capacitance varies is presented in [22]. Based on the output voltage and current measurements, the output capacitance is estimated and a variable gain of the voltage loop is adjusted to achieve effective ripple elimination.

Methods based on the use of analog or digital filters for ripple elimination [3], [7], [19], [20] do not require output current measurements. To effectively filter out the undesirable components from the voltage loop, a notch filter with a large Q factor and a well-tuned center frequency, which matches the frequency of the output capacitor ripple, is required. The filter characteristics should not change with temperature or aging. Moreover, in universal input applications, the filter should be able to "recognize" changes in the line frequency and accordingly adjust the center frequency. Because of these constraints, an analog notch filter implementation is not practical. Practical digital filter implementations have been presented [7], including a self-tuning comb filter (STCF) that automatically detects frequencies of the even harmonics and accordingly sets the center frequencies of the "notches" to eliminate the ripple.

In all of the above reviewed methods, additional analog or digital processing is required in order to improve the voltage loop dynamics. Relatively simple analog control methods based on an error amplifier that has a gain dependent on the amplitude of the input signal have been presented in [19], [20], [23]. In steady state, when the error is small (i.e., within a regulation band), the error-amplifier gain is zero (or small) and the output voltage ripple component does not significantly affect operation of the current loop. During transients, when the error is large (i.e., outside the regulation band), the gain of the error amplifier is increased to improve the response speed. The "dead-zone" digital controllers proposed in this paper are based on a similar idea. The implementation includes only a simple modification of the analog-to-digital converter characteristic and does not require any additional hardware or processing.

The paper is organized as follows: the control method based on a dead zone in analog to digital conversion is presented in Section II. Section III describes the voltage compensator design. An adaptive adjustment of the dead zone, which results in improved static regulation, is presented in Section IV. Experimental results obtained from a completely digitally controlled boost PFC prototype are presented in Section V.

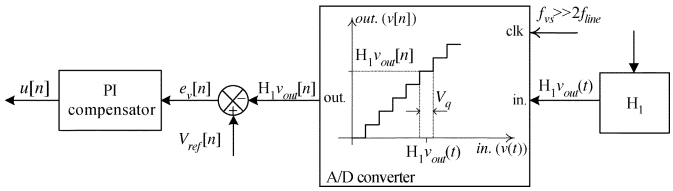

Fig. 2. Voltage loop regulator with a dead-zone controller.

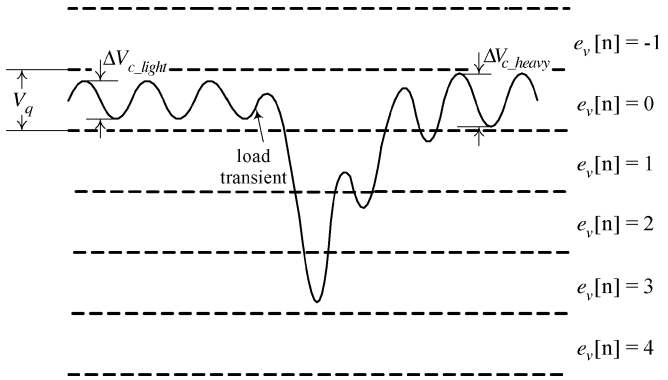

Fig. 3. Variation of the output voltage around the reference value during a load transient for the properly selected resolution of the analog-to-digital converter in a dead-zone controller.

II. Dead-Zone Control Method

In a properly operating PFC rectifier shown in Fig. 1, the difference between the instantaneous input power and the constant output load power $P_{\rm load}$ causes the output capacitor ripple at twice the line frequency $f_{\rm line}$. The peak-to-peak amplitude of this voltage ripple Δv_c is approximately [17]

$$\Delta v_c \approx \frac{P_{\rm load}}{2\omega_{\rm line} C V_{\rm out}} \tag{2}$$

where C is the output capacitance value, $V_{\rm out}$ is the dc output voltage and $\omega_{\rm line} = 2\pi f_{\rm line}$. The maximum value of this ripple is one of the design constrains that determines the value of the output capacitor. In the dead-zone control method, the maximum ripple amplitude is also used to set the resolution of the analog-to-digital converter for the output voltage sensing.

A description of operation of the dead-zone controller is given through the diagrams shown in Figs. 2 and 3. Fig. 2 shows a block diagram of the digital voltage loop controller. The attenuated output capacitor voltage $H_1 v_{\rm out}(t)$, which can be written as a sum of its dc value $H_1 V_{\rm out}$ and the ripple component $H_1 v_{\rm ripple}(t)$

$$H_1 v_{\rm out}(t) = H_1 V_{\rm out} + H_1 v_{\rm ripple}(t) \tag{3}$$

is converted into its digital equivalent $H_1 v_{\rm out}[n]$ using an analog-to-digital converter. The analog voltage is sampled and measured at each $T_s = 1/f_{vs}$ seconds, where the sampling frequency f_{vs} is significantly higher than twice the line frequency. The sampled and converted value $H_1 v_{\rm out}[n]$ is then compared with a digital reference value $V_{\rm ref}[n]$ and the resulting output voltage error signal $e_v[n]$ is processed by a digital PI compensator. The output of the voltage loop compensator $u[n]$ is multiplied by a digital value proportional to the input voltage $H_1 v_g[n]$ (see Fig. 1) resulting in the current loop reference.

From Fig. 2 it can be seen that the output of the analog-to-digital converter produces the same value at the output as long as the voltage variation around the mid-point of an A/D bin is smaller than $V_q/2$, where V_q is the quantization step of the analog-to-digital converter.

By using a PI regulator, which forces the average value of the error signal to be zero (i.e., operation of the A/D inside the "zero-error bin"), and an A/D with a relatively coarse resolution, the output voltage ripple can be eliminated from the voltage loop. This can be achieved if the quantization level around the reference voltage is larger than the attenuated worst-case peak-to-peak ripple $H_1\Delta v_{c\_\max}$

$$V_q > H_1 \cdot \Delta v_{c\_\max} \approx H_1 \cdot \frac{P_{\text{load\_max}}}{2\omega_{\text{line}} C V_{\text{out}}}. \tag{4}$$

The worst-case ripple is taken to be when the output power is at the maximum $P_{\text{load\_max}}$. Fig. 3 shows the output voltage ripple and the low-resolution A/D converter's quantization levels around the reference voltage in steady state and during a load transient, which causes a change of the output voltage.

In steady state, the voltage error $e_v[n]$ is zero and the output capacitor ripple does not affect operation of the voltage loop. During a transient, the output voltage is out of the zero-error bin, and the voltage loop compensator reacts in order to return the output voltage to regulation. In order to capture the moment when the transition from zero error range occurs and to react quickly to the load transient, the output voltage is sampled at the frequency significantly higher than the second harmonic frequency. With a proper selection of the operating point of the analog-to-digital converter and the attenuation factor H_1, the condition given by (4) can be easily satisfied.

In the approach illustrated by (4) and the block diagram of Fig. 2, the error in the dc output voltage regulation is smaller than the difference between the quantization step and the peak-to-peak amplitude of the capacitor voltage ripple. The regulation error is larger at light loads or with capacitive loads, when the actual output capacitor voltage ripple is smaller than the maximum ripple. In most cases, the maximum possible steady-state error V_q/H_1, which corresponds to the zero-ripple case, is acceptable. A modification of the dead-zone controller to improve the static voltage regulation is presented in Section IV.

III. Compensator Design

In order to design a voltage loop compensator we start from the block diagram shown in Fig. 4, which incorporates a large signal model of the PFC rectifier [17] and the voltage control loop. The input port of the PFC behaves as a lossless resistor, where the emulated resistance is controlled by the output of the voltage loop compensator. The power absorbed by the resistor is transferred to the power source and its averaged value over the switching cycle T_s is given by

$$\langle p_{\text{ac}}(t)\rangle_{T_s} = \frac{V_{\text{line}}^2}{R_e} \cdot \sin^2(\omega t) = \frac{V_{\text{line}}^2}{R_e}\left(1 - \cos(2\omega t)\right) \tag{5}$$

where V_{line} is the amplitude of the input line voltage. It can be seen that this is a nonlinear, time-varying system. The gain

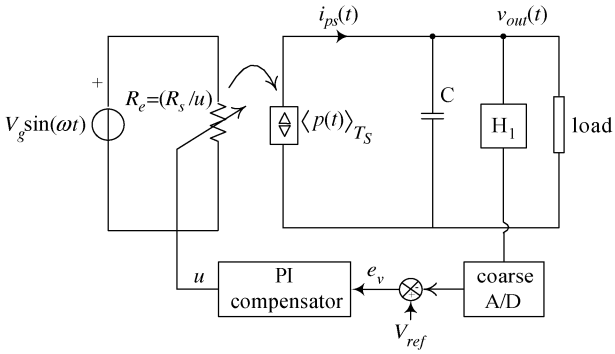

Fig. 4. Large-signal model of the voltage loop with the dead-zone controller.

of the system varies over time as the line voltage changes and the dependence between the output voltage and the control signal $u(t)$ is nonlinear. Moreover, the coarse resolution of the analog-to-digital converter brings additional nonlinearity in the closed loop system.

The compensator design is performed in three steps. First, the model of the system is manipulated to obtain a linear dependence between the control variable $u(t)$ and the output voltage. Then, the "frozen coefficient" method [24] is used to linearize the resulting time-varying system, and finally a digital PI compensator that provides a fast system response is designed.

A. Circuit Manipulation

A transformed large-signal model of the PFC shown in Fig. 5(a) is obtained by replacing the power source of the system in Fig. 4 with a controlled current source. The output current of the controlled source is

$$\langle i_{PS}(t)\rangle_{T_S} = \frac{\langle p(t)\rangle_{Ts}}{V_{\text{out}}}$$
$$\langle i_{PS}(t)\rangle_{T_S} = \frac{V_{\text{line}}^2 \sin^2(\omega t)}{R_e V_{\text{out}}} = \frac{V_{\text{line}}^2 \sin^2(\omega t)}{R_S V_{\text{out}}} \cdot u(t) \tag{6}$$

where V_{out} is the dc value of the output voltage, which is assumed to be much larger than the output capacitor ripple. It can be seen that the system in Fig. 5(a) consists of a time-varying current source controlled by the control variable $u_t(\text{t})$, A/D converter, and a linear time-invariant part comprised of a parallel connection of the output capacitor and the load (output impedance Z_{out}).

B. Voltage Loop Compensator Design

To design a compensator for the time varying system of Fig. 5(a), we use the frozen coefficients method [24]. In this approach, we "freeze" the time-varying system at a selected time point and analyze the structure as if it were a time invariant linear system. The system is frozen at the point which is assumed to be the most critical for its stability: when the input line voltage $v_g(t) = V_{\text{line}}|\sin(\omega t)|$ has the maximum value and when the additional gain introduced by analog-to-digital converter nonlinearity is the largest. The maximum instantaneous value of the input voltage in a universal-input PFC is $V_{\text{line\_max}} = 260\sqrt{2}$ V.

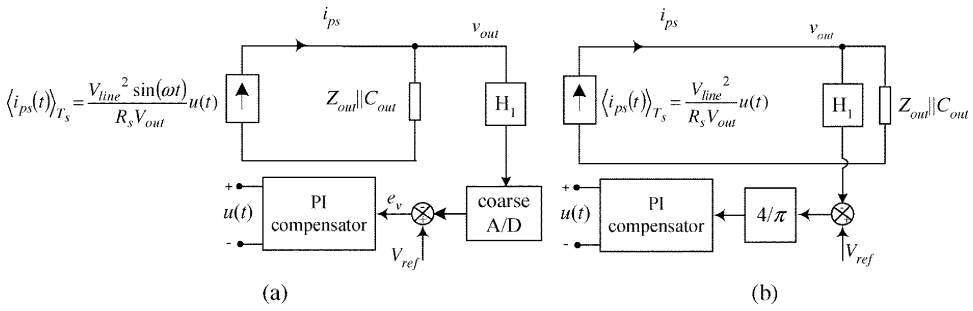

Fig. 5. (a) Time-varying large-signal model of the dead-zone controller with linear dependence between control variable u(t) and output voltage v(t) and (b) time-invariant linear system obtained using frozen coefficients method.

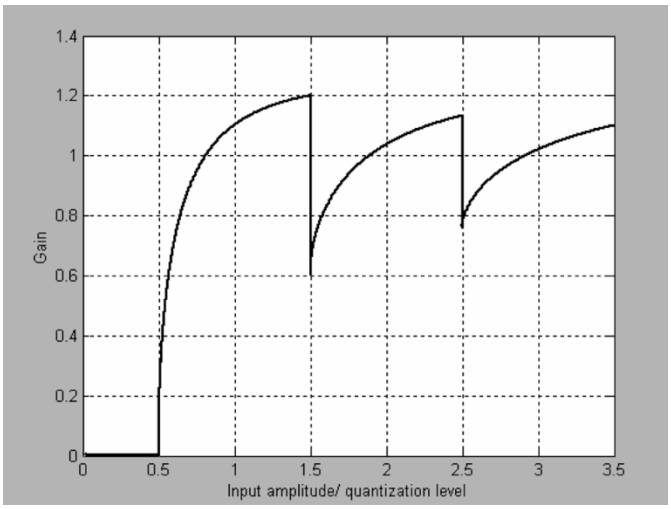

Fig. 6. Describing function of an analog-to-digital converter that shows dependence of the effective "gain" on the ratio of the input signal magnitude V_M and the quantization level V_q.

The gain variation introduced by the coarse resolution A/D is analyzed using an approximate method based on describing functions [25]. The describing function of the A/D with the quantization level equal to V_q is plotted in Fig. 6. It can be seen that the "gain" of the A/D depends on the input signal amplitude and can be as large as $4/\pi$. Fig. 6 also provides an additional explanation of the dead-zone controller operation. It shows that the "gain" of the A/D is zero for the amplitudes of the input signal smaller than one half of the quantization level. In the case of the PFC controller this corresponds to a complete elimination of the output voltage ripple when its peak-to-peak amplitude is inside the zero-error bin, i.e., within the dead-zone.

With the aim of transforming the system of Fig. 5(a) into a time-invariant linear system, the maximum gains of the time-varying current source and the A/D can be replaced with their maximum values, $V_{\text{line\_max}}$ and $4/\pi$ respectively, as shown in Fig. 5(b).

After the linear time-invariant system is obtained, a fast digital compensator can be designed. In the experimental prototype, which is described in Section V, a constant coefficients PI regulator is used. The compensator is obtained through digital redesign, where an analog compensator is designed first and then its digital equivalent is constructed using the pole-zero

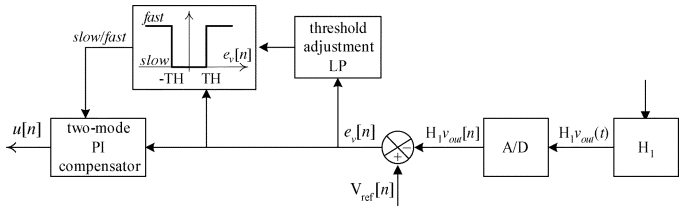

Fig. 7. Voltage loop regulator with the self-adjusting dead-zone controller.

mapping technique [26]. The discrete time control law of the compensator is given by

$$u[n] = u[n-1] + K_1 \left(e_v[n] - a_1 e_v[n-1]\right). \qquad (7)$$

The compensator characteristic can be adjusted by changing the gain K_1 and a_1, the parameter that determines the frequency of the compensator zero.

It should be noted that the design based on the frozen coefficients method does not always guarantee the system stability. In order to confirm the system stability under all operating conditions, the stability assessment method described in [27] can be applied. In this method, which is based on the circle criterion [28], the system stability verification involves two steps. First, the output voltage control loop of Fig. 5(b) is divided into two parts: a time-varying element represented by a sinusoidal current source, and a time-invariant linear part that contains all other parts of the block diagram. In the second step, the Nyquist plot of the linear part and the gain variation of the time-varying part, representing a half plane, are drawn in the same plane. These plots allow application of the circle criterion [28], which states that the system is stable if the Nyquist's plot does not intersect the half-plane of the time-varying gain. Further details of the stability assessment can be found in [27].

IV. Self-Adjustable Dead-Zone Controller

An improvement of the fixed dead-zone controller that eliminates the output voltage steady state error for light loads or capacitive load conditions and further improves voltage loop dynamic response is shown in Fig. 7.

The improvements of the fixed dead-zone method presented in Section II are obtained using a higher-resolution analog-to-digital converter ($V_q < 2\Delta v_c$), a comparator, a threshold adjustment circuit, and a dual-mode voltage loop compensator. The

idea of the dual-mode voltage loop compensator as an enhancement of the regulation-band approach in analog PFC controllers originates from [19].

The controller operates as follows: as long as the amplitude of the voltage error signal $e_v[n]$ is smaller than the threshold TH, the comparator output is low and the voltage loop PI compensator operates in a slow low-bandwidth mode with the voltage loop closed in the 10–20 Hz range. The low-bandwidth mode results in zero steady state error and elimination of the second harmonic from the voltage loop. During a transient, the voltage error signal exceeds the threshold value, sets the comparator to high level and causes a change of the voltage loop compensator to a high-bandwidth mode that provides faster response. The change of the PI compensator mode is performed through a change of the controller coefficient values K_1, and a_1 in (7). Design of the controller and selection of the coefficient for the low-bandwidth mode are based on the low-frequency model of the rectifier obtained by averaging over a half line cycle [17].

The adaptive threshold adjustment is implemented as shown in Fig. 7. A block that performs rectification and low-pass filtering of the voltage error signal sets up the threshold to a value slightly higher than the steady-state voltage ripple amplitude. The filtering and the threshold calculation are performed as

$$TH = \frac{1}{2N - \varepsilon} \sum_{n=1}^{N} |e_v[n]| \tag{8}$$

where TH is the threshold value, N is the number of voltage error samples and ε is a correction factor, which ensures that the threshold is always slightly larger than the amplitude of the steady state voltage error ripple. The low-pass filter does not allow fast threshold variations during transients, and provides a slow adjustment of the dead-zone in accordance with the steady state ripple value. Consequently, it allows further improvements of both static and dynamic characteristics of the voltage loop.

The filtering and the threshold computation based on (8) are suitable for fixed-point DSP implementation where the required memory for storage of the error samples is easily available. Alternative implementations of the moving-average filter are possible with reduced memory requirements, but at the expense of performing computations with a longer digital word [26]. Such simpler hardware implementations would be better suited for FPGA or custom IC based implementations.

The self-adjustable dead-zone method can be considered a digital implementation of the analog fixed regulation band control with variable PI compensator parameters [19], [23]. In comparison with the analog realizations, the digital implementation provides an added degree of flexibility in programming the compensator parameters. In addition, the adaptive adjustment of the dead zone results in improved transient responses by eliminating the delay in the response due to the slow compensator action while the output voltage is within the regulation band.

V. Experimental Results

An experimental prototype based on the block diagram shown in Fig. 8 has been used to test the presented control methods.

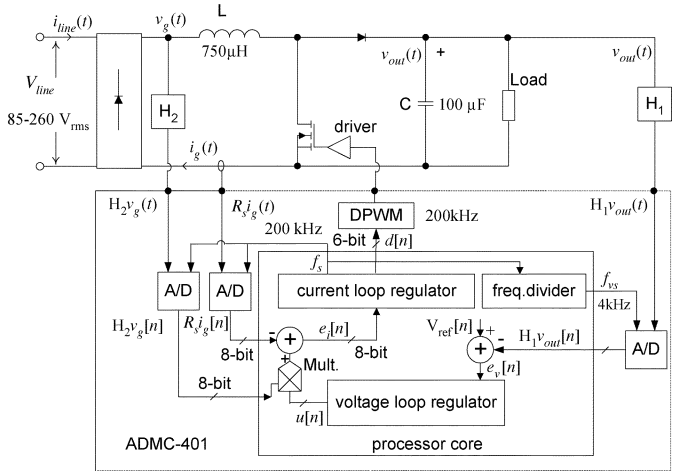

Fig. 8. Experimental system.

A. Experimental Prototype

An experimental 250 W boost PFC operating at 200-kHz switching frequency is controlled by an ADMC-401 16-b DSP evaluation board. To implement the fixed dead-zone voltage loop controller described in Section II, the resolution of the analog to digital converter was limited to six bits. In the implementation of the self-adjusting dead-zone controller of Section IV, 8 b of the on-board A/D converter output were used.

Although the ADMC-401 includes a 16-b fixed-point processor, 8-b arithmetic was used for all computations in order to show that the complete system could be implemented with a simpler hardware. The output voltage is controlled at 375 V, and sampled at $f_{vs} = 4$ kHz. This frequency satisfies the requirement $f_{vs} \gg 2f_{\text{line}}$, and at the same time allows implementation of both high-bandwidth and low-bandwidth digital compensators using 8-b arithmetic.

The operating point of the analog to digital converter in the fixed dead-zone controller is selected to give an equivalent output voltage quantization step equal to 15 V around the operating point. This quantization step is slightly larger than the maximum expected peak-to-peak ripple across the output filter capacitor. The input current is sampled at 200 kHz using the variable-delay sampling method and the current control loop described in [7]. The same hardware structure was used for verification of both the fixed and the self-adjusting dead-zone control methods. All modifications required to implement the self-adjusting dead-zone controller were completed in software.

B. Steady-State Operation and Limit-Cycling Issues

In general, a feedback system with a strong nonlinearity, such as the dead zone, is susceptible to instabilities, which can result in undesirable limit cycle oscillations. In typical limit cycle oscillations, the converter voltage and currents bounce periodically around a desired steady-state operating point. This type of instability can occur even in analog PFCs with a regulation band [19], [20], [23]. When the output voltage is within the regulation band, the voltage regulation loop is effectively open. Because of the analog integrator drift in the voltage-loop error amplifier, or because of the integral action of the output filter capacitor, the open-loop output voltage tends to drift toward one of the regulation band limits, and then back toward the other limit. As a

result, the output voltage and the amplitude of the input current may bounce periodically around the desired steady-state values.

In this section, we examine steady-state operation and possible limit-cycle oscillations in the proposed digital dead-zone controllers. Experimental results are used to illustrate the discussion.

Consider a PFC with a resistive load R and the fixed dead-zone controller of Section II. In steady state, referring to Fig. 4, the command $u[n]$ is constant and, neglecting losses, the output power averaged over one half line cycle is $P = V_{\rm line}^2/R_e = (V_{\rm line}^2/R_s)u[n]$. The steady-state solution for the dc output voltage can be found from

$$\frac{V_{\rm out}^2}{R} = P. \tag{9}$$

Because of the quantization of the command $u[n]$, the finite resolution of the A/D converters for sensing the input voltage $v_g(t)$ and the input current $i_g(t)$, as well as the finite resolution of the DPWM, the power P is also quantized. Let q_P be the power quantization level, i.e., the effective least significant bit (LSB) value of the average power P delivered to the output. From (9) we can find the quantization step $\Delta V_{\rm out}$ in the output voltage that corresponds to the power quantization level

$$\frac{2V_{\rm out}\Delta V_{\rm out}}{R} = q_P, \tag{10}$$

$$\Delta V_{\rm out} = \frac{q_P}{2}\frac{R}{V_{\rm out}} = \frac{q_P}{2}\frac{V_{\rm out}}{P}. \tag{11}$$

Similar to the static no-limit-cycling condition formulated in [29], [30] for digitally controlled dc/dc converters, the static no-limit-cycling condition for the PFC with the fixed dead-zone controller can be formulated in terms of the output voltage quantization step $\Delta V_{\rm out}$ and the quantization step V_q of the output voltage A/D converter

$$H_1\Delta V_{\rm out} < \frac{V_q}{2}. \tag{12}$$

Notice that (12) is a necessary condition for existence of a stable steady-state solution. If the condition (12) is not satisfied, the output voltage will bounce around the desired steady-state value. Combining (11) and (12), we have the static no-limit-cycling condition

$$\frac{q_P}{P} < \frac{V_q}{H_1 V_{\rm out}} \tag{13}$$

which implies that the effective resolution in the power command must be better than the resolution of the voltage A/D converter. This condition is comparable to the static no-limit-cycling condition for digitally controlled dc/dc converters [29], [30], which states that the effective DPWM resolution (in terms of the output voltage) must be better than the resolution of the A/D converter. For a given input line voltage, q_P in (13) depends on the hardware realization, and is a constant. Hence, the condition (13) is more difficult to meet at lower output power.

In our experimental prototype with the fixed dead-time controller, we found that the PFC has a stable steady-state operation without limit-cycle oscillations for the output power greater than about 50 W, or about 20% of the maximum output power.

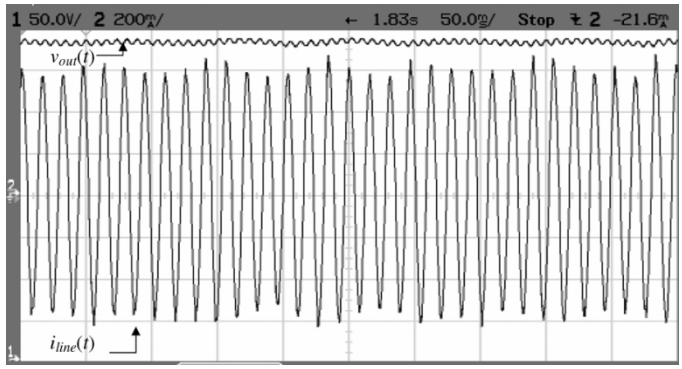

Fig. 9. Limit-cycle oscillations in the experimental PFC with the fixed dead-zone controller at a light load (45 W). Time scale is 50 ms/div, Ch.1: $v_{\rm out}(t)$, 50 V/div, Ch-2: $i_{\rm line}(t)$, 0.2 A/div. The input rms voltage is 110 V.

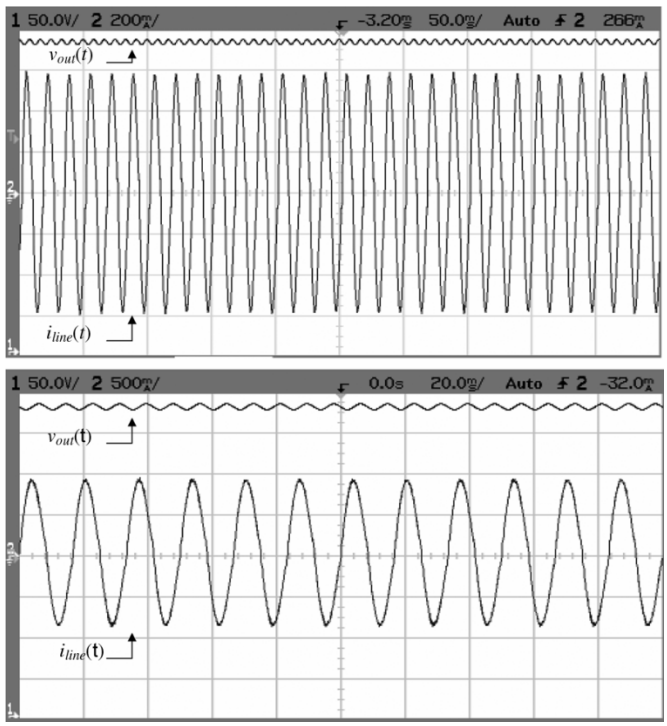

Fig. 10. Input current and output voltage in steady state operation of the PFC with the self-adjustable dead-zone controller. The input voltage is $V_{\rm line}$ = 110 rms, and the output load is 45 W (top) and 75 W (bottom) Ch-1: $v_{\rm out}(t)$, 50 V/div, Ch-2: $i_{\rm line}(t)$ 0.5 A/div.

For example, Fig. 9 shows limit cycle oscillations at the output power of 45 W.

For analog PFC controller with a regulation band, a PI compensator with changing parameters (slow inside the regulation band, and fast outside the regulation band) has been proposed as a solution to the limit-cycle oscillation problem [19]. As noted in Section IV, the self-adjustable dead-zone controller is a digital implementation of this approach.

Fig. 10 shows stable steady-state operation of the PFC with the adjustable dead-zone controller at 45 W and at 75 W. No limit cycle oscillations are observed. Fig. 11 shows an expanded view of the steady-state input voltage and ac line current, demonstrating low harmonic distortion and high power factor of the experimental PFC rectifier with adjustable dead-zone control.

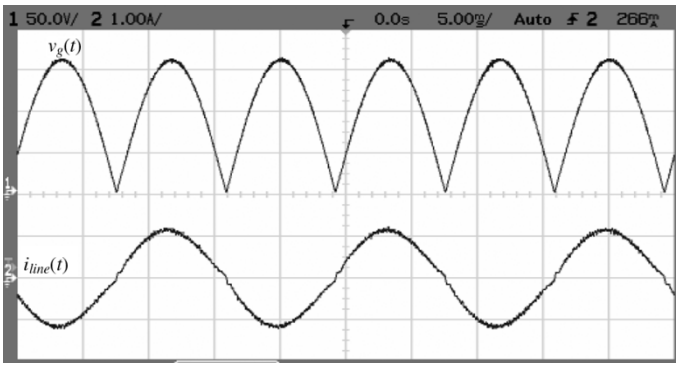

Fig. 11. Input current and rectified input voltage in steady-state operation of the PFC with the self-adjustable dead-zone controller. The rms value of the input voltage is 110 V, the output voltage is regulated at 375 V and the output load is 100 W. The measured power factor is 0.997. Ch-1: $v_g(t)$, 50 V/div, Ch-2: $i_{\rm line}(t)$ 1 A/div.

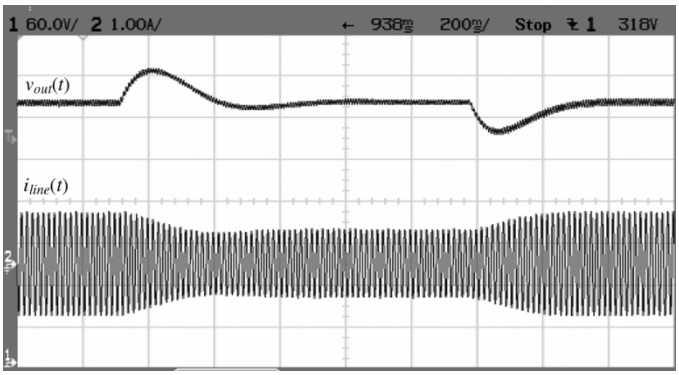

Fig. 12. Load transient response of the experimental PFC system with a conventional, slow controller for 100 W–50 W and 50 W–100 W load changes for $V_{\rm line}$ = 110 V. Time scale 200 ms/div, Ch-1: $v_{\rm out}(t)$, 60 V/div, Ch-2: $i_{\rm line}(t)$, 1 A/div.

C. Load Transient Responses

As a reference, Fig. 12 shows 100 W–50 W–100 W load transient responses of the PFC with a conventional, slow voltage loop controller. This controller is the same as the low-bandwidth controller of the self-adjustable dead-zone method. Large overshoots and dips of the output voltage can be observed, with settling times that extend over a number of line periods. The overshoots cause additional voltage stresses on the components, while the voltage dips could cause a loss of regulation at high input line voltage, and increased current stresses on a downstream converter. Attempting to increase the bandwidth of the voltage loop without eliminating even harmonics of the line frequency from the loop results in much higher harmonic distortion, as shown in [7] and [18].

Figs. 13–15 show load transient responses of the fixed and self-adjustable dead-zone controllers for the 100 W–150 W–100 W output load change. Because of the increased voltage ripple at heavier loads, the output voltage regulation in the fixed dead-zone controller is improved, and since the output power is relatively high, no limit cycle oscillations are observed. Both methods result in very similar load transient responses. Compared to the conventional low-bandwidth design, the responses are much faster, and the voltage overshoots and dips are significantly smaller. Fig. 15 shows that similar transient responses are obtained at high line voltage, even though no feed-forward compensation of the input voltage was implemented in the experimental PFC with the self-adjustable dead-zone controller.

Fig. 13. Load transient response for 100 W–150 W–100 W output load changes in the experimental PFC with the fixed dead-zone controller (top) and the self-adjustable dead-zone controller (bottom). Time scale 50 ms/div, Ch-1: $v_{\rm out}(t)$, 50 V/div, Ch-2: load transient, Ch-4: $i_{\rm line}(t)$, 0.5 A/div. The input rms voltage is 110 V.

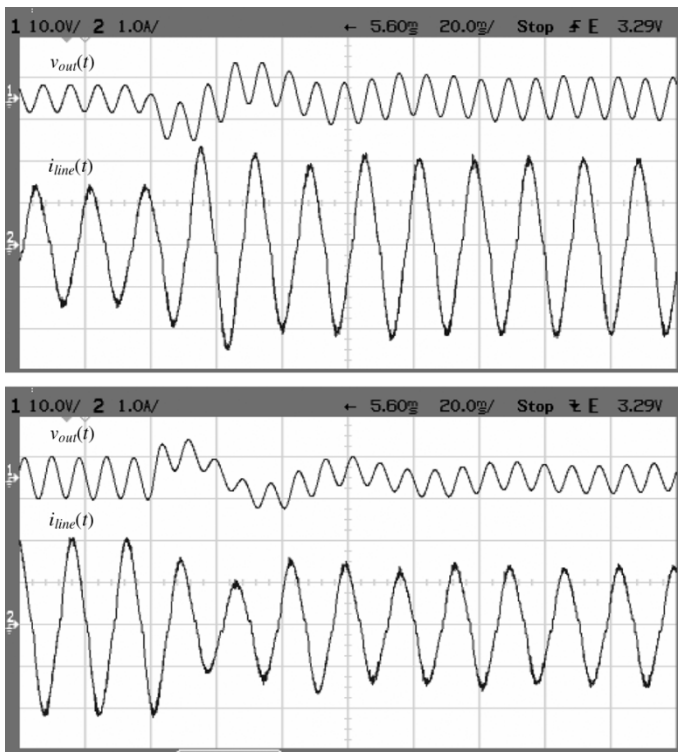

Fig. 14. Details of the load transient responses for 100 W–150 W–100 W output load changes in the experimental PFC with the adjustable dead-zone controller. Top: light-to-heavy load transient. Bottom: heavy-to-light load transient. Time scale is 20 ms/div, Ch-1: $v_{\rm out}(t)$, 10 V/div (ac-coupling), Ch-2: $i_{\rm line}(t)$,1 A/div. The input rms voltage is 110 V.

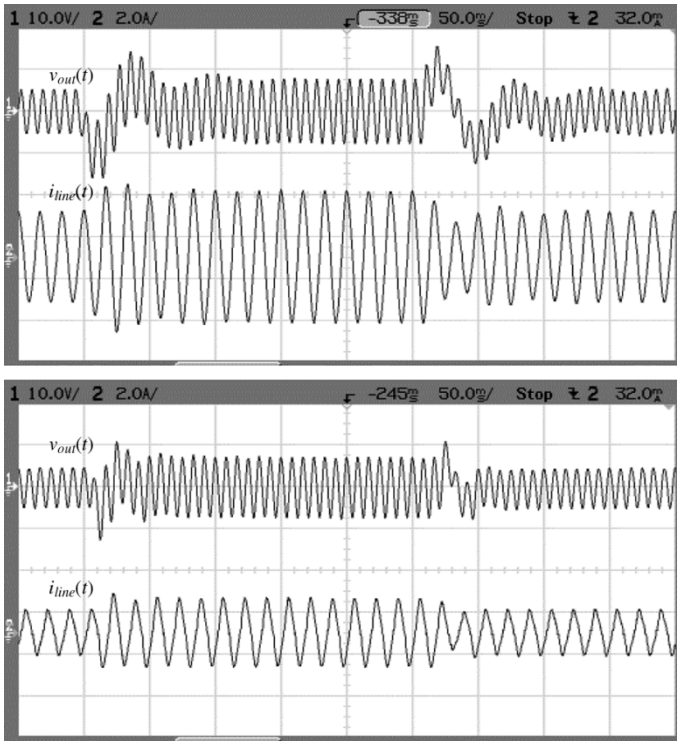

Fig. 15. Output voltage and input current during load transients between 150 W and 250 W for the input rms voltage of 110 V (top) and 220 V (bottom). The time scale is 50 ms/div, Ch-1: $v_{\rm out}(t)$, 10 V/div (ac-coupling), Ch-2: $i_{\rm line}(t)$, 2 A/div.

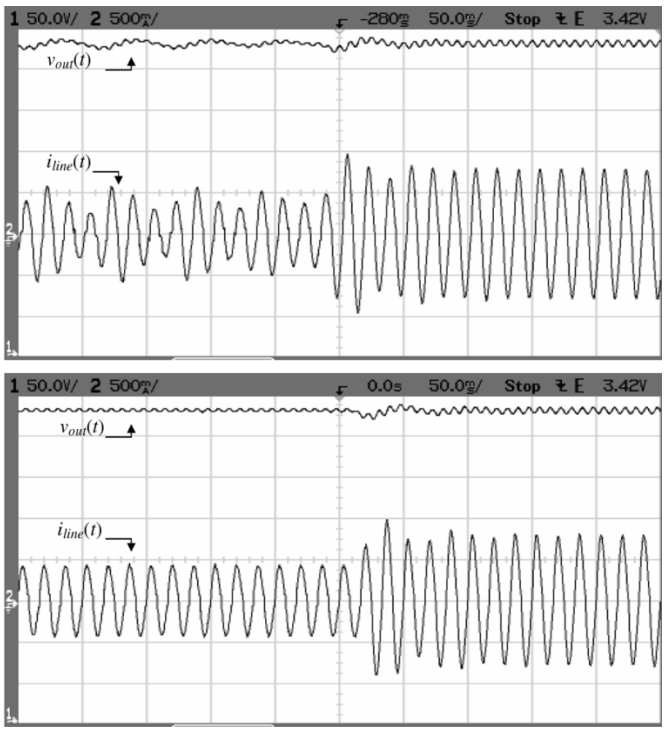

Fig. 16. Output voltage and input current during a 30–60 W load transient in the experimental PFC with the fixed dead-zone controller (top), and the self-adjustable dead-zone controller (bottom). The time scale is 100 ms/div, Ch1: $v_{\rm out}(t)$, 50 V/div, Ch-2: $i_{\rm line}(t)$, 0.5 A/div.

Fig. 16 shows light-load transients (30 to 60 W). For the fixed dead-zone method, limit-cycle oscillations can be observed for the light load case (30 W). When the output power is increased to 60 W, the PFC with the fixed dead-zone controller exhibits a stable steady-state operation. No limit-cycle oscillations are observed when the self-adjustable dead-zone controller is applied. These observations are consistent with the discussion in Section V-B.

VI. Conclusion

This paper describes a dead-zone control method for improvement of voltage loop dynamic responses in digitally controlled low-harmonic rectifiers [i.e., power factor correctors (PFC)]. Implementation of the dead-zone controller is based on a simple modification of the analog-to-digital converter characteristic and does not require any additional hardware or processing. The dead-zone is the range of output voltages that produces a zero error at the output of the A/D converter. By selecting the A/D resolution, i.e., its quantization step, around the reference, the dead-zone is selected to be larger than the expected output voltage ripple. In steady-state, the output voltage error is zero and the second harmonic does not affect operation of the voltage loop. In transients, a fast voltage loop can be designed to quickly bring the output voltage back to regulation, without increasing distortion of the input line current.

A method for fast voltage loop compensator design is also shown. It is based on a transformation of the nonlinear time-varying model of the fast voltage loop into a linear time-invariant system using a describing function model for the voltage A/D converter, and the frozen coefficient method to replace the time-varying part of the system with a linear, time-invariant model. The system stability can be verified using a method based on the circle criterion.

Two versions of the dead-zone method are presented: a fixed dead-zone controller and a self-adjusting dead-zone controller. In the fixed dead-zone method, the zero error range has a constant value, designed for the maximum expected output voltage ripple. In the self-adjustable method, the dead zone is adjusted to match the actual output voltage ripple. With changes in the control software and a relatively small increase in processing, the self-adjusting dead-zone controller offers improved static voltage regulation and improved steady-state operation without limit cycle oscillations. Both dead-zone controllers offer much faster voltage transient responses and significantly reduced voltage overshoots and dips compared to standard, low-bandwidth voltage controllers in PFC systems.

Experimental results obtained on a DSP controlled 250-W boost PFC operating at 200-KHz switching frequency show an order of magnitude faster load transient responses with the dead-zone controllers compared to the responses with a conventional low-bandwidth controller.

Advantages of the proposed method include: smaller output voltage variations, a potential for less conservative designs of the PFC and downstream dc/dc converters, and simpler controller implementation compared to alternative methods for improvement of voltage-loop dynamic responses in digitally controlled PFC systems.

REFERENCES

[1] P. Zumel, A. De Castro, O. Garcia, T. Riesgo, and J. Uceda, "Concurrent and simple digital controller of an AC/DC converter with power factor correction," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 334–343, Jan. 2003.

[2] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 814–823, Sep. 1998.

[3] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Power factor preregulators with improved dynamic response," in *Proc. IEEE PESC Conf.*, 1995, pp. 150–156.

[4] J. Chen, A. Prodić, D. Maksimović, and R. W. Erickson, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 411–419, Jan. 2003.

[5] S. Bibian and H. Jin, "Digital control with improved performance for boost power factor correction circuits," in *Proc. IEEE APEC Conf.*, 2001, pp. 137–143.

[6] W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, "A digital power factor correction (PFC) control strategy optimized for DSP," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1474–1485, Nov. 2004.

[7] A. Prodić, J. Chen, R. W. Erickson, and D. Maksimović, "Self-tuning digitally controlled PFC having fast dynamic response," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 420–428, Jan. 2003.

[8] K. De Gusseme, D. Van de Sype, A. P. Van den Bossche, and J. A. Melkebeek, "Sample correction for digitally controlled boost PFC converters operating both in CCM and DCM," in *Proc., IEEE APEC Conf.*, 2003, pp. 389–395.

[9] S. Kim and P. Enjeti, "Control of multiple single phase PFC modules with a single low-cost DSP," *IEEE Trans. Ind. Appl.*, vol. 18, no. 5, pp. 1379–1385, Sep. 2003.

[10] ——, "A parallel-connected single phase power factor correction approach with improved efficiency," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 87–93, Jan. 2004.

[11] P. Mattavelli, P. Spiazzi, and P. Tenti, "Predictive digital control of power factor preregulators with input voltage estimation using disturbance observers," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 140–147, Jan. 2005.

[12] M. Fu and Q. Chen, "A DSP based controller for power factor correction (PFC) in a rectifier circuit," in *Proc. IEEE APEC Conf.*, 2001, pp. 144–149.

[13] J. Zhou, Z. Lu, Z. Lin, Y. Ren, Z. Qian, and Y. Wang, "A novel DSP controlled 2 kW PFC converter with a simple sampling algorithm," in *Proc. IEEE APEC Conf.*, 2000, pp. 434–437.

[14] K. De Gusseme and D. Van De Sype, "Design issues for digital controller of boost power factor correction converters," in *Proc. IEEE ISIE Conf.*, 2002, pp. 26–29.

[15] A. H. Mitwalli, S. B. Leeb, G. C. Verghese, and V. J. Thottuvelil, "An adaptive digital controller for a unity power factor converter," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 374–382, Mar. 1996.

[16] P. Mattavelli, W. Stefanutti, G. Spiazzi, and P. Tenti, "Digital control of single-phase power factor preregulators suitable for smart-power integration," in *Proc. IEEE PESC*, 2004, pp. 3195–3201.

[17] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Boston, MA: Kluwer, 2000, pp. 668–673.

[18] R. Erickson, M. Madigan, and S. Singer, "Design of a simple high power factor rectifier based on the flyback converter," in *Proc. IEEE APEC Conf.*, 1990, pp. 792–801.

[19] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Methods to improve dynamic response of power factor preregulators: an overview," in *Proc. IEE EPE Conf.*, vol. 3, 1995, pp. 754–759.

[20] J. B. Williams, "Design of feedback loop in unity power factor AC to dc converter," in *Proc. IEEE PESC Conf.*, 1989, pp. 959–967.

[21] S. Wall and R. Jackson, "Fast controller design for single-phase power-factor correction system," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 654–660, Oct. 1997.

[22] M. O. Eissa, S. B. Leeb, G. C. Verghese, and A. M. Stanković, "Fast controller for unity-power-factor PWM rectifier," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 1–6, Jan. 1996.

[23] J. Lazar and S. Ćuk, "Feedback loop analysis for AC/DC rectifiers operating in discontinuous conduction mode," in *Proc. IEEE APEC*, 1996, pp. 797–806.

[24] W. L. Brogan, *Modern Control Theory*, 3rd ed. Upper Saddle River, NJ: Prentice-Hall, 1991, pp. 358–361.

[25] J. H. Taylor. (1999) Describing Functions. Electrical Engineering Encyclopedia. [Online] Available: http://www.ee.unb.ca/jtaylor/Publications/EEncyc_final.pdf

[26] G. F. Franklin, J. D. Powell, and M. Workman, *Digital Control of Dynamic Systems*, 3rd ed. Menlo Park, CA: Addison-Wesley, 1997, pp. 200–202.

[27] A. Prodić and D. Maksimović, "Stability of the fast voltage control loop in power factor correctors," in *Proc. IEEE PESC*, 2004, pp. 2320–2325.

[28] G. Zames, "On the input-output of time-varying nonlinear feedback systems part II: conditions involving circles in the frequency plane and sector nonlinearities," *IEEE Trans. Automat. Contr.*, vol. 11, no. 3, pp. 465–476, Jul. 1966.

[29] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003.

[30] H. Peng, D. Maksimovic, A. Prodic, and E. Alarcon, "Modeling of quantization effects in digitally controlled dc/dc converters," in *Proc. IEEE PESC*, 2004, pp. 4312–4318.

Aleksandar Prodić (S'00–M'03) received the B.Sc. degree in electrical engineering from the University of Novi Sad, Novi Sad, Yugoslavia, in 1994 and the M.Sc. and Ph.D. degrees from the Colorado Power Electronics Center, University of Colorado, Boulder, in 2000 and 2003, respectively.

Since 2003, he has been with the University of Toronto, Toronto, ON, Canada, where he is an Assistant Professor. He established the Laboratory for Low-Power Management and Integrated Switch-Mode Power Supplies at the University of Toronto in 2004. His research interests include digital control of low-power high-frequency SMPS, mixed-signal IC design, DSP techniques for power electronics, and the development of systems-on-chip (SoC) for power management.

Dragan Maksimović (M'89) received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, Yugoslavia, in 1984 and 1986, respectively, and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1989.

From 1989 to 1992, he was with the University of Belgrade. Since 1992, he has been with the Department of Electrical and Computer Engineering, University of Colorado, Boulder, where he is currently an Associate Professor and Co-Director of the Colorado Power Electronics Center (CoPEC). His current research interests include power electronics for low-power, portable systems, digital control techniques, and mixed-signal integrated circuit design for power management applications.

Dr. Maksimović received the NSF CAREER Award, and the IEEE Power Electronics Society TRANSACTIONS Prize Paper Award in 1997.

Robert W. Erickson (S'82–M'82–SM'97–F'01) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 1978, 1980, and 1982, respectively.

Since 1982, he has been a member of the Faculty of Electrical and Computer Engineering, University of Colorado, Boulder, where he is currently Professor and Chairman. The Colorado Power Electronics Center, established and co-directed by him, is helping the industry in low-harmonic rectifiers, dc/dc converters for battery-powered systems, and magnetics modeling for multiple-output converters. He is the author of *Fundamentals of Power Electronics*, now in its second edition. He is the author of approximately 60 journal and conference papers in the area of power electronics.

Dr. Erickson received the IEEE Power Electronics Society TRANSACTIONS Prize Paper Award for the paper "Nonlinear Carrier Control for High-Power-Factor Boost Rectifier," in 1996.