Letters

An EMI Reduction Technique for Digitally Controlled SMPS

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***Abstract*—A spread spectrum technique and system for reducing average electromagnetic interference (EMI) in low-power digitally controlled dc-dc switch-mode power supplies (SMPS) are introduced. The technique utilizes very simple hardware, where the switching frequency of a SMPS is dynamically varied over a controlled range. This is achieved by changing the supply voltage of a ring-oscillator based digital pulse-width modulator in a pseudo-random fashion, through 128 discrete steps. The change is performed with a 1–b $\Delta\Sigma$ digital-to-analog converter. Compensator design guidelines for this variable frequency system are provided for obtaining good dynamic response. The technique was tested with a 500-mW, 1.8-V buck converter prototype, whose switching frequency was varied from 1.74 to 2.84 MHz. A reduction of 23 dB in the conducted EMI with an efficiency degradation of less than 0.1% was obtained, compared to fixed frequency operation.**

***Index Terms*—DC–DC, digital control, electromagnetic interference (EMI) reduction, low-power, spread spectrum.**

I. Introduction

In MODERN noise-sensitive hand-held devices, such as mobile phones, personal data assistants (PDAs), and digital still cameras (DSCs), the close proximity of semiconductor power-stages to the supplied functional blocks causes significant electromagnetic interference (EMI) problems, despite the relatively low processed power. Harmonic trap filters [1], often used in medium-to-high power applications, require bulky and expensive passive components, which makes them unsuitable for space-limited and price-sensitive portable devices. The selection of the filter parameters presents additional design challenges, due to the presence of multiple switch-mode power-supplies (SMPS) operating at different switching frequencies and often influencing each other in unpredictable ways. Alternative, pre-emptive EMI mitigation techniques [2]–[7] eliminate the need for EMI filters by spreading the SMPS noise over a frequency range. This is typically achieved by varying the switching frequency of the SMPS. By doing so, the noise generated by the SMPS can be spread across a well defined frequency band. As a result, the average spectral power density (SPD) of the broadband noise can thus be drastically reduced. Fig. 1(a) shows the input current spectrum of a fixed-frequency SMPS. The case when the switching frequency is randomly switched within the range of $f_0 - BW/2 < f_s < f_0 + BW/2$ is shown in Fig. 1(b). It is important to recognize that within each time slot where the switching frequency is fixed, the peak SPD is identical to that of Fig. 1(a), while the average SPD is reduced. It is well proven that this spread spectrum technique, or randomized pulse-width modulation (PWM) dramatically reduces the average EMI in SMPS [8], [9] and allows the average noise to fall below the legal electromagnetic compatibility (EMC) standards.

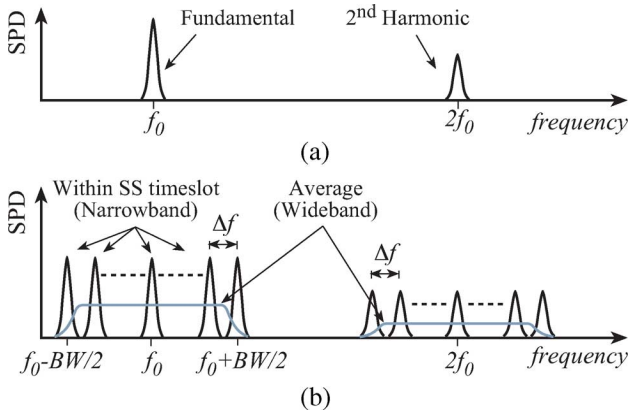

Fig. 1. Typical EMI spectral power density of a SMPS system operating with (a) fixed switching frequency f_0 and (b) frequency hopping resulting in spread spectrum.

On the system level, the existing techniques usually involve tradeoffs between the losses/stress in power-stage, the added complexity of the controller, and the effectiveness of EMI mitigation [6]. In higher power converters digital solutions based on frequency modulation [10], [11] are effectively used. However, from the practical point of view, existing solutions are not suitable for SMPS used in hand-held applications with switching frequencies in the multi-MHz range, mainly due to the reliance on complex and power-hungry frequency-synthesis hardware.

Control-based methods having inherent variable switching frequency such as single-bit $\Delta\Sigma$ modulation [9], chaotic control [12] and hysteretic methods [13] may also be considered for EMI mitigation; however they usually do not have a good control of the switching frequency range and, consequently, require over-design of the power-stage. This inevitably leads to increased losses in the power-stage. Control-based methods having a predictable switching frequency, such as multi-bit $\Delta\Sigma$ modulation, dithering-based systems [3], as well as soft switching converters [14], provide a relatively modest reduction in EMI which may not satisfy EMC limits dictated by agencies

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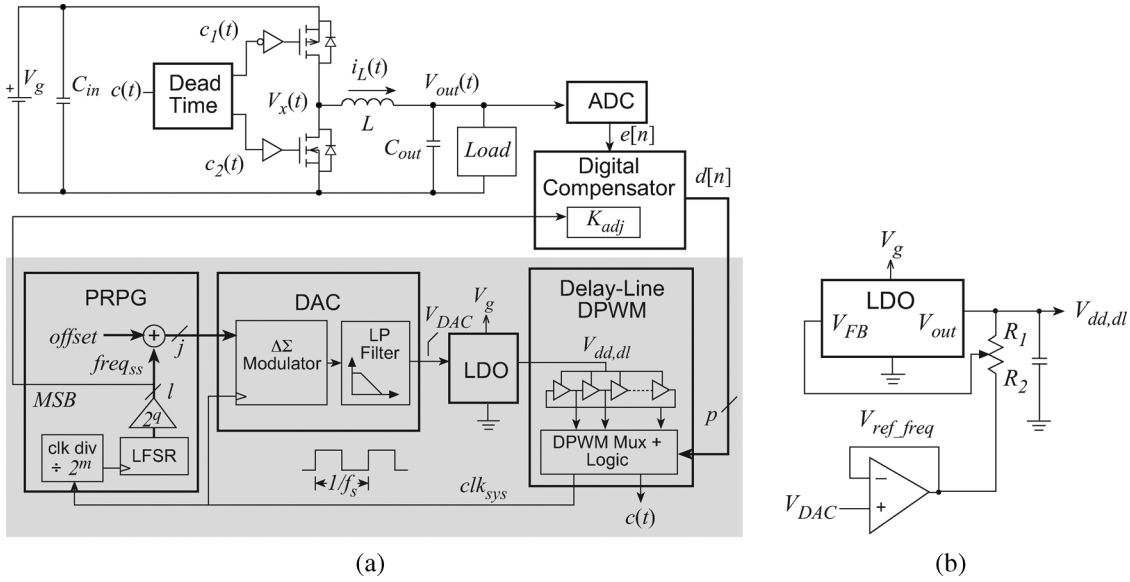


Fig. 2. (a) Architecture of the spread spectrum system (shaded) as part of a digitally controlled buck converter. (b) Modified circuit used in this work to accommodate an off-chip LDO having a fixed internal reference in the proof-of-concept prototype.

such as CISPR, FCC, etc. Dedicated spread spectrum clock synthesizers integrated circuit (IC)-s [8], developed for analog controlled low-power SMPS, could potentially be combined with some of the existing low-power digital controllers, but the resulting multichip solution and inherent hardware redundancy would significantly raise the system cost.

The main goal of this letter is to introduce a spread spectrum technique and simple hardware architecture that effectively constrains the switching frequency range and performs strong EMI mitigation. The system is designed for easy integration with existing low-power digital controllers with ring-oscillator based pulse-width modulators, thereby eliminating the need for an additional frequency synthesizer as in [8] and [15] and minimizing hardware redundancy. In addition, the flexibility of the digital implementation provides programmability of various parameters such as the spread spectrum bandwidth and center frequency. In the following sections we give a brief description of the novel system, provide a design procedure for its compensator design, and show experimental results demonstrating the effectiveness of this method.

II. Achieving Spread Spectrum

A. Spread Spectrum Architecture

A variety of digital pulsewidth modulator (DPWM) topologies based on tapped delay lines and/or ring oscillators have been demonstrated to achieve low power consumption, high switching frequency f_s and high resolution, as summarized by [16]. While the numerous existing delay line DPWMs may differ slightly due the choice of reset architecture and the use of segmented and/or hybrid counter approach, their core consists of delay cells having a supply-voltage-dependent propagation time. It is well known that this delay, and hence the oscillation frequency of any CMOS-based ring oscillator, can be tuned by varying its supply voltage. The proposed spread spectrum DPWM architecture shown in Fig. 2 is based on this simple concept applied with a pseudo-random pattern generator (PRPG) scheme [8], [10].

The generic self-oscillating delay-line DPWM is used to generate both the spread spectrum system clock clk_{sys}, as well as the high precision PWM pulse $c(t)$ required for output voltage regulation. The delay-line's supply voltage, $V_{dd,dl}$ is controlled by a low drop-out linear regulator (LDO) whose reference voltage, $V_{\text{ref\_freq}}$ is modulated to achieve a variable switching frequency f_s, where $(f_0 - BW/2) < f_s < (f_0 + BW/2)$. The modified circuit shown in Fig. 2(b) was used in this work to build a proof-of-concept system with an off-chip LDO having a fixed internal reference.

A k-element linear feedback shift-register (LFSR) with optimum taps is used to generate a 2^k-cycle pseudo-random sequence to achieve a uniformly distributed frequency target [8]. The output of the LFSR is scaled by a factor of 2^q, which allows the spread spectrum bandwidth BW to be digitally adjusted. A 1-b bus, $freq_{ss}$ is extracted from the LFSR and converted to $V_{\text{ref\_freq}}$ using a $\Delta\Sigma$ DAC having a j-b input bus. The $\Delta\Sigma$ DAC includes a digital noise-shaping modulator and low-pass reconstruction filter. The DAC in Fig. 2(a) is used to generate the analog voltage reference for the LDO. In this application, the DAC sampling rate, $f_{\text{DAC}} = f_{sys}/\text{OSR}$, is set by the m-b clock-divider circuit, where the oversampling rate is $\text{OSR} = 2^m$. The one-bit $\Delta\Sigma$ DAC topology is chosen for this work because it offers high linearity, low power (no quiescent current) and potential for compact on-chip implementation. For a 1st order modulator, it can be shown that the noise falls by 9 dB and hence the effective resolution increases by 1.5 b for every doubling of the OSR [17].

The proposed architecture is compatible with monolithic IC implementation and the vast majority of the functionality can be achieved using synthesizable digital blocks. A regulated supply is required for any delay-line DPWM to reduce jitter, and hence the LDO does not add to the system cost. It is only used to supply dynamic current to the delay-line DPWM circuit block

that draws very low current. For example, a self-calibrated integrated DPWM circuit with a fast delay- locking mechanism suitable for frequency hopping and having a current draw of only 16 μA/MHz presented in [18] can be used in conjunction with the proposed spread spectrum technique.

B. Design Considerations

The main design parameters are the desired center switching frequency f_0, the averaging time used by the applicable EMC test standard $\Delta t_{\rm avg}$ and the tolerable spread spectrum bandwidth BW, all of which are highly application dependent. The frequency range $(f_0 - BW/2) < f_s < (f_0 + BW/2)$ is divided into 2^l bins of $\Delta f = BW/2^l$. The average EMI is clearly reduced as l increases, reaching a minimum when neighboring frequency bins are indistinguishable due to limited spectral purity of the system clock. The number of cascaded delay elements in the self-oscillating DPWM, as dictated by the DPWM resolution, and the LDO noise both strongly affect the jitter in clk_{sys} and hence dictate its spectral purity. In turn, this puts a practical upper limit on l and the achievable reduction in EMI for a given bandwidth BW allocation. In this work, it was found experimentally that practical values of l range from 5-7 b for 20%$< BW/f_0 <$50%. The DAC input bus width j should be at least one bit larger than l to allow a flexible choice of offset in order to position $V_{dd,dl}$ within the allowable range and to avoid saturation inside the $\Delta\Sigma$ modulator. The DAC oversampling ratio is set by the m-bit clock divider inside the pattern generator block; OSR$= 2^m$. Using a 1-b $\Delta\Sigma$ DAC reduces the system complexity and results in a high-linearity $V_{\rm ref\_freq}$; m is therefore chosen to achieve sufficient SNR from the DAC for a given input resolution $j > l$.

The time slot spent at each frequency is $\Delta t_{ss} = 2^m/f_s \propto 1/V_{dd,dl}$. The total period of the repetitive pattern of $V_{dd,dl}$ and f_s can be calculated by summing $\Delta t_{ss}(V_{dd,dl})$ over the discrete range of $V_{dd,dl}$

$$\Delta T_f = 2^{k-l} \sum_{i=0}^{2^l-1} \Delta t_{ss} \left(V_{\rm min} + \Delta V \frac{i}{2^{l-1}} \right) \tag{1}$$

where k is the number of elements in the LFSR, $V_{\rm min}$ and $V_{\rm min}+\Delta V$ are the delay-line supply voltages corresponding to $f_s = f_0 - BW/2$ and $f_s = f_0 + BW/2$, respectively. For effective averaging, the total period of the pseudo-random pattern T_f should exceed $\Delta t_{\rm avg}$. For a given l, BW, m and f_0, k is obtained from (1) by setting $\Delta T_f > \Delta t_{\rm avg}$, where the relationship between $V_{dd,dl}$ and Δt_{ss} is obtained either from simulations or experimental characterization.

The pattern generator clock is derived from the variable-frequency system clock. This implies that the time interval for each target frequency Δt_{ss} varies with the frequency itself, as shown in Section V. As a result, while the target frequency is uniformly distributed, the actual switching frequency will not be uniformly distributed in time, leading to a less than ideal spreading of the noise spectrum [19]. Excellent noise reduction can be achieved despite the deviation from a uniformly distributed frequency caused by the variable system clock rate, as demonstrated in Section V. As a result, no attempt was made to correct for this effect. If the resulting average EMI does not meet target specifications for a given application, a uniform frequency distribution can also be achieved by using a fixed frequency clock for the pattern generator derived from an additional oscillator. Alternatively, the clock divider ratio in Fig. 2 can be modified on-the-fly to account for the predictable frequency variation of $\rm clk_{sys}$. Both of these options would increase the system cost and complexity.

III. Compensator Design Guidelines

The compensation of a digitally controlled SMPS under spread spectrum operation requires special consideration due to the resulting time-varying control law. This issue does not occur with analog compensators since the controller transfer function is fixed by passive components and/or transconductances, independent of the switching frequency. The digital PID compensator, whose difference equation is given by (2), is popular for low-power designs due to its simplicity and ease of implementation

$$d[n] = d[n-1] + K_{\rm adj}\left(C_0 e[n] + C_1 e[n-1] + C_2 e[n-2]\right) \tag{2}$$

where $d[n]$ is the duty cycle command, $e[n]$ is the error signal, $K_{\rm adj}$ is a loop-gain adjustment coefficient and C_{0-2} are the discrete compensator coefficients. While so-called direct-digital/nonlinear controller design is gaining popularity for improved response, analyzing the digital PID compensator using an equivalent continuous time model is more intuitive for the spread spectrum system. In the following discussion it is assumed that the digital compensator is clocked at the switching frequency f_s, which is most often the case

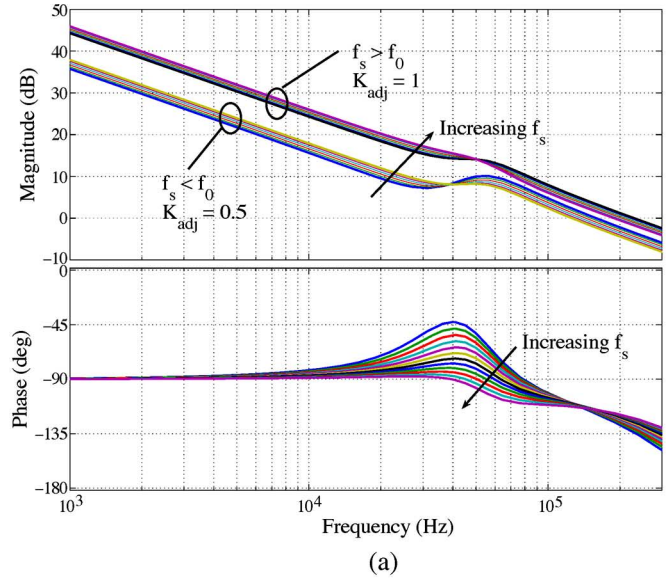
$$d[n] = d[n-1] + K\left(e[n] - 2r \cdot cos\left(2\pi\frac{f_z}{f_s}\right) \cdot e[n-1] + r^2 e[n-2]\right) \tag{3}$$

$$r = exp\left(-\frac{\pi f_z}{Q_z f_s}\right). \tag{4}$$

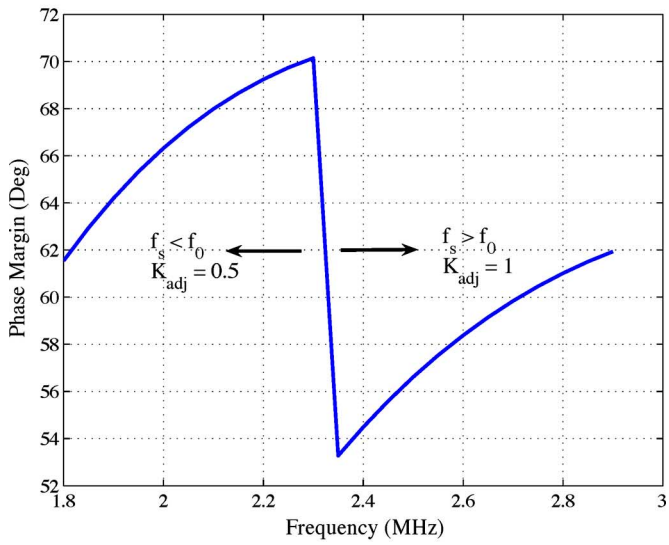
The correlation between the discrete coefficients of (2) in discrete-time and the equivalent continuous-time compensation zeroes' characteristics (Q_z and f_z) is given by (3) using the pole-zero matching technique, where r is given by (4).

The change in switching frequency occurs only once every $2^m >$100 switching cycles, and therefore it is safe to assume that the system will reach steady-state within each time-slot. As a result, a separate linear model is used within each time-slot where the switching frequency is constant. The three coefficients in (2) are derived from the optimized continuous-time compensator using pole-zero matching [20]. The main focus here is the effect of varying the switching frequency on the control-loop response. Due to practical limitations in low-power designs, the digital PID compensator generally has fixed coefficients C_{0-2}, which are usually hard-coded into area efficient lookup tables [20]. From (2) and (3), it is clear that the combination of fixed coefficients C_{0-2} and variable switching frequency f_s causes an undesirable shift in f_z, resulting in imperfect cancellation of the converter's fixed frequency complex poles at $f_p = 1/(2\pi\sqrt{LC})$.

At low f_s, f_z is shifted below f_p, causing the magnitude response to increase, pushing the cross-over frequency f_c beyond the nominal value and reducing the phase-margin. The



(a)



(b)

Fig. 3. (a) Magnitude and phase of the digitally compensated system for different switching frequencies. The variation in the digital compensator clock frequency shifts the complex zero location and damping affecting system dynamics. (b) Phase-margin versus switching frequency for the digitally compensated system with an adjustable loop gain $K_{\rm adj}$.

following procedure can be used to maintain good transient response for the entire spread spectrum operating range:

1) C_{0-2} are chosen to place f_z just above f_p at the maximum switching frequency $f_s = f_0 + BW/2$;
2) $K_{\rm adj} = (1/2)(-6$ dB) is used for $f_s \leq f_0$ and $K_{\rm adj} = 1$ for $f_s > f_0$ to reduce the spread in f_s/f_c.

The on-the-fly gain adjustment $K_{\rm adj}$ is easily achieved using a simple bit shift within the compensator based on the most significant bit of $freq_{ss}$. The frequency response of the compensated system with $V_g = 3.6$ V, $V_{\rm out} = 1.8$ V, $L = 2$ μH and $C_{\rm out} = 4.7$ μF is shown in Fig. 3(a) for switching frequencies ranging from 1.74 to 2.84 MHz. The phase-margin versus switching frequency is shown in Fig. 3(b). The use of $K_{\rm adj}$ allows the phase-margin to stay within an acceptable range, without sacrificing the control bandwidth f_c for high switching frequencies.

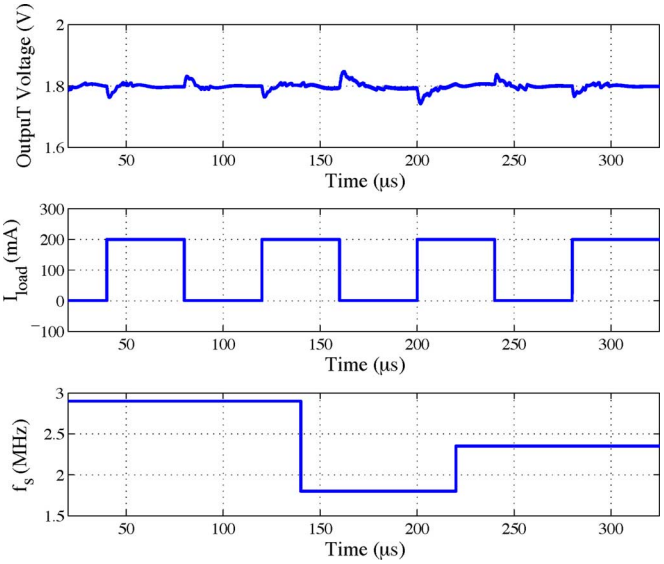


Fig. 4. Transient simulation showing the converter dynamic response for a 1–200 mA load step at three different switching frequencies. In a practical system, the slew-rate of f_s is set by the LDO settling time.

The effect of a 1–200 mA load step for three switching frequencies covering the full range was simulated using MATLAB/Simulink to verify the system transient response, as shown in Fig. 4. The synchronous buck power-stage operation is modeled using switches having a finite on-resistance, output capacitance and body-diodes. The inductor and capacitor ESR are included in the power-stage model, as well as finite dead-time. The system damping varies with the switching frequency, as predicted by the phase-margin plot of Fig. 3(b). Clearly, increasing the relative spread BW/f_0 makes the compensator design more challenging. If the gain scaling technique described above does not result in satisfactory phase-margin due to a large BW/f_0, a compensator with adaptive coefficients should be used, at the cost of additional silicon area.

IV. Implementation of the Spread Spectrum Prototype

A proof-of-concept prototype of the proposed spread spectrum system was implemented using a combination of off-the-shelf analog ICs, a complex programmable logic device (CPLD) and a custom power-stage IC. The power-stage IC, which is fabricated in 0.6-μm CMOS technology, includes a high-speed power MOSFET half-bridge and gate-drivers. The architecture shown in Fig. 2(b) was used to accommodate an off-chip LDO IC. The LDO has an internal 1.22 V reference, V_{ldo}, and is controlled by the buffered DAC output. The buffer and potentiometer would not be required in a fully integrated implementation since the internal LDO reference could be adjusted directly. The DAC is implemented using the simple first order $\Delta\Sigma$ modulator and a first-order passive RC filter. This circuit topology operates over a wide range of input voltages, V_g and provides a low-noise supply voltage for the delay-line DPWM. The delay-line supply voltage is given by

$$V_{dd,dl} = V_{ldo}\frac{R_1 + R_2}{R_1} - V_{\rm ref\_freq}\frac{R_2}{R_1}. \qquad (5)$$

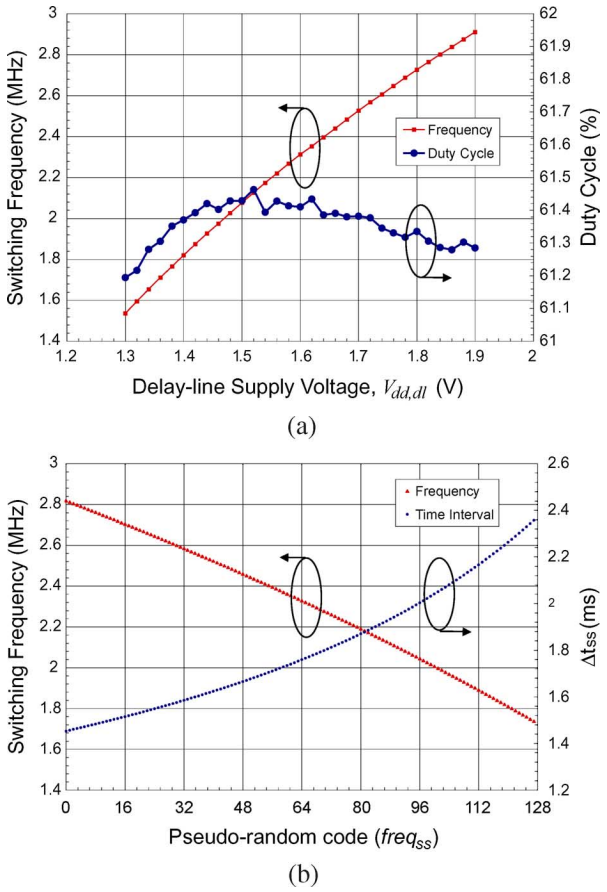


Fig. 5. (a) Measured variation of the switching frequency and effective duty cycle with delay-line supply voltage. (b) Frequency and corresponding time slot versus 7-b frequency target code.

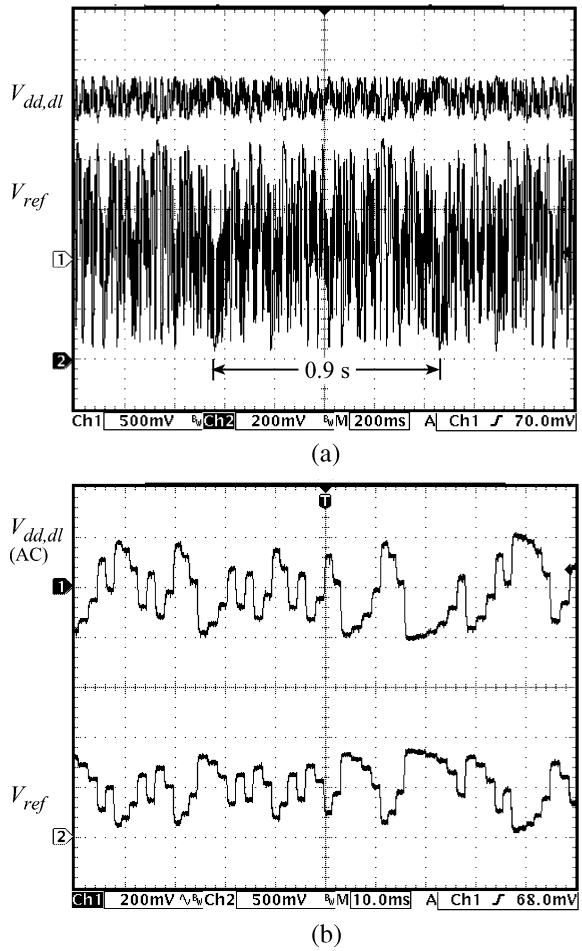


Fig. 6. (a) Waveforms of the buffered DAC output (channel 2) and delay-line supply voltage (channel 1) when the system operates in spread spectrum mode. (b) The same waveforms are shown with a reduced 10 ms/div time scale and $V_{dd,dl}$ is ac-coupled.

V. Experimental Results

The frequency parameters $f_0 = 2.3$ MHz, and $BW/f_0 = 0.48$ were used in the experimental prototype. Following the procedure described in Section II, the spread spectrum system was designed with $j = 10$, $k = 9$, $l = 7$, $m = 12$, and $p = 7$ with respect to Fig. 2(a). The frequency versus supply voltage of the 7-b DPWM block is shown in Fig. 5(a). The frequency changes from 1.74 to 2.84 MHz for a 480 mV change in $V_{dd,dl}$. The DPWM pulse width tracks the period variation, resulting in a nearly constant effective duty-cycle. The duty cycle varies by less than 0.3% over the operating range. The time slot during which the converter operates at a constant frequency, Δt_{ss}, is plotted versus the 7-b target frequency code, $freq_{ss}$, in Fig. 5(b). The Δt_{ss} ranges from 1.45 ms at the maximum switching frequency to 2.35 ms at the minimum switching frequency. This gives $\Delta T_f = 924$ ms for $l = 7$, $k = 9$ and the Δt_{ss} given in Fig. 5(b).

The DAC output and resulting delay-line supply voltage waveforms are shown in Fig. 6(a) and (b). The digitally generated pseudo-random sequence has a period of approximately 900 ms, which is very close to the $\Delta T_f = 924$ ms predicted by (1). The time-varying inductor current ripple due to spread spectrum operation is shown in Fig. 7. The reduction in efficiency with spread spectrum enabled was found to be below 0.1% with a 200 mA output current, compared to fixed frequency operation.

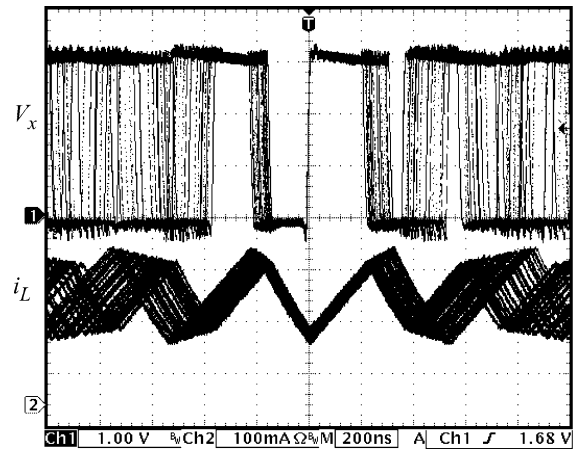
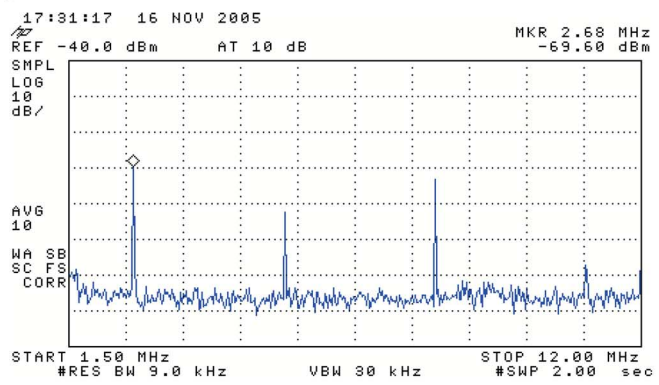
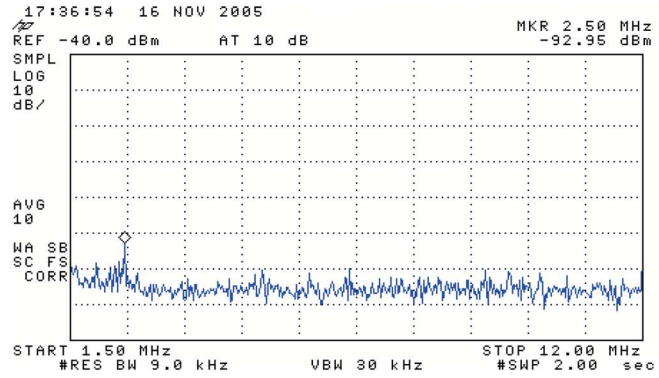


Fig. 7. Switching node voltage and inductor current during spread spectrum operation.

A current probe (TCP312+TCPA300) and spectrum analyzer (HP8591E) were used to measure the converter input current spectrum. A linear scan from 1.5 to 12 MHz was used with a



(a)



(b)

Fig. 8. (a) Averaged EMI spectrum of the input current to the dc–dc converter with fixed frequency and (b) with the spread spectrum enabled.

sweep time of 2 s, a resolution bandwidth of 9 kHz and a video bandwidth of 30 kHz. The measured input current's time-averaged spectrum with and without the spread spectrum mode enabled is shown in Fig. 8(a) and (b), respectively. Using the proposed architecture with custom designed integrated power-stage IC, the peak at f_s is reduced by 23.4 dB at a load current of 0.2 A, $V_g = 3.3$ V, $V_{\text{out}} = 1.8$ V, $L = 2$ μH and $C_{\text{out}} = 4.7$ μF.

VI. Conclusion

A spread spectrum architecture suitable for monolithic integration with advanced delay-line DPWM low-power digital controllers has been demonstrated. To reduce average EMI over a predefined digitally controllable range, the supply voltage of a DPWM is changed in a pseudo-random fashion, resulting in the change of switching frequency. Unlike with analog controllers, the compensator zeros of the proposed system are pseudo-randomly shifted as well. To minimize this effect, PID compensator design guidelines are given. The architecture is successfully verified with a digitally controlled 1.8-V, 0.5-W buck converter prototype. By changing the switching frequency between 1.74 and 2.84 MHz, a 23-dB reduction in the conducted EMI peak is achieved, while the converter efficiency is degraded by only 0.1%, compared to that of the constant switching frequency case.

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