Compensator Design and Stability Assessment for Fast Voltage Loops of Power Factor Correction Rectifiers

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***Abstract*—This paper introduces a new method for stability analysis and design of fast voltage-loop compensators in rectifiers with power factor correction (PFC). The method has few constraints and can be used with various implementations of the fast voltage loop. It is based on utilization of circle criterion, which unifies frequency domain and nonlinear system analysis. A step-by-step procedure of stability assessment and compensator design is described and demonstrated on two controller implementations. In the first system, the voltage-loop dynamic response of an experimental 200-W digitally-controlled boost-based PFC is improved with a self-tuning comb filter. In the second implementation, it is shown how the circle criterion can be used to design a fast voltage loop for controllers with regulation band, i.e., "dead-zone," element for ripple elimination.**

***Index Terms*—Circle criterion, fast voltage loop, power factor correction (PFC).**

I. Introduction

A CONVENTIONAL power factor correction (PFC) rectifier based on a high-frequency switching power converter consists of a power stage controlled by two interconnected feedback loops: a wide bandwidth current loop and a slower voltage loop. The task of the current loop is to make the input port of the PFC behave as an emulated resistor. This is accomplished by forcing the input current of the PFC to follow the waveshape of the rectified input voltage. The voltage loop keeps its output regulated by changing the ratio between line voltage and input current, i.e., through the variation of emulated resistance R_e.

A block diagram of an average-current controlled PFC and its large-signal model [1], [2] are shown in Fig. 1. In the model, the current loop is replaced with a "lossless" emulated resistor R_e and a controlled power source, whose average power over one converter switching cycle $T_s = 1/f_s$ is

$$\langle p_{\rm ac}(t)\rangle_{T_s} = \frac{V_g^2 \sin^2(\omega_L t)}{R_e} = \frac{V_g^2}{2R_e}(1-\cos(2\omega_L t)) \qquad (1)$$

where V_g is the peak value of the input line voltage and $f_L = \omega_L/(2\pi)$ is its frequency. Since this power has dc and ac components, a ripple at twice the line frequency (and its harmonics) occurs across the output filter capacitor C. The voltage loop cannot attempt to remove the ripple. This would cause the emulated resistance to change at a frequency higher than the line frequency, and consequently introduce a significant distortion of the input current waveform [1], [3].

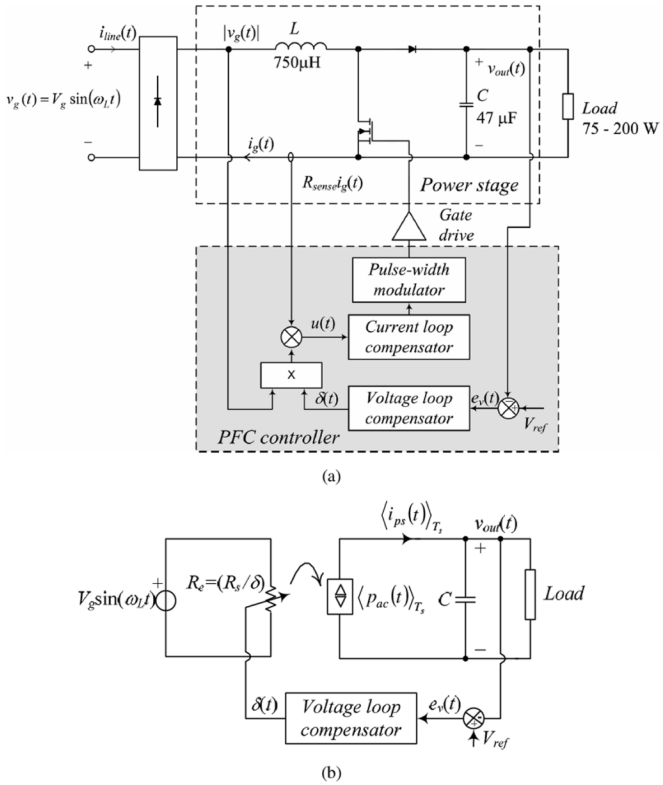

Fig. 1. Power factor correction rectifier: (a) block diagram and (b) large-signal model of the voltage loop.

Commonly, the ripple influence is minimized by limiting the bandwidth of the voltage loop to a frequency significantly lower than the ripple frequency, typically 10 to 20 Hz. As a result, the compensator behaves as a low-pass filter strongly suppressing the ripple component. The main shortcoming of this approach is a slow response to disturbances in the circuit. The disturbances can cause large voltage drops and overshoots imposing additional stress on the PFC components, as well as on its downstream dc-to-dc converter. Consequently, in most realizations, both the PFC and the downstream stage are over-designed, both in the terms of the size and voltage/current ratings of their components.

Various methods have been proposed to improve the dynamic response without allowing propagation of the ripple through voltage loop. They include ripple cancellation [4]–[8], regulation

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band, and "dead-zone" circuits [4]–[6], [9], [10]. In the cancellation techniques, the ripple is eliminated by modifying the voltage reference $V_{\rm ref}$ (see Fig. 1) with a component having the same amplitude and opposite sign of the sensed voltage ripple. The operation of regulation band and dead-zone controllers depends on the amplitude of the voltage-loop error signal $e_v(t)$. For small errors, approximately equal to the ripple magnitude, the loop is either slow [6], [9] or completely insensitive to voltage variations [10]. During transients, when the error is large, the voltage-loop compensator operates in a fast mode improving response time. Filtering techniques usually use a notch [5], [6], [11] or a comb filter [12] to eliminate the ripple. In digital implementations, filters can be made self-adjustable [12] to accommodate changes in line frequency. Compared to traditional solutions, all of these techniques show large improvements of voltage-loop transient response and a potential for significant reduction in the size and power ratings of converter components.

Even though effective methods for improvement of the voltage-loop dynamics have been developed, the conventional low-bandwidth design of the voltage loop is still predominant. This is largely due to unresolved controller design issues. The problem is that a fast voltage loop behaves as a time-varying nonlinear system for which traditional linear compensator design and stability analysis techniques usually cannot be used. Consequently, in most of the cases the stability of the loop cannot be guaranteed for all operating conditions. In [5], [8], and [13]–[15] the authors presented stability analysis and compensator design methods whose applications are limited to just a few fast controller realizations.

The main goal of this paper is to show a new universal method for the stability analysis and the design of fast voltage-loop compensator that can be used with most of the existing ripple influence elimination techniques. The proposed method is based on the circle criterion [16] and gives guarantees for a stable operation of the fast voltage loop under all operating conditions. The method has some similarities with the Nyquist plane based small-signal stability criteria developed for multiple dc-dc converter systems [17]–[22]. However, it does not require signals to be small and, consequently, can be used in PFC applications where, as shown in Fig. 1(b), large variations of the input voltage exist.

The paper is organized as follows. The nonlinear time-varying nature of the fast voltage loop is described in the following section and limitations of previous modeling approaches are pointed out. Section III gives an introduction to the circle criterion and shows the stability analysis and controller design procedure. Two design examples demonstrating how the circle criterion can be applied for the design of fast voltage loops in systems having comb/notch filters and a dead-zone element are given in Section IV. Section V presents simulations and experimental results verifying validity of the proposed compensator design method.

II. Time-Varying Nonlinear Nature of the Fast Voltage Loop

The nonlinear time-varying nature of the system shown in Fig. 1 comes from the fact that the output voltage has a square root dependence on the instantaneous power from the power source [1], which changes in time, at twice the line frequency. In addition, the relation between emulated resistance R_e and the voltage-loop compensator output signal $\delta(t)$ is also nonlinear. The emulated resistance is inversely proportional to the control signal $R_e = (R_s/\delta)$, where R_s is a constant that depends on the gain of the sensor for the input current measurement.

For fast voltage loops, conventional modeling method used for the design of low-bandwidth loops cannot be applied. It is based on averaging over a half of the line period followed by a linearization of the resulting large-signal averaged model [1], [3]. The averaging step eliminates signals at frequencies higher than twice the line frequency, thus removing crucial control signal components that make fast voltage regulation possible.

Previous attempts to address the problem mainly focus on ripple cancellation methods [8]. In [5] a "transfer function" having time varying terms was introduced and the use of a linear PI compensator was proposed. This model lacks mathematical accuracy since it introduces time-varying terms in system transfer functions. More accurate small-signal models are proposed in [14], [15]. The modeling approach shown in [15] replaces the input voltage source of Fig. 1 with its root-mean square value to obtain a system transfer function. Large-signal time-domain models and control methods are presented in [8], [13]. They are based on the analysis of energy balance in the time domain and regulation of the squared value of the output voltage $v_{\rm out}^2(t)$.

One of the main limitations of all of the abovementioned methods is that they are not directly applicable for the loops containing dead-zone or regulation band circuits, whose realization generally requires much simpler hardware. The fast controllers of these circuits are usually not active in steady state and only start operating when a large disturbance occurs. Since small-signal assumption is not completely valid in such situation, stable system operation cannot be guaranteed. On the other hand, as will be discussed in Section IV-B in more details, $v_{\rm out}^2(t)$-based controlling approach suffers from regulation problem when a dead-zone element is used.

The proposed methods cannot easily be used in the loops with notch and comb filters either. The filters strongly suppress the component at ripple frequency and, in the case of a comb, its harmonics as well. This results in the loop gain magnitude characteristic with multiple zero crossings for which Bode plots-based stability analysis cannot be directly applied. On the other hand, time-domain analysis [8], [13] of the systems having higher order filters is impractical.

III. Circle Criterion

The *circle criterion*, introduced by Zames [16], is a method for the analysis of nonlinear time-varying systems that gives a sufficient condition for closed loop system stability. It provides a link between the tools for nonlinear system analysis and the transfer function methods used in linear control theory. In this section, we summarize the main results of the circle criterion that are used in the stability analysis and controller design method proposed in this paper.

A general block of the system under consideration is shown in Fig. 2. It consists of a linear-time invariant element with transfer function $H(s)$, and a time-varying nonlinear block $N(x,t)$.

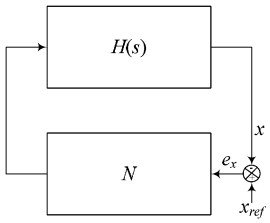


Fig. 2. General block diagram of a time-varying nonlinear system.

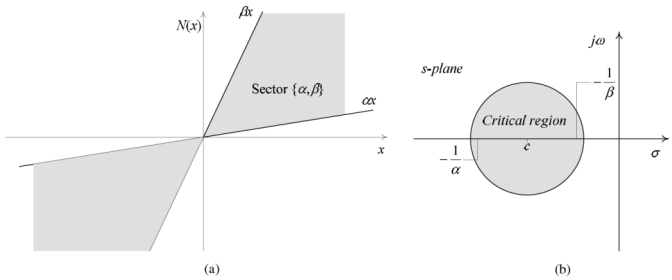


Fig. 3. Basic elements of circle-criteria-based stability analysis: (a) sector $\{\alpha, \beta\}$ and (b) corresponding critical circle.

In accordance with the cycle criterion, stability of this closed-loop system is assessed via three main steps.

- First, as shown in Fig. 3(a), in the input-to-output plane the nonlinear element, $N(x)$, is bounded with a sector $\{\alpha, \beta\}$. The sector consists of the area in between two straight lines αx and βx, that for each input x satisfy the following equation:

$$\alpha x < N(x) < \beta x, \tag{2}$$

  where both α and β are positive real numbers.
- Next, the sector's counterpart is defined in the complex plane (s-plane). In this way the plane is divided into stable area and a *critical region*, which, as shown in Fig. 3(b), is usually a disk whose center is right in between the points $-1/\alpha$ and $-1/\beta$. When $\alpha = 0$, the disk transforms into the half-plane spreading left from the vertical line $\sigma = -1/\beta$.
- Finally, the frequency response of the linear time-invariant element $H(s)$ is plotted in the complex plane, i.e., a Nyquist plot is drawn, and the stability of the system is assessed. *It is assumed that the system is stable if the Nyquist plot avoids the critical region and does not encircle it.*

A. Multiple Nonlinearities, Product Sector, and Transformed Multiplier

The previously stated criterion gives sufficient stability condition for practically any type of nonlinearity. However, due to its very general nature, it also results in overly conservative estimation of the critical region's size and, consequently, limits the compensator design options. When certain restrictions on the nonlinear element are applied, the size of the critical region can be significantly reduced. In particular, this occurs, when a time-varying element $N(x,t)$ causes multiple nonlinear effects and when its "gain" varies at a limited rate, i.e., is *instantaneously incremental inside a sector* $\{\alpha, \beta\}$. As we will see soon, these conditions apply for the PFC system under consideration

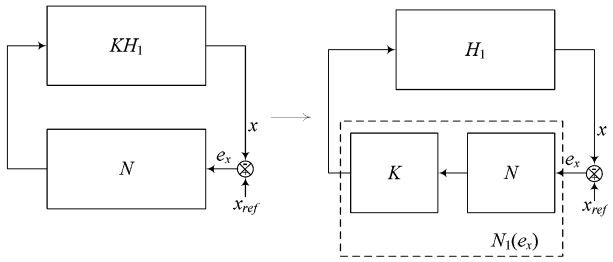


Fig. 4. Transformation of multipliers, i.e., rearrangement of the feedback loop elements.

and, as such, are of special interest for us. From the mathematical point of view, it is assumed that $N(x,t)$ is instantaneously incremental inside the sector $\{\alpha, \beta\}$ if for any two inputs x_1, x_2, and corresponding time instants t_1 and t_2, the condition

$$\alpha \leq \frac{[N(x_2,t_2) - N(x_1,t_1)]}{x_2 - x_1} \leq \beta \tag{3}$$

is satisfied. To analyze multiple nonlinearities, the circle criterion utilizes a *product sector*. A nonlinearity $N_2(N_1(x,t))$, comprising of two effects $N_1(x,t)$ and $N_2(x,t)$, bounded by sectors $\{\alpha_1, \beta_1\}$ and $\{\alpha_2, \beta_2\}$, respectively, is inside the product sector $\{\alpha, \beta\} = \{\alpha_1, \beta_1\} \times \{\alpha_2, \beta_2\}$. Where $\{\alpha, \beta\}$ is defined with the interval of real numbers

$$[\alpha, \beta] = \{xy, x \in [\alpha_1, \beta_1] \text{ and } y \in [\alpha_2, \beta_2]\} \tag{4}$$

i.e., it is the point-wise product of the corresponding intervals. As it can be seen from (3) and (4), the multiple nonlinearities change the size of $\{\alpha, \beta\}$, and can result in less conservative estimation of the critical region.

Often, the size of the critical disc can be further reduced when $N(x,t)$ is incrementally inside the section $\{\alpha, \beta\}$ and when the linear part of the system of Fig. 3 is represented as

$$H(s) = H_1(s)K(s), \tag{5}$$

where $K(s)$ behaves as a first order low-pass filter, i.e., $K(s) = K/(1 + s/\omega_p)$. The coefficients K and ω_p are the gain and the corner frequency of the filter, respectively. In that case, $N(x,t)$ can be combined with $K(s)$, as shown in Fig. 4, to form a new nonlinear element $N_1(x,t)$. This element is bounded with product sector $\{\alpha, \beta\} \times \{K(\infty), K(0)\}$, where $K(\infty)$ and $K(0)$ denote the gain of $K(j\omega)$ for the two extreme frequencies. This rearrangement is called *transformation of multipliers*. In the next section, we will see how this property can be used to reduce complexity of a high-order linear system and simplify the fast voltage-loop compensator design.

IV. Stability Analysis and Compensator Design Based on the Circle Criterion

This section shows how the circle criterion can be used for the assessment of the voltage loop's stability and for the design of a linear compensator that provides a fast dynamic response. The versatility of the design method is demonstrated on two examples. In the first example, the expansion of the voltage-loop bandwidth of a digitally controlled universal PFC rectifier is enabled using a self-tuning digital comb filter (STCF) [12]. In

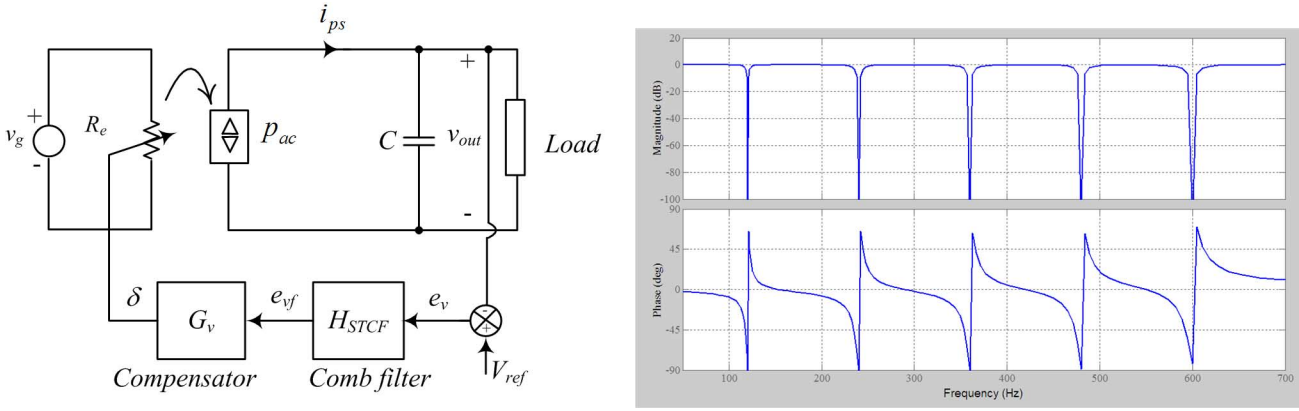
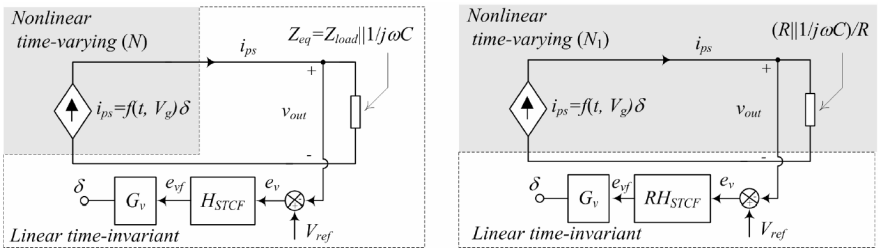


Fig. 5. Fast voltage loop with a self-tuning comb filter: (a) large-signal mode and (b) amplitude and phase characteristics of the filter loop compensator.



(a) (b)

Fig. 6. Separation of the PFC's voltage loop into nonlinear and linear parts: (a) initial step and (b) after the transformation of multipliers is applied.

the second example, the expansion is made possible though the utilization of the dead-zone, i.e., regulation band, method [4], [9], [10].

For the both cases, the design procedure is a three-stage process:

i first, a separation of the system into a nonlinear and a linear parts is performed;

ii next, the critical sector and corresponding critical region are defined;

iii finally, through compensator design, the Nyquist plot of the linear part is shaped to avoid the critical region and provide fast dynamic response of the system.

The resulting controllers are guaranteed stable for all operating conditions and provide a fast response of the system.

A. Fast Voltage Loop With STCF

A large-signal model of the system under consideration is illustrated in Fig. 5(a). In this case, a self-tuning comb filter (STCF) for ripple elimination is inserted in the loop before the voltage compensator $G_v(s)$. The amplitude and phase characteristics of a comb filter are shown in Fig. 5(b). Its magnitude exhibits total attenuation at equally spaced frequency points, called notches, and has unity gain at all other frequencies. The STCF examines the output voltage ripple and, based on its amplitude, automatically tunes notches of an internal comb filter to match twice the line frequency and its harmonics. In that way, a ripple-free error signal $e_{\rm vf}(t)$ for the voltage-loop compensator is provided. The system significantly improves dynamic characteristics of the voltage loop but at the same time makes stability analysis more complicated. In addition to the previously mentioned problems of time-varying gain (1) and nonlinear dependence on the control variable$\delta(t)$, the comb filter causes multiple-zero crossings of the loop-gain magnitude characteristic.

In [12], the "*frozen coefficients*" method [22] is applied to design a fast voltage-loop compensator for this system. The system is "frozen" at the operating point considered to be the worst operating condition. Even though this method usually results in good controller performance, it does not give any guarantee for the stability of the system in all operating conditions [22]. On the other hand, neither the time-domain compensator design proposed in [8] nor Bode plot-based methods [14], [15] can be simply applied. The high order of this filter makes the time domain analysis complicated and its multiple zero crossings invalidate stability assessment based on the phase and amplitude margin concept of conventional linear control theory.

Here, it is shown that by following the three-step, design procedure described at the beginning of this section a fast compensator can be designed and stability of the system verified for all operating conditions.

1) System Separation: In order to analyze the system and obtain a structure similar to the one depicted in Fig. 2, the system of Fig. 5(a) is redrawn and separated into linear and nonlinear parts, as shown in Fig. 6(a).

The nonlinear time-varying part N is obtained by replacing the power source at the input port with a dependent current source, whose output is controlled by signal $\delta(t)$ and has average value over one switching cycle of

$$\langle i_{\rm PS}(t)\rangle_{T_S} = \frac{\langle p(t)\rangle_{Ts}}{V_{\rm out}} \tag{6}$$

$$\langle i_{\rm PS}(t)\rangle_{T_S} = \frac{V_g^2\sin^2(\omega_L t)}{R_e V_{\rm out}} = \frac{V_g^2\sin^2(\omega_L t)}{R_S V_{\rm out}}\cdot\delta(t). \tag{7}$$

In this approximation, it is assumed that the dc value of the output voltage $V_{\rm out}$ is much larger than the ripple and that the instantaneous power from the input port $p(t)$ is equal to $\langle p(t)\rangle_{Ts}$, its own average value [1].

The linear part of the system comprises of a parallel connection of a load $Z_{\rm out}(s)$ and the output capacitor C, a voltage-loop compensator, and STCF. The transfer function of the STCF $H_{\rm STCF}(j\omega)$, is a continuous-time equivalent of the discrete expression

$$H_{\rm STCF}(z)=\frac{1-z^{-M}}{1-z^{-1}}\frac{1-(r\cdot z)^{-1}}{1-(r\cdot z)^{-M}} \tag{8}$$

obtained by replacing z with $e^{j\omega}$, where $\omega=2\pi f/f_s$ and f_s is the sampling frequency of the STCF [23].

2) Determination of the Critical Region: A critical sector that describes the nonlinear part of the system (the current source) is defined by two nonlinearities: a time-varying gain $\sin^2(\omega_L t)$ and a square dependence on V_g, which for universal-input PFC rectifiers can span a range of more than three to one (assuming that a feedforward [1] does not exist).

The critical sector for the first nonlinearity $\{\alpha_1,\beta_1\}$ is limited by the value of $\sin^2(\omega_L t)$, which varies between 0 and 1. Therefore, the sector $\{\alpha_1,\beta_1\}$ is $\{0,1\}$. The boundaries of the second sector are defined by the minimum and the maximum *rms* voltage values in universal-input PFC rectifiers ($V_{g\min}=90\ \mathrm{V_{rms}}$ and $V_{g\max}=260\ \mathrm{V_{rms}}$). Based on this, the second critical sector is

$$\{\alpha_2,\beta_2\}=\left\{\frac{2V_{g\min}^2}{R_s\mathrm{V_{out}}},\frac{2\mathrm{V}_{g\max}^2}{R_sV_{\rm out}}\right\}. \tag{9}$$

In accordance with the results given in Section III, the resulting sector of N, $\{\alpha_N,\beta_N\}$ can be described with the product sector

$$\{\alpha_N,\beta_N\}=\{\alpha_1,\beta_1\}\times\{\alpha_2,\beta_2\}=\left\{0,\frac{2V_{g\max}^2}{R_s\mathrm{V_{out}}}\right\}. \tag{10}$$

The counterpart of this sector, i.e., critical region, is a half-plane drawn in Fig. 7(a). On its right side, this plane is bounded by the vertical line passing through the point $(-(R_s\mathrm{V_{out}}/(2\ \mathrm{V}_{g\max}^2)),0)$. It should be noted that the methods for obtaining a less conservative estimation of the size of critical region, used in dc-dc converters [18]–[20], cannot be easily applied here. As described in [16], the size reduction requires a slope-restricted nonlinearity, meaning that the rate of change of signals in nonlinear and/or time varying components needs to be limited. Possible sudden changes in the amplitude of the input voltage make the calculation of such a slope uncertain and, if applied for the critical region reduction, could result in unstable system operation.

3) Stability Assessment and Voltage-Loop Compensator Design: Fig. 7(a) also shows the Nyquist plot of $H_{\rm STCF}(j\omega)(Z_{\rm out}(j\omega)||1/j\omega C)$ for the system of Fig. 1, i.e., linear part without compensator, under initial assumptions that $Z_{\rm out}(j\omega)$ is a pure resistance R, i.e.,

$$Z_{\rm out}\left|\left|\frac{1}{j\omega C}=R\right|\right|\frac{1}{j\omega C}=\frac{R}{1+j\omega RC}. \tag{11}$$

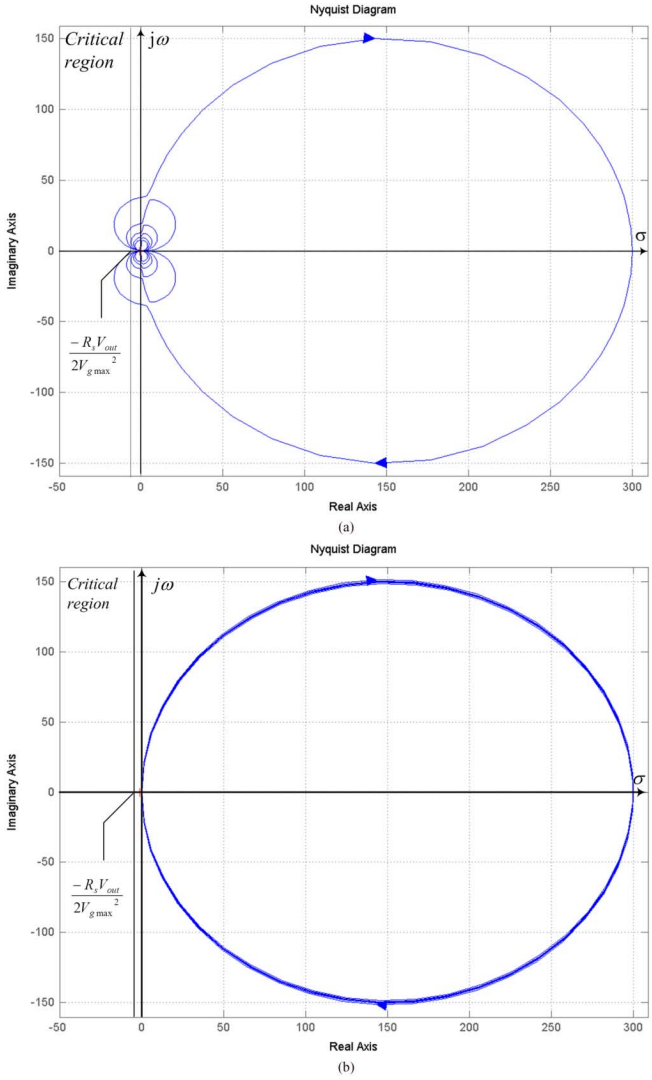


Fig. 7. Critical region and the Nyquist plot of the continuous part without compensator: (a) initial system; (b) system after the transformation of multiplier is applied.

It can be seen that the Nyquist plot enters the critical region, a sufficient stability condition is not satisfied, so nothing can be said about the system stability.

In this case, the main difficulty related to design of a voltage-loop compensator comes from the shape of Nyquist plot that has periodic excursion into the critical region. To eliminate this problem a transformation of multipliers, can be applied. In accordance with the procedure described in Section III-A, we transfer the denominator of (11) to the nonlinear portion of the system forming a new nonlinear part N_1. Then, the a new critical region and Nyquist plot for the remaining linear portion of the system, i.e., $RH_{\rm STCF}(j\omega)$, are drawn.

The transferred multiplier $1/(1+j\omega CR)$ is bounded by sector $\{1/(1+j\omega CR)_{\omega\to\infty},1/(1+j\omega CR)_{\omega\to 0}\}=\{0,1\}$. Hence, the resulting product sector of $N_1\{\alpha_{N1},\beta_{N1}\}=\{\alpha_N,\beta_N\}\times\{0,1\}$ is $\{\alpha_N,\beta_N\}$ (the critical region remains the same). However, the Nyquist plot of the new linear part, drawn in Fig. 7(b), becomes much simpler.

The voltage-loop compensator design is performed by having two goals in mind: first to avoid the critical region, and

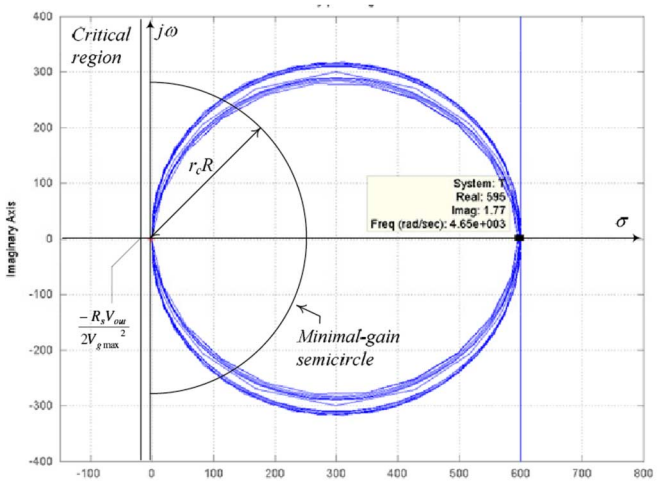


Fig. 8. Critical region and the Nyquist plot of the compensated system of Fig. 1. The voltage-loop compensator parameters (13) are $K_p = 2$, $f_z = 8$ Hz, and $f_p = 8$ kHz).

second to provide a fast response by keeping the "instantaneous loop gain" larger than one, during the largest portion of the line voltage period, specifically, during the period for which $v_g(t) = V_g \sin(\omega_L t) > V_g/\sqrt{2}$. Based on (6), (7), (8), and (11), the latter requirement can be satisfied by designing the compensator such that

$$||G_v(j\omega)||_{\omega=\omega_c} > \frac{4R_s \mathrm{V_{out}}}{V_{g\_\min}^2} \left|\left|\frac{1+j\omega RC}{R}\right|\right|_{\omega=\omega_c} = r_c \quad (12)$$

where $f_c = \omega_c/(2\pi)$ is selected to be higher than twice the line frequency. When $||G_v(j\omega)||$ is a monotonic function, this inequality coincides with requirement of having the Nyquist plot's point $\omega = \omega_c$ outside a semicircle with center at the origin and radius r_c. Note that based on Fig. 5(b), unity gain for the comb filter is assumed.

To satisfy the previous requirements, a simple PID compensator

$$G_v(s) = \frac{\delta(s)}{e_{\mathrm{vf}}(s)} = K_p \frac{1+\frac{\omega_z}{s}}{1+\frac{s}{\omega_p}} \quad (13)$$

is chosen and its gain K_p, and the frequencies of the zero $f_z = \omega_z/2\pi$ and pole $f_p = \omega_p/2\pi \gg f_z$ are adjusted accordingly. This type of compensator is selected because its pole at zero provides tight output voltage regulation and at higher frequencies behaves as a simple gain stage ensuring the Nyquist plot of Fig. 7(b) remains outside the critical region. To design the compensator, first the frequency of the zero is set to be significantly lower than the frequency of the lowest notch of the comb filter and the pole is set to be at a higher frequency than the highest notch. In the next step, the gain K_p is adjusted in accordance with (12). As can be seen in Fig. 8, showing the Nyquist plot of $G_v(j\omega)H_{\mathrm{STCF}}(j\omega)$, both stability and speed requirements are satisfied. The plot does not intersect critical region and for $f > 120$ Hz, it lies outside of the minimal-gain semicircle (the diagram shows point at $\omega = 4650$ rad/s, i.e., $f = 740$ Hz). In this case, due to the transformation of multipliers, the minimal gain semicircle is r_cR. Note that, since $f_p \gg f_z$, this result coincides with the analysis presented in [13], stating that a PI

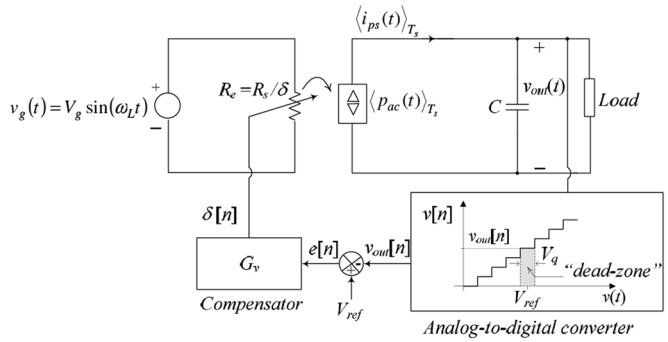


Fig. 9. Large-signal model of a PFC with a digital "dead-zone" voltage-loop controller.

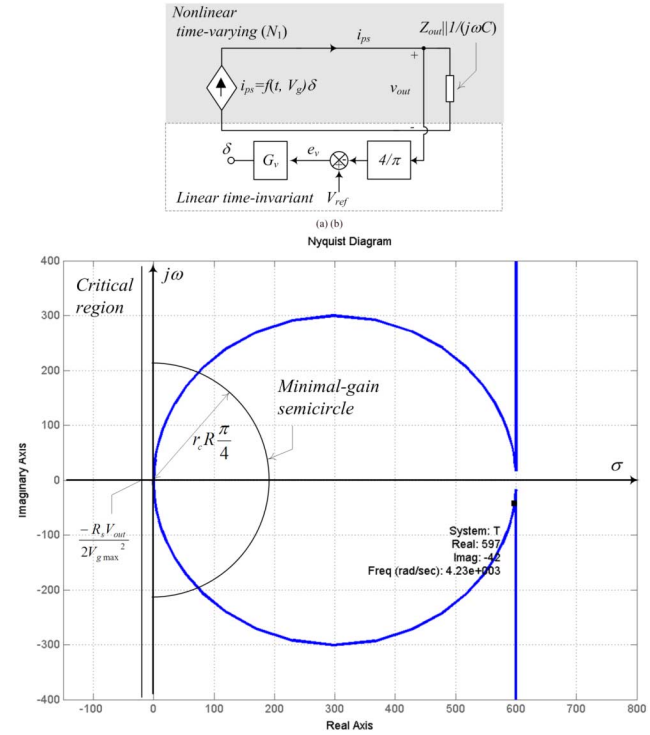


Fig. 10. Dead-zone voltage-loop controller: (a) large-signal model and (b) its complex plane representation. (The system of Fig. 1 with inserted dead-zone block is analyzed for $R = 300\,\Omega, \mathrm{V_{out}} = 385$ V, $C = 47\,\mu$F, and $R_s = 25\,\Omega$. The voltage-loop compensator parameters (13) are $K_p = 1.5$, $f_z = 8$ Hz, and $f_p = 8$ kHz).

compensator is a good choice for the regulation of the PFC's voltage loop.

4) Downstream Converter Load: Often, a PFC supplies a downstream dc-dc converter, having an input impedance $Z_{\mathrm{in}}(j\omega)$ and acting as a negative incremental resistance [17]–[21], [24], [25]. In that case, the equivalent impedance seen by the controlled current source of Fig. 6(a) becomes

$$Z_{\mathrm{eq}}(j\omega) = Z_{\mathrm{in}}(j\omega)\left|\left|\frac{1}{j\omega C}\right.\right. . \quad (14)$$

The analysis of this system can be simplified by taking the approach adopted in distributed power supplies (DPS), where it is assumed that the system is stable if the output impedance of a source is significantly smaller than the input impedance of its downstream converter [17]. Then, the compensator for

the source and the downstream converter can be constructed independently.

Accordingly, we assume that $||1/(j\omega C)|| \ll ||Z_{\rm in}(j\omega)||$, i.e., that $Z_{\rm eq}(j\omega) \cong 1/(j\omega C)$, and construct the voltage-loop compensator for this case. Note that, in most of the realistic PFCs, this assumption is valid, due to the relatively high value of the output capacitance, needed to satisfy hold-on time requirement [1]. Compared to the previous case, where a resistive load was assumed, the difference in the design procedures is minor. Here, a more conservative estimation for the critical region is obtained after the multiplier transformation is performed. The new critical region occupies the whole right half plane but, as it can be seen from Fig. 7(b) and 8, the system stability is unaffected. In this case, a radius $rR_{\rm dc}$ is used, where $R_{\rm dc} = {\rm V_{out}}/{\rm I_{out}}$ is the ratio of the dc values of the output voltage and current, equal to the dc input resistance of the downstream power stage [17], [25].

B. Fast Voltage-Loop Design for a "Dead-Zone" Controller

The versatility of the proposed control method is now demonstrated on a system in which the output voltage ripple elimination is achieved using the "dead-zone" controller [10] shown in Fig. 9. In this digital technique, which is similar to analog regulation band methods [4]–[6], [9], the voltage-loop dynamic improvement is achieved through the utilization of an insensitive ("dead") zone in analog to digital conversion. More specifically, the output capacitor ripple is eliminated by setting the quantization step of the analog-to-digital converter (ADC) V_q to be larger than the ripple magnitude.

The main advantage of this method over previous solutions is its very simple realization. It can be implemented with hardware as simple as the one used for conventional low-bandwidth PFCs or even with a simpler system, utilizing a less-expensive ADC. However, wider adoption of this method is hampered by two problems. First, the core-resolution ADC introduces an amplitude dependent gain. Secondly, fast voltage-loop compensator is active only upon a large disturbance causing significant change of the output voltage. In such conditions, the initial assumption used for small-signal models [14], [15], that the converter is in steady-state, is not valid. As a result, stability problems during mode transients often occur.

The circle criterion based method is not constrained to small-signal analysis. Hence, it gives us a more reliable voltage-loop design tool. To analyze this system we start from the equivalent model of the loop, presented in Fig. 9, where the ADC is replaced with a constant gain of $4/\pi$. This value is obtained from describing functions (DF) analysis [26], under assumption that the voltage-loop compensator contains an integrator that forces zero dc bias at the quantizer input. Then, the DF shows that the gain of the ADC varies between 0 and $4/\pi$, where the later value is taken as the worst case. A large-signal model and corresponding control method [8], [13] based on regulation of $v_{\rm out}^2(t)$ cannot be directly used either, since the voltage regulation would be compromised. In that case, to eliminate the ripple from error $e_v 2(t) \approx {\rm V_{ref}^2} - ({\rm V_{out}} + v_{\rm ripple}(t))^2$, a large dead-zone, proportional to the product of the dc output voltage and ripple magnitude, would be needed.

The following design steps, i.e., system separation and the transformation of multiplier, are performed in the same way as in the previously discussed STCF example and the equivalent system of Fig. 10(a) is obtained.

Because of the similarity in the design procedures, the critical region is the same and the only difference is in the compensator design. Now, as shown in Fig. 10(b), to account for the gain of the ADC, the radius of the minimum gain semi-circle is reduced to $\pi/4$ of its original size.

The absence of the comb filter makes the shape of the plot simpler. The problem is reduced to the design of a compensator that does not cause the Nyquist plot to cross to the left part of the complex plane while satisfying the speed requirements as well. Again, the compensator (13) is chosen, and its gain slightly modified to accommodate the new speed requirement, i.e., modified radius of the minimum-gain semicircle.

V. Simulations and Experimental Verification

The verification of the circle-criterion-based stability assessment and controller design method was performed both through simulations and experiments. For the simulations, a Matlab simulink tool was used. The power stage, a boost converter operating at 200-kHz switching frequency, and controllers were simulated using a modification of the real-time model with ideal switches presented in [27]. Experiments were performed with a digitally controlled 200-W boost-based PFC, operating at the same switching frequency. The output voltage was regulated at 385 V. The controller was implemented with an Analog Devices ADMC-401 DSP Evaluation board that allows simple implementation of both abovementioned controllers. The voltage-loop controllers were built based on the block diagrams given in Figs. 1, 5, and 9 and the other system parts are implemented as described in [10] and [12].

A. Simulation Results

Figs. 11–13 show simulation results for load-transient responses of an STCF voltage loop regulated by three different compensators.

The load-transient response of Fig. 11 is obtained with a compensator that is designed as described in Section IV-A, where, as shown in Fig. 8(b), both stability and speed requirements are met. It can be seen that upon the disturbance the output voltage and rectified line current settle down in few line cycles demonstrating the effectiveness of the compensator.

1) Unstable Operation: Figs. 12(a) and (b) show the case when the zero of compensator (13) is set in the vicinity of the first filter notch (≈80 Hz). As a result, the Nyquist plot of the linear part intersects the ctirical region, and the sufficent stability condition is not satisfied. As the diagram of Fig. 12.(a) shows, in this case the PFC system is not stable. It exhibits large variations of the input current and the output voltage.

2) Slow Compensator: Figs. 13(a) and (b) show the situation when the speed requirement is not satisfied, i.e., when the Nyquist plot's point at twice the line frequency is inside minimal-gain semicircle. The simultaions shows slow load-transient response characterized with large output voltage drops and overshoots.

3) Simulations With a Downstream Converter: Simulation results of the fast STCF controller for the case when the

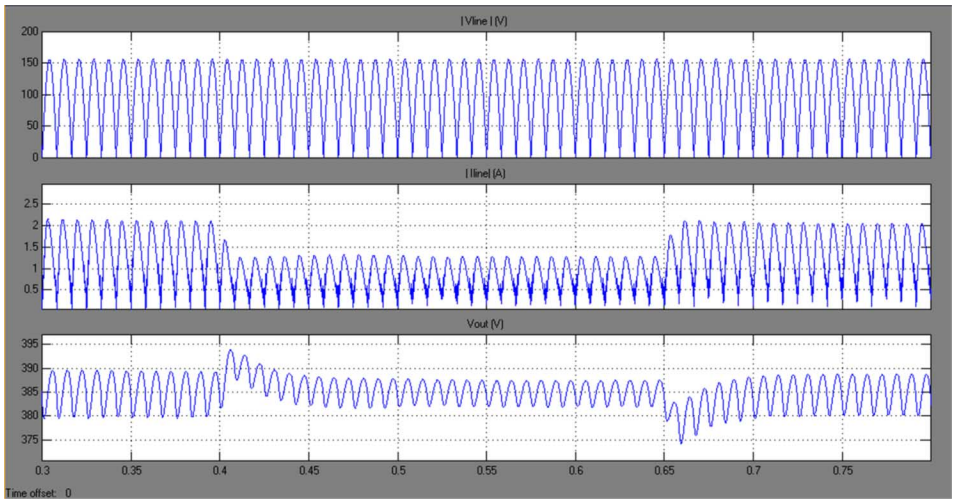


Fig. 11. Simulation results for the fast STCF controller when the load changes between 150 W and 175 W. Top waveform: rectified line voltage, middle: rectified input current, and bottom: PFC's output voltage. The time scale shows seconds.

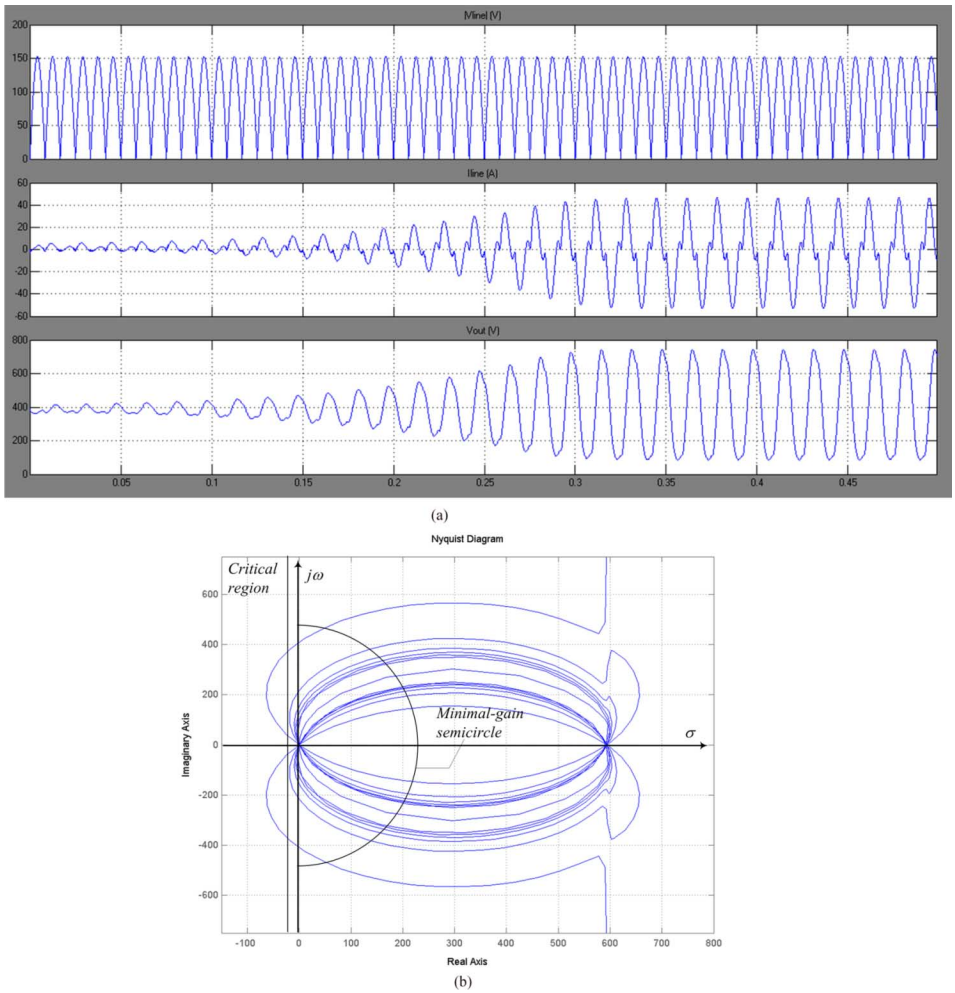
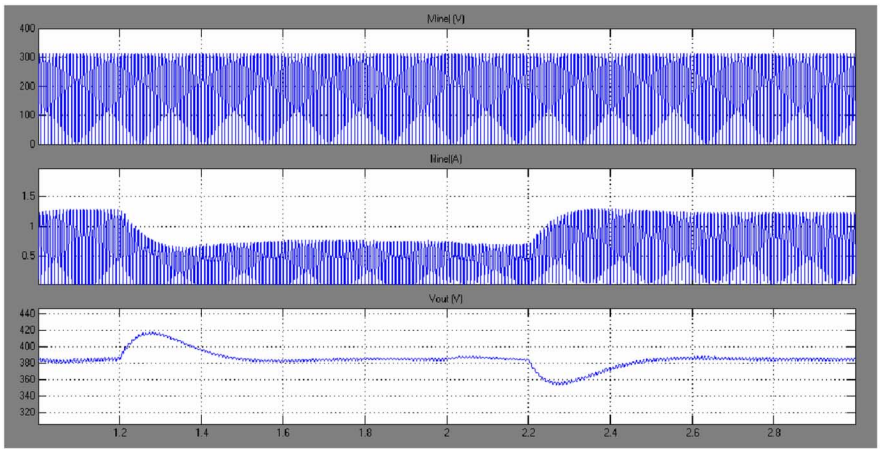


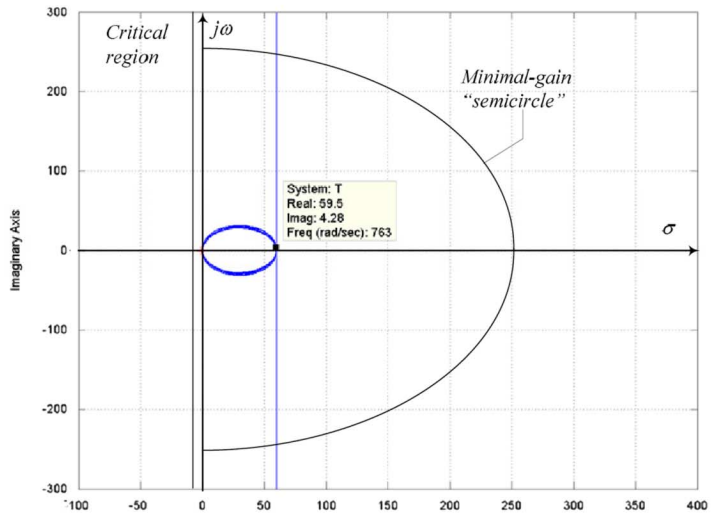
Fig. 12. Unstable operation of STCF controller. (a) Top: rectified line voltage. Middle: input line current. Bottom: output voltage. The time scale shows seconds. (b) Complex plane controller representation for $R = 300\ \Omega, \mathrm{V_{out}} = 385$ V, $C = 47\ \mu$F, and $R_s = 25\ \Omega$. The voltage-loop compensator parameters (13) are $K_p = 2, f_z = 80$ Hz, and $f_p = 8$ kHz.

output resistance is replaced by a dc-dc converter are shown in Fig. 14.

It can be observed that afer the heavy-to-light load change the negative incremental resistance of the downstream converter



(a)



(b)

Fig. 13. (a) Simulation results of a slow controller for output load changes between 100 W and 175 W. Top: rectified line voltage. Middle: rectified line current. Bottom: output voltage. The time scale shows seconds. (b) Complex plane representation for $R = 300\ \Omega, \mathrm{V_{out}} = 385$ V, $C = 47\ \mu$F, and $R_s = 25\ \Omega$; voltage-loop compensator parameters (13) are $K_p = 0.2$, $f_z = 8$ Hz, and $f_p = 8$ kHz).

initially decreases the output voltage. However, the controller quickly compensates for the new conditions in the circuit. The influence of the negative incremental resistance and the effective operation of the controller can also be seen for the light-to-heavy load transient.

4) Simulations of the Dead-Zone Controller: Simulation results of a fast dead-zone controller are shown in Fig. 15. The controller is designed as described in Section IV-B. It can be seen that the response matches circle criteria conditions in this case as well.

B. Experimental Verification

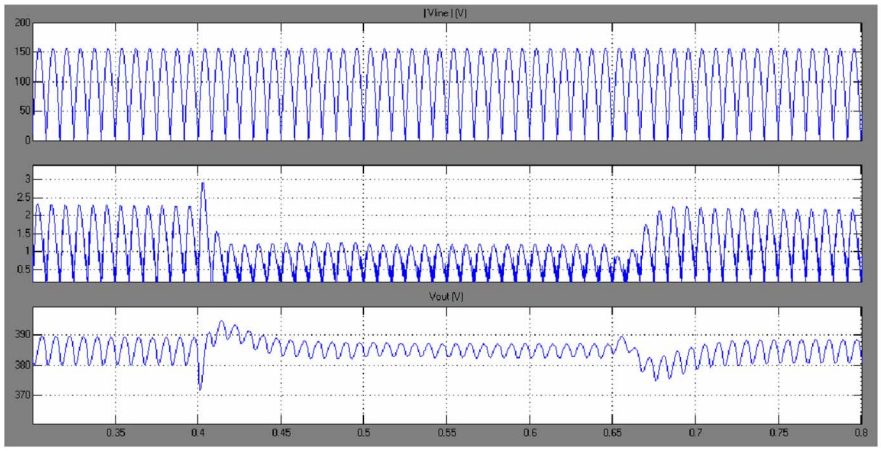
In Figs. 16–18, experimental results of load-transient response for the STCF-based system and the dead-zone controller are shown. Fig. 16(a) and (b) shows load-transient response of the STCF experimental prototype when the controller of Fig. 8(b) is used. The results agree with simulations. To verify performance for the universal input, the controller is tested for two standard line voltage values, 110 $\mathrm{V_{rms}}$ and 240 $\mathrm{V_{rms}}$. The waveforms show that in both cases the controller satisfies speed and stability requirements.

Fig. 17 shows load-transient response of the slow PID compensator of Fig. 13(b). Again, the experimental waveforms are in good compliance with simulations [Fig. 13(a)]. However, it should be noted that for a low-bandwidth compensator design, conventional approach, a utilizing double-averaged model [3] is probably more convenient. It allows more intuitive adjustment of the desired voltage-loop bandwidth and phase margin, allowing better control of the system dynamic response.

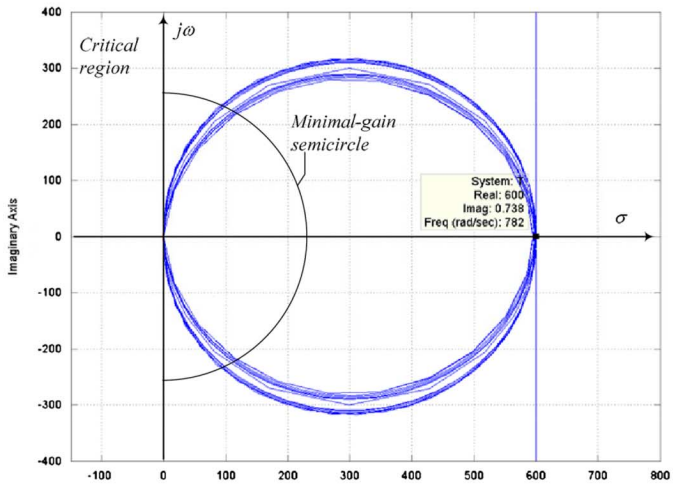
The load-transient response of the fast dead-zone controller of Figs. 9 and 10(b) is demonstrated in Fig. 17. As expected, the system response is fast, stable, and almost identical to that of the STCF system. This result gives additonal verification of the validity of the proposed controller desing method and demonstrates its versatility.

VI. Conclusion

Fast voltage-loop controllers for rectifiers with power factor correction (i.e., PFCs) have been feasible for quite some time. However, even though they bring obvious advantages in dynamic performance and the PFC's size optimization, traditional low-bandwidth controllers are still predominantly used. This is



(a)



(b)

Fig. 14. Simulation results for the fast STCF controller loaded with a downstream dc-dc converter: (a) load change between 100 W and 175 W. Top: rectified line voltage. Middle: rectified line current. Bottom: output voltage. The time scale is in seconds. (b) Complex plane controller representation. The system of Fig. 1 with added STCF is analyzed for $R = 300\ \Omega, \mathrm{V_{out}} = 385$ V, $C = 47\ \mu$F, and $R_s = 25\ \Omega$. The voltage-loop compensator parameters (13) are $K_p = 2$, $f_z = 8$ Hz, and $f_p = 8$ kHz.

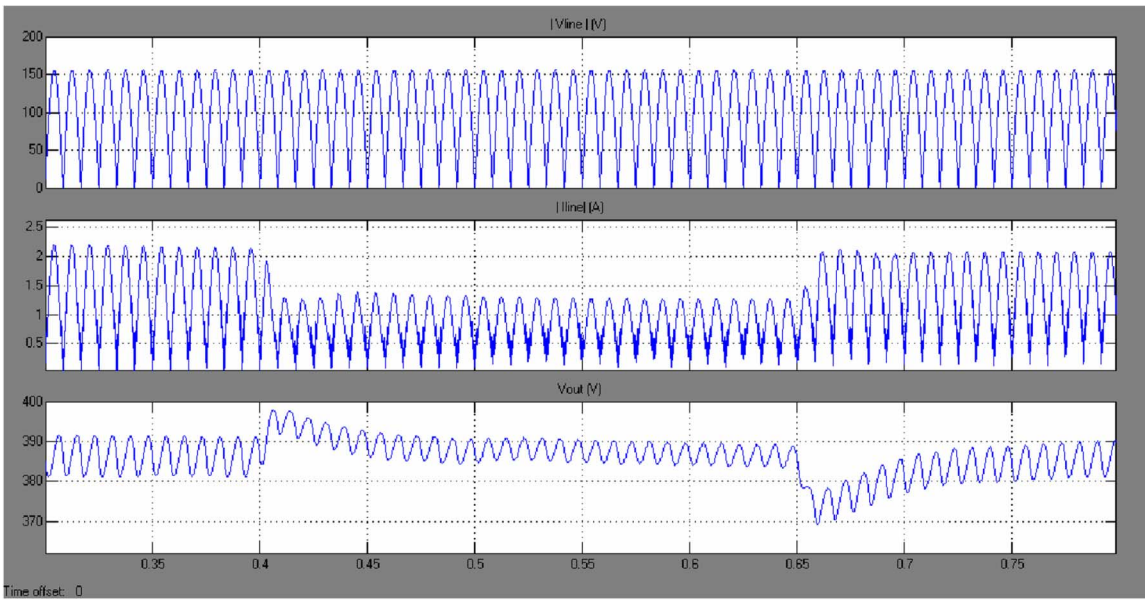


Fig. 15. Simulation results for fast dead-zone controller when the output load changes between 100 W and 175 W. Top waveform: rectified line voltage. Middle: rectified input current. Bottom: PFC's output voltage. The time scale shows seconds.

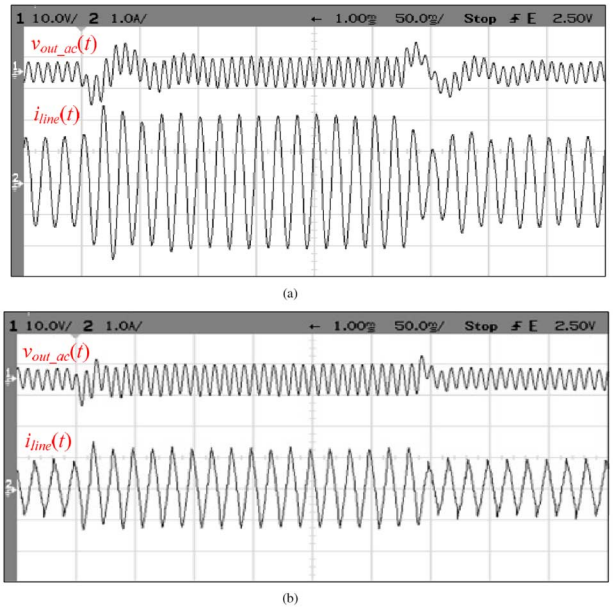


Fig. 16. Load-transient response of STCF controller for the load change between 100 W and 175 W. The input line voltage is: (a) $V_{\rm line} = 110\ {\rm V_{rms}}$, (b) $V_{\rm line} = 220\ {\rm V_{rms}}$; Ch-1: ac component of the output voltage $v_{\rm out\_ac}(t)$ 10 V/div - ac; Ch-2: $i_{\rm line}(t)$ 1 A/div.

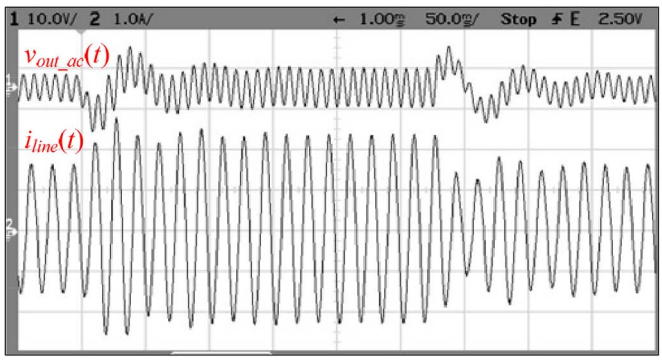


Fig. 17. Load-transient response of the fast dead-zone controller for load change between 100 W and 175 W. The input line voltage is: (a) $V_{\rm line} = 110\ {\rm V_{rms}}$, Ch-1: ac component of the output voltage $v_{\rm out\_ac}(t)$ 10 V/div—ac; Ch-2: $i_{\rm line}(t)$ 1 A/div.

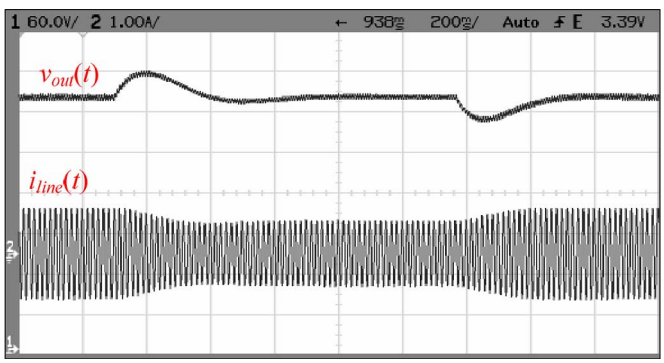


Fig. 18. Load-transient response of a slow controller for the output load change between 100 W and 175 W. The input line voltage is $V_{\rm line} = 220\ {\rm V_{rms}}$; Ch-1: $v_{\rm out}(t)$ 60 V/div; Ch-2: $i_{\rm line}(t)$ 1 A/div.

mostly due to the unsolved modeling and related stability problems, caused by the nonlinear time-varying nature of the fast voltage loop. Most models are developed for particular controller implementations and cannot be directly applied for several systems requiring very simple hardware for realization. In particular, for controllers containing regulation band (i.e., dead-zone) elements and notch/comb filters, stability of the system for all operating conditions is hard to verify.

This paper introduces a new general method for stability assessment and fast voltage-loop compensator design that can be applied for the two above mentioned controller realizations, as well as for many others. It is based on the utilization of the *circle criterion* that unifies conventional linear control theory tools (i.e., frequency domain analysis) with those used for nonlinear time-varying systems. The design procedure consists of three fairly simple steps. First, using a transformation of a power source to a current source, the structure of the PFC voltage loop is rearranged so a clear distinction between nonlinear time-varying and linear parts of the system can be made. Then, a sector defining the nonlinearity and the corresponding critical region in the complex plane are defined. In the final step, a Nyquist plot of the linear part of the system is drawn and shaped with a linear compensator to satisfy stability and speed requirements. The system is considered both fast and stable if the Nyquist plot does not intersect or encircle the critical region and if at a frequency larger than twice the line frequency the plot remains outside a minimal-gain semicircle. The minimal-gain semicircle is chosen based on the requirement that the instantaneous "loop gain" of the system is sufficiently high during most of the line period.

The step-by-step compensator design procedure is demonstrated on two practical digital controllers. The first employs a STCF for ripple elimination and the second utilizes a dead-zone in the analog-to-digital conversion. The performance of the controllers are tested and verified both through simulations and experiments. Matlab Simulink results show a good agreement between theoretical analysis and expected system behavior. The experimental results obtained with a 200-W boost-based PFC prototype show fast and stable operation of the voltage loop, further verifying validity of the proposed method.

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