A Modular Bidirectional DC Power Flow Controller With Fault Blocking Capability For DC Networks

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***Abstract*—This paper introduces a power flow controller that can be deployed to interconnect DC networks of different or similar voltage levels and manage the power flow between them. Its key features include: 1) bidirectional power flow 2) both step-up and step-down operation and 3) bidirectional fault blocking similar to a DC circuit breaker. Moreover, its modular architecture makes it aptly suited for high-voltage DC (HVDC) applications. The kernel of the power flow controller is a new class of single-stage bidirectional DC/DC converters utilizing interleaved strings of cascaded submodules. The converter operation is analyzed and a simplified model is implemented in PSCAD/EMTDC. A control strategy that ensures steady-state power balance of each submodule capacitor via circulating AC currents is introduced. Simulation results validate the converter's principle of operation and the proposed control strategy.**

I. Introduction

The use of DC transmission for the large scale integration of renewable energy sources is burgeoning [1]; most notably, for grid connection of offshore wind farms [2], [3]. Due to this changing landscape, the development of DC grids for the collection and distribution of energy from renewable sources is gaining traction [4], [5]. For such applications, the use of high-voltage DC (HVDC) technology has garnered significant attention [6], [7].

One of the principle challenges facing the widespread deployment of DC grids is management of network power flows. Bidirectional DC/DC converters can be dispatched to adjust line voltages, or the voltage between different network segments, and thereby extend the power controllability domain of DC grids [8]. However, few DC/DC topologies are suitable for HVDC applications. The use of back-to-back DC/AC conversion stages is costly and hinders converter efficiency while transformerless DC/DC converters are typically not modular and suffer from uncontrolled propagation of fault currents due to external DC faults. The aim of this work is to propose a power flow controller architecture for DC networks that avoids these drawbacks, and to validate its operation and steady-state control requirements via simulation of an appropriate converter model. In particular, the architecture must be well suited for HVDC applications.

II. Proposed DC Power Flow Controller

A. Three-String Architecture

Fig. 1 shows the three-string architecture of the DC power flow controller for deployment in bipolar DC networks. The kernel of the controller is a new class of single-stage bidirectional DC/DC converters utilizing interleaved strings of cascaded submodules (SMs). Each string is comprised of two pairs of arms; each pair of arms consisting of an inner arm and an outer arm, where an arm is defined as a set of cascaded SMs. The arms of each string are series-stacked in symmetric relation about an associated midpoint, i.e. o1,o2,o3, with the inner arms flanked by the outer arms. Each inner arm and outer arm employs m half-bridge SMs (HB/SMs) and k full-bridge SMs (FB/SMs), respectively. Circuit diagrams for the HB/SM and FB/SM are given in Fig. 2. The arm voltages for each string, e.g. $[v_{1\mathrm{k}}, v_{1\mathrm{m}}, v'_{1\mathrm{m}}, v'_{1\mathrm{k}}]$ for string #1, have both DC and AC components. Arm chokes L_{a} accommodate the switching action of the SMs. Inductors L_{r} link the strings together via their midpoints and serve to establish circulating AC currents that are required by the DC/DC conversion process.

Input filtering for the power flow controller is optionally provided by inductors L_{s}. However, filter element L_{f} is necessary to attenuate AC voltages present at the DC output nodes of each string. The magnetizing inductance of each set of coupled inductors, L_{f}, is suitable to provide the large impedance needed for attenuation of the AC output filter currents. Moreover, use of coupled inductors as shown ensures cancellation of DC flux within the core. The capacitors C_{f} are a practical consideration to sink any high-frequency AC currents introduced by switching action of the SMs.

In comparison to the well known three-phase DC/AC modular multilevel converter (MMC) [9]–[11], the three-string architecture for the DC power flow controller in Fig. 1 shares a similar modular structure. As will become more apparent in subsequent sections, the three-string implementation of the proposed power flow controller may be viewed as the MMC structure adapted for single-stage DC/DC conversion.

B. Two-String Architecture

The DC power flow controller in Fig. 1 utilizes three interleaved strings of cascaded SMs. By removing one of the strings, a two-string implementation is also possible as shown in Fig. 3. Note the ability to install a coupled inductor set at each DC output pole has been exploited due to the even number of interleaved strings. The two-string and three-string architectures have the same fundamental principle of operation as each string employs an identical DC/DC conversion process.

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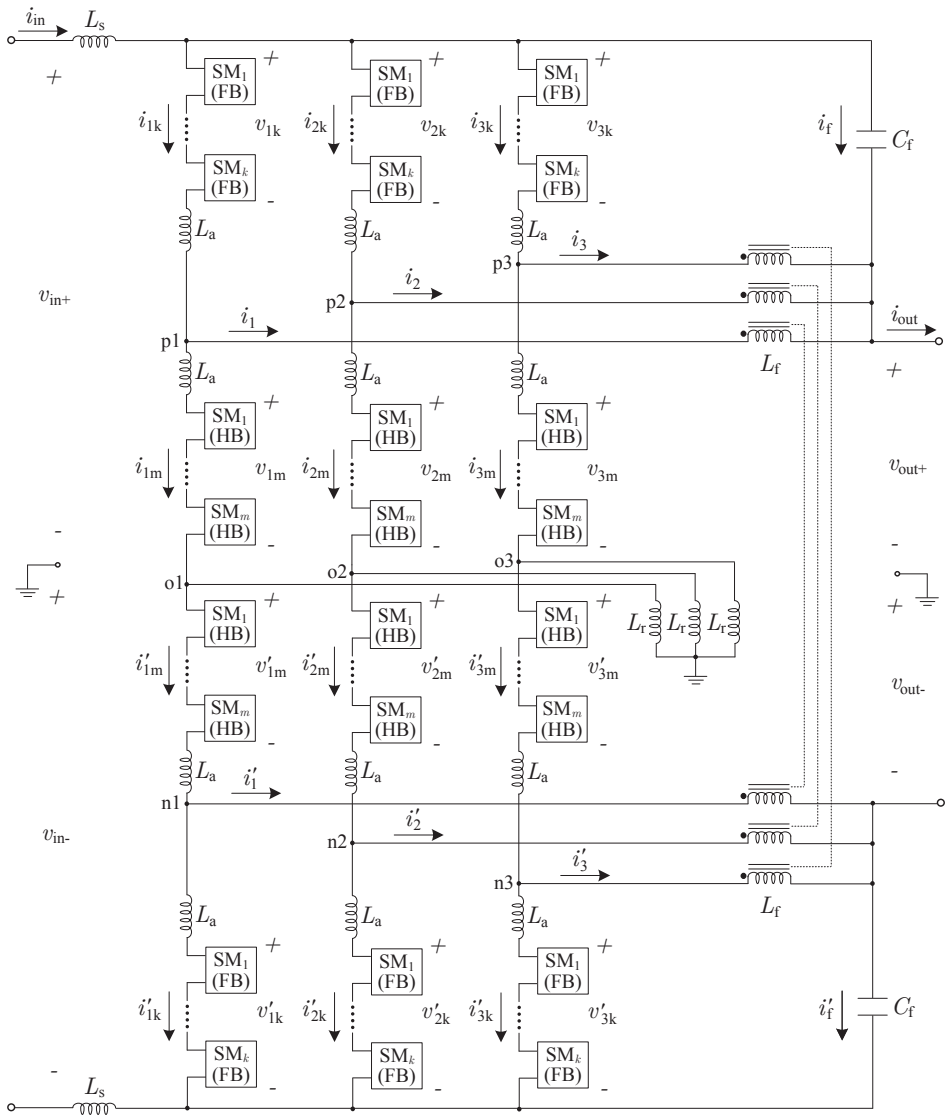


Fig. 1. Three-string DC power flow controller architecture.

For equal string designs, the two-string architecture has 2/3 the output power rating of the three-string.

The sections outlining principle of operation, fault blocking capability and modeling and analysis of the power flow controller apply to both the two-string and three-string architectures. However, only the two-string is analyzed in subsequent sections. This architecture is chosen as it is the simplest multi-string implementation of the power flow controller. In particular, AC phasor diagrams used in converter analysis can be simplified, ensuring key aspects of the single-stage DC/DC conversion process are clearly illustrated.

III. Principle of Operation

In Fig. 1 and Fig. 3, the DC input network voltages $v_{\text{in}+}$ and $v_{\text{in}-}$ can be unevenly split between the arms of each string. For example, arm voltages $v_{1\text{k}}$ (outer arm) and $v_{1\text{m}}$ (inner arm) can have unequal DC components that sum to $v_{\text{in}+}$. The same applies to $v'_{1\text{m}}$ (inner arm) and $v'_{1\text{k}}$ (outer arm) with $v_{\text{in}-}$. Division of $v_{\text{in}+}$ and $v_{\text{in}-}$ as described is achieved by controlling the number and polarity of SM capacitors inserted along each string via switching action. The DC output network, represented by $v_{\text{out}+}$ and $v_{\text{out}-}$, is coupled across the inner arms of each string as shown.

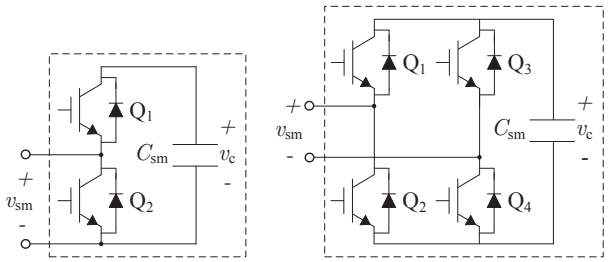
The arrangement of HB/SMs and FB/SMs in Figs. 1 and 3 permits both step-up and step-down voltage level conversion for the power flow controller. The voltage conversion ratio, D, and its complement, D', are defined as

$$D \triangleq \frac{v_{\text{out}+}}{v_{\text{in}+}} = \frac{v_{\text{out}-}}{v_{\text{in}-}} \tag{1}$$

$$D' \triangleq 1 - D. \tag{2}$$

From (1) and (2) the operating modes of the power flow controller are summarized

- step-down operation: $0 < D < 1$ and thus $0 < D' < 1$
- step-up operation: $D > 1$ and thus $D' < 0$.



(a) Half-bridge SM (HB/SM) (b) Full-bridge SM (FB/SM)

Fig. 2. SM configurations for the DC power flow controller.

For step-down operation where the voltages at nodes p1,p2,p3 (and n1,n2,n3) relative to ground always remain below $v_{\mathrm{in}+}$ (and above $-v_{\mathrm{in}-}$), the FB/SMs in Fig. 1 and Fig. 3 need only function as HB/SMs. That is, the FB/SMs can be replaced with HB/SMs[1] as long as the outer arms of each string are never required to inject negative voltages, e.g. $v_{1\mathrm{k}}$ & $v'_{1\mathrm{k}} > 0$. However, by exploiting the additional switching state (i.e. $v_{\mathrm{sm}} = -v_{\mathrm{c}}$) provided by the FB/SMs, the aforementioned node voltages can exceed their respective DC input rails. This enables step-up operation and the ability of the power flow controller to interconnect networks of similar voltage levels. The range of permissible voltage conversion ratios depends primarily on the SM ratio k to m and maximum allowable SM capacitor voltage. $v_{\mathrm{out}+}$ and $v_{\mathrm{out}-}$ can thus be generated within a certain range of step-up and step-down ratios, without the use of an AC transformer as is conventionally required [12], [13].

The DC power flow controller in Fig. 1 and Fig. 3 achieves single-stage DC/DC conversion by using circulating AC currents to ensure power balance for each SM capacitor. This new form of energy conversion employs a power transfer mechanism similar to that recently described in [14]. The circulating currents are established primarily by inductors L_{r} and serve to exchange average AC power between each outer arm and the adjacent inner arm, in a near lossless manner. To setup the circulating currents, the AC components of the arm voltages are synthesized such that each pair of arms generates a net AC voltage. DC power transfer between networks is reversed by changing polarity of i_{in}. The capability for bidirectional DC power transfer is a result of employing SMs, as they inherently permit bidirectional current flow.

IV. Bidirectional Fault Blocking

In addition to enabling step-up operation and the interconnection of networks with similar voltage levels, the FB/SMs in Fig. 1 and Fig. 3 can provide bidirectional fault blocking. That is, the power flow controller can interrupt fault currents initiated by DC faults in either the input or output side networks similar to a DC circuit breaker. This is accomplished by controlling the FB/SMs in Fig. 1 and Fig. 3 to impose the appropriate polarity of voltage during fault events, thereby blocking the flow of fault currents. This strategy is similar

[1]Bidirectional fault blocking for the power flow controller, which necessitates the use of FB/SMs as shown in Figs. 1 and 3, is discussed in section IV.

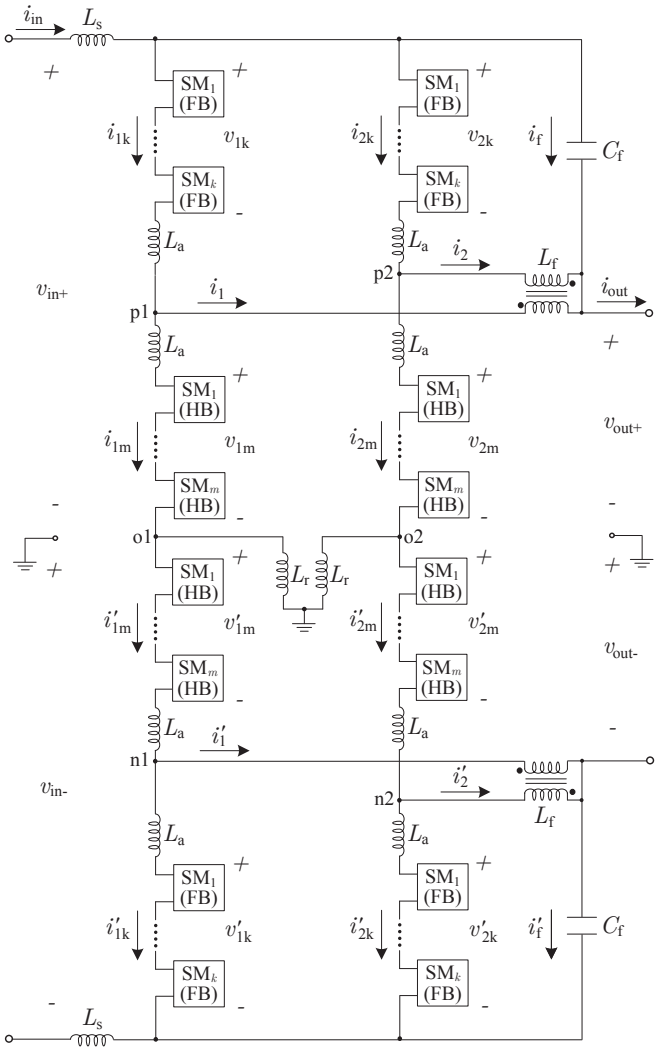


Fig. 3. Two-string DC power flow controller architecture.

to the recognized fault blocking scheme for the MMC [5], [15]. However, unlike in Figs. 1 and 3, fault blocking for the MMC requires that all HB/SMs be replaced with FB/SMs. Moreover, the MMC gains no other operational benefit at the large expense of doubling the number of switches. In comparison, by utilizing FB/SMs in only the outer arms, the power flow controller gains bidirectional fault blocking along with the operational advantages outlined in section III.

In general, to ensure bidirectional fault blocking the $2k$ FB/SMs within each string must collectively provide enough reverse blocking voltage to counteract the larger of $v_{\mathrm{in}+}+v_{\mathrm{in}-}$ and $v_{\mathrm{out}+}+v_{\mathrm{out}-}$. However, in practice the DC network with the highest voltage stress will likely be connected to the input side of the controller for insulation coordination purposes. The FB/SMs would in this case need to block $v_{\mathrm{in}+}+v_{\mathrm{in}-}$.

V. Converter Modeling and Analysis

Unless otherwise indicated, the following assumptions are enforced: 1) each arm has a large number of SMs such that ideal sinusoidal AC voltages are synthesized 2) AC voltages and currents are represented by their steady-state fundamental

frequency components 3) AC output filtering is ideal and 4) AC output filter currents are negligible. The last assumption implies $L_{\rm f}$ is sufficiently high such that, for each string, the AC filter currents are small relative to the AC component of the outer arm currents, e.g. $|\tilde{i}_1| << |\tilde{i}_{1\rm k}|$ and $|\tilde{i}'_1| << |\tilde{i}'_{1\rm k}|$. Here $\tilde{i}$ denotes the fundamental frequency component of i.

Based on the discussions in section II, each arm can be viewed as a controllable AC voltage source with a variable DC component. However, the fundamental operating frequency of the arm voltages is not constrained to conventional 50/60 Hz. Modulating frequencies greater than 50/60 Hz can be used to reduce the size of circuit reactive components, for example $L_{\rm r}$, as well as the SM storage capacitors.

A simplified model for string #1 of the power flow controller is shown in Fig. 4, which is valid for both Fig. 1 and Fig. 3. An identical model is obtained for the remaining string(s) by changing the appropriate variable subscripts. The cascaded SMs within each arm are modeled with ideal voltage sources, which is common practice in MMC analysis [16]–[20]. These sources model both the DC and AC components of the arm voltages. All currents are separated into their DC and AC parts with n denoting the number of interleaved strings, e.g. $n = 2$ for Fig. 3. Observe the DC current through the inner arms increases as D becomes smaller. For $D < 0.5$, the inner arms carry a DC current greater than $|i_{\rm in}/n|$. This operating region thus incites high conduction losses, and may necessitate additional inner arms installed in parallel to avoid derating of power transfer between networks. The ability to parallel multiple arms is enabled by the inclusion of $L_{\rm a}$ in each arm. Restructuring of arm chokes in Fig. 1 and Fig. 3 to eliminate individual chokes is possible provided the basic requirement of an inductance in every voltage loop is not violated.

Each string follows the DC/DC conversion process in Fig. 4. The outer arms and inner arms of each string carry a DC current of $|i_{\rm in}/n|$ and $|(D'/D)i_{\rm in}/n|$, respectively. To ensure power balance for each SM capacitor in string #1, the following average power constraints must be met

$$\mathbf{V}_{1\rm k} \cdot \mathbf{I}_{1\rm k} = -D' v_{\rm in+} \frac{i_{\rm in}}{n} \tag{3}$$

$$\mathbf{V}_{1\rm m} \cdot \mathbf{I}_{1\rm m} = D' v_{\rm in+} \frac{i_{\rm in}}{n} \tag{4}$$

$$\mathbf{V}'_{1\rm m} \cdot \mathbf{I}'_{1\rm m} = D' v_{\rm in-} \frac{i_{\rm in}}{n} \tag{5}$$

$$\mathbf{V}'_{1\rm k} \cdot \mathbf{I}'_{1\rm k} = -D' v_{\rm in-} \frac{i_{\rm in}}{n}. \tag{6}$$

$\mathbf{V}_{1\rm k} \cdot \mathbf{I}_{1\rm k}$ denotes the phasor dot product. The notation $\mathbf{V}_{1\rm k}$ and $\mathbf{I}_{1\rm k}$ signifies the fundamental frequency AC rms phasors for $\tilde{v}_{1\rm k}$ and $\tilde{i}_{1\rm k}$, respectively.

Power balance constraints (3) through (6) reveal an average AC power equal to $|D' v_{\rm in+}(i_{\rm in}/n)|$ (and $|D' v_{\rm in-}(i_{\rm in}/n)|$) must be exchanged between the outer arm and adjacent inner arm of the positive (and negative) DC pole for string #1. A similar set of constraints can be formulated for the remaining string(s) in Figs. 1 and 3. To ensure a net AC voltage is not impressed across the input or output terminals of the power

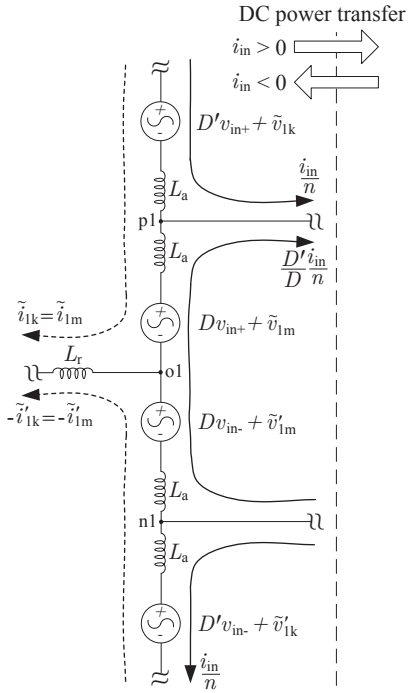


Fig. 4. Simplified model for string #1 of DC power flow controller in Fig. 1 and Fig. 3, with ideal output filtering and AC filter currents neglected.

flow controller, requirements are imposed on the synthesized arm voltages

$$\tilde{v}_{1\rm k} = -\tilde{v}'_{1\rm k} \tag{7}$$

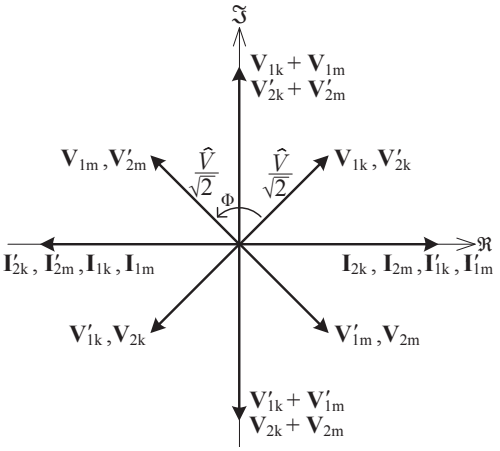
$$\tilde{v}_{1\rm m} = -\tilde{v}'_{1\rm m}. \tag{8}$$

In general, symmetry constraints similar to (7) and (8) are imposed on each string. Taking into consideration the phase shift between modulating waveforms of each string, interleaving of strings as shown in Figs. 1 and 3 offers natural cancellation of AC output inductor currents independent of D. For example, $\tilde{i}_1$ (and $\tilde{i}'_1$) and $\tilde{i}_2$ (and $\tilde{i}'_2$) in Fig. 3 always sum to zero as they are phase shifted by 180°. This implies $C_{\rm f}$ ideally carries zero current; $v_{\rm out+}$ and $v_{\rm out-}$ are effectively free of AC stimuli. However, in practice $C_{\rm f}$ will carry a small amount of high frequency current due to switching of the SMs.

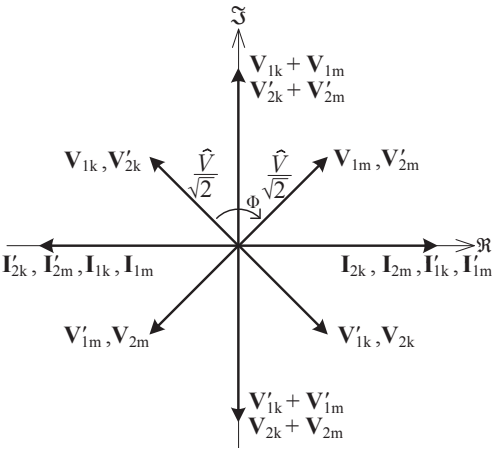
VI. Steady-State Power Balance of SM Capacitors

There are infinitely many combinations of AC arm voltages and resulting AC arm currents that can satisfy (3) through (8) for string #1. The same notion applies to a similar set of equations that can be formulated for the remaining string(s) in Figs. 1 and 3. However, only the two-string architecture is analysed in this section as it is the simplest multi-string implementation of the power flow controller. In particular, this choice reduces insulation requirements on the output filter inductances.

Fig. 5 gives two example AC phasor diagrams that illustrate the fundamental power transfer mechanism employed to achieve steady-state power balance of each SM capacitor in Fig. 3, for all possible operating modes of the power flow



(a) valid for: 1) step-down operation with input to output DC power transfer and 2) step-up operation with output to input DC power transfer.

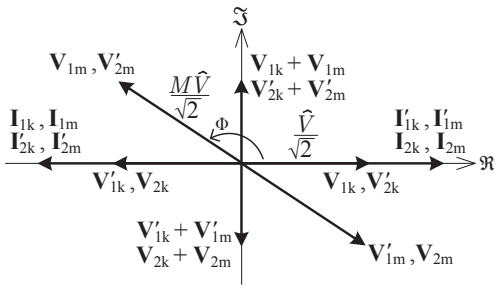


(b) valid for: 1) step-down operation with output to input DC power transfer and 2) step-up operation with input to output DC power transfer.

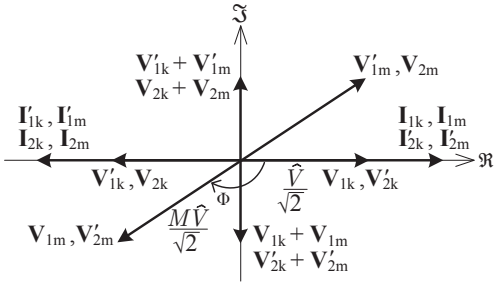
Fig. 5. Fundamental frequency AC rms phasor diagrams for arm voltages and currents that illustrate the power transfer mechanism used to achieve power balance of SM capacitors in Fig. 3, with AC output filter currents neglected.

controller. The peak magnitude of the AC arm voltages is denoted by $\hat{V}$. Φ is the phase shift between AC voltages of each outer arm and the adjacent inner arm, with positive values of Φ defined for the inner arm voltage leading the outer arm voltage. For example, positive values of Φ for string #1 correspond to $\mathbf{V}_{1\mathrm{m}}$ leading $\mathbf{V}_{1\mathrm{k}}$ and $\mathbf{V}'_{1\mathrm{m}}$ leading $\mathbf{V}'_{1\mathrm{k}}$. Note the modulating waveforms of each string in Fig. 5 are displaced by 180°.

It is easy to visualize via phasor dot products that each pair of inner and outer arms in Fig. 5 exchange equal AC average power. However, modulating the converter arm voltages with such a strategy constrains each pair of arms to equally share the reactive power requirements of the composite load formed by L_{r} and L_{a}. This implies each arm operates at an equal AC power factor (in Fig. 5 the example case of power factor equal to 0.707 is shown where $\Phi = \pm 90°$). A preferred control strategy is to impose unity power factor on the outer arms while realizing near unity power factor operation for the inner



(a) valid for: 1) step-down operation with input to output DC power transfer and 2) step-up operation with output to input DC power transfer.



(b) valid for: 1) step-down operation with output to input DC power transfer and 2) step-up operation with input to output DC power transfer.

Fig. 6. Fundamental frequency AC rms phasor diagrams depicting control strategy for arm voltages and currents to ensure power balance of SM capacitors in Fig. 3 while imposing unity power factor on outer arms and near unity power factor on inner arms, with AC output filter currents neglected.

arms as shown in Fig. 6. Here M is the ratio of inner arm to outer arm AC voltage magnitudes, e.g. $M = |\mathbf{V}_{1\mathrm{m}}/\mathbf{V}_{1\mathrm{k}}|$. For a fixed $\hat{V}$, this control scheme minimizes the circulating AC currents needed when operating with larger values of D, e.g. $D > 0.6$. Moreover, it significantly reduces the circuit reactance (e.g. wL_{r} product) needed to establish the circulating AC currents.

Based on Fig. 4 and Fig. 6, the average power exchanged between each outer arm and the adjacent inner arm is

$$P_{\mathrm{k/m}} = \frac{M\hat{V}^2}{4X_{\mathrm{r}}} \sin\Phi \tag{9}$$

where

$$X_{\mathrm{r}} = \omega(L_{\mathrm{r}} + L_{\mathrm{a}}). \tag{10}$$

Positive values of $P_{\mathrm{k/m}}$ denote average AC power delivered from each outer arm to the adjacent inner arm of the same string. In general, $P_{\mathrm{k/m}}$ is adjusted by changing any combination of M, $\hat{V}$ or Φ. Converters designed with smaller X_{r} offer reduced circuit VAR requirements and result in values of $|\Phi|$ approaching 180°.

Equation (10) reveals the power flow controller can in fact be operated with L_{r} equal to zero. That is, the midpoints of each string in Fig. 3 (and similarly Fig. 1) can be connected together and solidly grounded. In this case the arm chokes solely provide the reactance needed to setup the circulating AC currents. However, it must be stressed the midpoint inductors

TABLE I
SIMULATION PARAMETERS

Converter Parameters	**Value**	
DC input network voltage, $v_{\mathrm{in}+}$, $v_{\mathrm{in}-}$	600 kV	
DC input network current, i_{in}	0.8 kA	
Input filter inductance, L_{s}	0 mH	
Arm choke, L_{a}	0.5 mH	
Midpoint string inductance, L_{r}	3 mH	
Output filter magnetizing inductance, L_{f}	6400 mH	
Output filter capacitance, C_{f}	1 uF	
Fundamental frequency, ω	2.513 krad/sec	
AC Parameters	**Value**	
	$D = 0.6$ ($i_{\mathrm{in}} > 0$)	$D = 1.1$ ($i_{\mathrm{in}} > 0$)
AC arm voltages magnitude, $\hat{V}$	230 kV	85 kV
AC arm voltages ratio, M	1.002	1.007
AC arm voltages phase shift, Φ	176.35°	-173.33°

L_{r} need only carry AC currents while arm chokes L_{a} must carry both DC and AC currents. The allocation of circuit inductance to L_{r} versus L_{a} is the outcome of a converter design optimization, and as such is outside the scope of this paper. The simulations in the subsequent section utilize a non-zero L_{r}.

VII. SIMULATION RESULTS

Two operating scenarios are simulated in PSCAD/EMTDC to validate operation of the two-string DC power flow controller architecture in Fig. 3. The scenarios include: 1) $D = 0.6$ (step-down) and 2) $D = 1.1$ (step-up). Each string is modeled as shown in Fig. 4. Arm voltages are modulated according to the strategy in Fig. 6. For each scenario, DC power transfer is from input to output ($i_{\mathrm{in}} > 0$) such that both Fig. 6(a) and Fig. 6(b) are utilized. The fundamental operating frequency of the arm voltages is selected as 400 Hz. Simulation parameters are given in Table I.

The simulation results for $D = 0.6$ and DC power transfer from input to output are given in Fig. 7. The DC input and output network voltages are $\pm$600 kV and $\pm$360 kV, respectively. i_{in} and i_{out} are 0.8 kA and 1.333 kA, respectively. The scheme in Fig. 6(a) is used with $\Phi = 176.35°$ and $M = 1.002$, which favourably enforces unity power factor operation for the outer arms while achieving near unity power factor for the inner arms. To facilitate the transfer of 960 MW between networks, each outer arm and the adjacent inner arm exchange 96 MW of AC average power. $i_{1\mathrm{m}}, i'_{1\mathrm{m}}, i_{2\mathrm{m}}, i'_{2\mathrm{m}}$ and $i_{1\mathrm{k}}, i'_{1\mathrm{k}}, i_{2\mathrm{k}}, i'_{2\mathrm{k}}$ have DC components of -0.267 kA and 0.4 kA, respectively. The AC currents circulating in the arms have a peak magnitude of 0.835 kA. Observe L_{f} imposes a large AC impedance to i_1, i_2 and i'_1, i'_2, which validates the prior assumption of negligible output filter currents.

Fig. 8 shows the simulation results for $D = 1.1$ and DC power transfer from input to output. The DC input and output network voltages are $\pm$600 kV and $\pm$660 kV, respectively. i_{in} and i_{out} are 0.8 kA and 0.727 kA, respectively. To accommodate step-up operation the modulation scheme in Fig. 6(b) is adopted with $\Phi = -173.33°$ and $M = 1.007$. Only 24 MW of AC average power is exchanged between each pair of arms to facilitate the same 960 MW transfer between networks. $i_{1\mathrm{m}}, i'_{1\mathrm{m}}, i_{2\mathrm{m}}, i'_{2\mathrm{m}}$ and $i_{1\mathrm{k}}, i'_{1\mathrm{k}}, i_{2\mathrm{k}}, i'_{2\mathrm{k}}$ have DC components of 0.036 kA and 0.4 kA, respectively. The peak magnitude of the circulating AC currents is 0.565 kA. The SMs experience lower peak current stresses due to the decreased AC power exchange between arms.

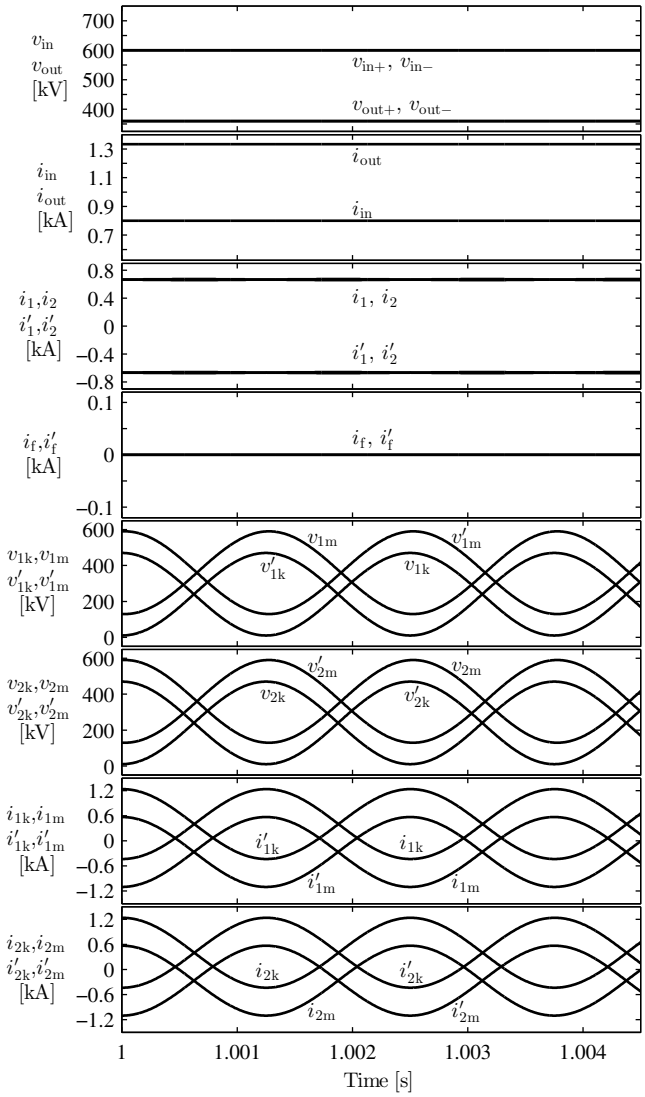


Fig. 7. Simulation results for two-string DC power flow controller architecture in Fig. 3 with $D = 0.6$ and $i_{\mathrm{in}} > 0$.

For the operating scenario in Fig. 7, the FB/SMs need only function as HB/SMs because $\hat{V}$ remains below $D'v_{\mathrm{in}+}$ and $D'v_{\mathrm{in}-}$. In comparison, the operating scenario in Fig. 8 necessitates the use of FB/SMs. In both cases, the FB/SMs serve the dual purpose of providing bidirectional fault blocking.

VIII. CONCLUSION

A new modular DC power flow controller for bipolar DC networks is presented. Its modular and easily scalable architecture makes it aptly suited for high-voltage and high-power applications, particularly HVDC. The controller features a new class of single-stage bidirectional DC/DC converters utilizing

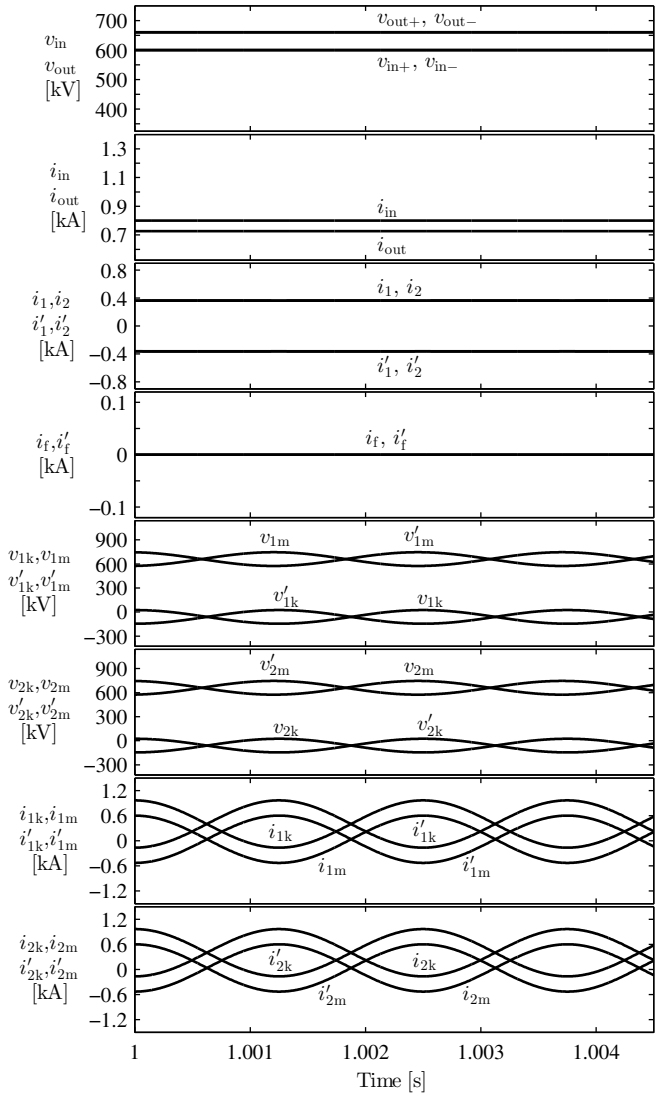


Fig. 8. Simulation results for two-string DC power flow controller architecture in Fig. 3 with $D = 1.1$ and $i_{\text{in}} > 0$.

interleaved strings of cascaded SMs. Power balance for each SM capacitor is achieved via circulating AC currents, which are established by reactive elements linking each string.

The two-string and three-string architectures for the power flow controller are introduced, where the latter is revealed to show similarity to the three-phase DC/AC MMC structure. By employing a unique arrangement of HB/SMs and FB/SMs for each string, the controller can provide both step-up and step-down operation and interconnect DC networks of similar voltage levels. Moreover, the placement of FB/SMs enables bidirectional fault blocking similar to a DC circuit breaker. This is a key operational advantage of the power flow controller as DC fault protection is widely recognized as a primary obstacle hindering the development of future DC grids.

A simplified model of the converter is developed and the DC/DC conversion process is analyzed in detail. A control strategy is proposed for the arm voltages that ensures steady-state power balance of the SM capacitors. This strategy has the benefits of minimizing the circulating AC currents needed for the DC/DC conversion process while significantly reducing the installed circuit reactance. As an adopted case study, the two-string DC power flow controller architecture is implemented in PSCAD/EMTDC. Presented simulation results validate both its principle of operation and the proposed control strategy.

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