A Low-Power DC-DC Converter with Digital Spread Spectrum for Reduced EMI

Olivier Trescases, Guowen Wei, Wai Tung Ng
University of Toronto, 10 King's College Road, Toronto, ON, M5S 3G4, Canada
E-mail: {trescas, weig, ngwt}@vrg.utoronto.ca

***Abstract*— This paper presents a 1.8 V step-down DC-DC converter prototype with a hybrid delay-line based digital pulse-width modulator. A spread spectrum clock generation scheme is demonstrated for reducing EMI. The switching frequency of the buck converter prototype is automatically varied from 1.74 MHz to 2.84 MHz in 128 steps using a pseudo-random 512 cycle pattern, resulting in a 23 dB reduction in the conducted EMI peak. The digital pseudo-random pattern is converted to an analog reference voltage using a low-cost one-bit delta-sigma DAC having an over-sampling rate of 4096. The DAC output modulates the reference voltage of an LDO that regulates the delay-line supply voltage. It is shown that the effective duty-cycle changes by only 0.27 % over the frequency range. With spread spectrum mode enabled, the inductor current ripple becomes time-dependent but the efficiency degrades by less than 0.1%. The proposed architecture can be applied to a wide variety of state-of-the-art digital controllers that rely on delay-line based pulse width modulators.**

I. Introduction

Meeting stringent conducted EMC standards can be challenging for hand-held devices since EMI problems are often difficult to trace and eradicate late in the product development phase. A number of active EMI mitigation schemes for SMPS have been described [1]–[6] as promising alternatives to expensive passive EMI snubbers. With these preemptive techniques, snubbers may be completely eliminated from the PCB, significantly reducing the form factor and cost of the SMPS. Active EMI reduction schemes, with the exception of soft-switching, all have variable switching frequency (VF) operation in common. They differ only in the method of achieving VF; using a pseudo random clock, a frequency modulated clock, chaotic peak current control, delta sigma modulation or hysteretic control. By varying the switching frequency, the noise generated by the SMPS can be spread across a frequency band and the fundamental peak can be drastically reduced. This spread spectrum, or randomized PWM is a well proven technique for dramatically reducing the EMI in SMPS [7] [8]. Given that this feature is already commercially available in low-power analog DC-DC controller ICs [7], the objective of this paper is to demonstrate a practical, low-cost spread spectrum architecture compatible with advanced delay-line DPWMs used in monolithic digital SMPS controllers for low-power applications.

Several key innovations are making it feasible for digital switch-mode power supply (SMPS) controllers to displace their analog counterparts in the highly cost-sensitive low-power (<10 W) hand-held device market [9] [10]. These include delay-line based digital pulse with modulators (DPWM), low-power specialized ADCs and compensators. In particular, the move from counter-based to delay-line based DPWMs can drastically reduce the power consumption in the controller.

II. Achieving Spread Spectrum

A. Spread Spectrum Architecture

It is well known that the delay and hence the oscillation frequency of a ring oscillator can be tuned by varying the supply voltage of the internal delay elements. The proposed spread spectrum DPWM architecture shown in Figure 1 is based on this simple concept applied with a pseudo-random pattern generator scheme [7]. The delay-line supply voltage, $V_{dd,dl}$ is controlled by a low drop out linear regulator (LDO) whose reference voltage, V_{ref} is varied to achieve a variable switching frequency, f_s. A 9-element linear feedback shift-register (LFSR) is used to generate a 512 cycle pseudo-random sequence to achieve a uniformly distributed frequency target [7]. A 7-bit number, freq_{ss} is extracted from the LFSR and converted to V_{ref} using a one-bit $\Delta\Sigma$ DAC that includes a digital modulator and low-pass filter, as explained in the following section. The one-bit $\Delta\Sigma$ DAC reduces the system complexity and results in a high-resolution V_{ref} since a high over-sampling ratio (OSR) of 4096 is used in this work. The OSR is set by the clock divider inside the pattern generator block. The self-oscillating hybrid delay-line DPWM block described in the following section provides both the PWM signal that feeds the power stage, as well as the system clock, clk_{sys}.

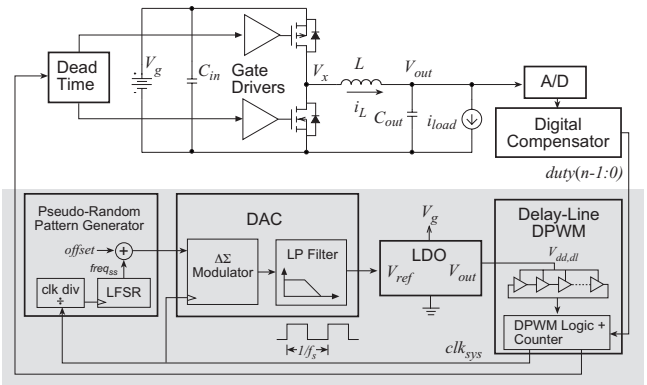


Fig. 1. Architecture of the spread spectrum system (shaded) as part of a digitally controlled buck converter.

The pseudo-random pattern generator clock is derived from the variable frequency system clock. This implies that the time interval for each target frequency varies with the frequency

itself. As a result, while the target frequency is uniformly distributed, the actual switching frequency will not be uniformly distributed in time, leading to a less-than ideal spreading of the noise spectrum. To illustrate this effect, the time delay before a new frequency is selected, Δt_{ss} is plotted versus the target frequency code freq_{ss} in Figure 2. The data is extrapolated from the experimental results presented in Section V. The Δt_{ss} ranges from 1.45 ms at the maximum switching frequency to 2.35 ms at the minimum switching frequency. The duration of the repetitive pattern of $V_{dd,dl}$ can be estimated using:

$$\Delta T_f = 2^{k-l} \sum_{i=0}^{2^l-1} \Delta t_{ss}(i) \tag{1}$$

where l is the number of bits in the target frequency, k is the number of elements in the LFSR. This gives ΔT_f = 924 ms for l = 7, k = 9 and the Δt_{ss} given in Figure 2.

The spectral power density of various symmetric distribution laws is analyzed by [11], with the conclusion that a uniform distribution leads to an excellent trade-off between implementation complexity and spectrum spread. The deviation from a uniformly distributed frequency caused by the variable system clock rate still results in excellent noise reduction as demonstrated in Section V and hence no attempt was made to correct for this effect. If necessary, a uniform frequency distribution could be achieved by either using a fixed system clock derived from an additional fixed-frequency oscillator. Alternatively, the clock divider ratio in Figure 1 could be modified on-the-fly to account for the predictable frequency variation of clk_{sys}. Both of these options would potentially increase the system cost and complexity.

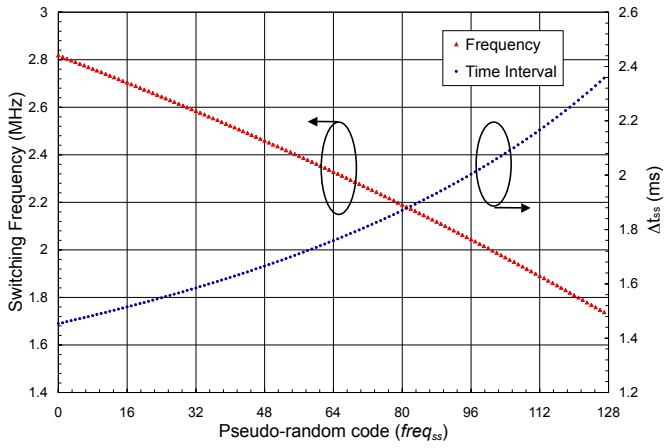


Fig. 2. Frequency and corresponding time slot versus 7-bit frequency target code.

The proposed architecture is compatible with monolithic IC implementation. The vast majority of the functionality can be achieved using synthesizable digital blocks. The LDO is only used to supply dynamic current to the delay-line line DPWM circuit block and hence it is not expected to contribute significantly to the overall system cost. As an example, a self calibrated DPWM [12] has been presented with a current consumption below 16 μA/MHz (including the calibration circuitry).

B. Digital Pulse Width Modulator

A variety of DPWM techniques have been proposed to achieve low power consumption, high switching frequency, f_s and high resolution as summarized by [13]. In one scheme [14], a self-oscillating delay-line is used in conjunction with a low frequency counter to reduce the number of delay-cells, resulting in a so-called hybrid DPWM. An N-bit hybrid DPWM includes a delay-line having 2^{M} elements to generate fine delay, followed by a $2^{\text{N-M}}$-bit counter to provide coarse delay adjustment [14]. The proposed 7-bit DPWM shown in Figure 3 builds on this topology by reducing the required number of delay-line elements by a factor of 2$\times$ for the same resolution and counter frequency. The 8-element delay line oscillator provides a clock, *clk* with a frequency of $8f_s$.

The delay through a single element, Δt corresponds to 1 LSB of the PWM resolution. Therefore a total resolution of 3 bits can be obtained by tapping the 8-element delay-line. If a 4-bit resolution is required, the number of elements must increase to 16 with the conventional approach. However, using only a NOR gate and a 2-1 MUX its possible to extract extra timing information from the delay line and therefore generate a signal at the MUX output with an effective timing resolution of 4 PWM bits. For example, when *duty(3)* is 0 in Figure 3(b), the tapped delay-line output (3-bit) is sufficient and is passed through the MUX. However when *duty(3)* changes to 1, an extra delay of $8\Delta t$ should be added to the tapped delay line output. This is achieved with the NOR gate when its output is selected to pass through the MUX. The final PWM pulse is generated by the SR latch which is set at the beginning of each switching period by the D-Flip-Flop, and reset when the combination of counter output and delay line output matches the desired duty cycle.

C. One-Bit $\Delta\Sigma$ Digital to Analog Converter

The DAC in Figure 1 is used to generate the analog voltage reference for the LDO. In this application, the DAC sampling rate, $f_{DAC} = f_{sys}/\text{OSR}$ is set by the clock divider circuit.

The 1st order $\Delta\Sigma$ modulator is shown in Figure 4. The delay element is implemented as a register clocked by clk_{sys}. The modulator can be implemented using a single register and two adders. The one-bit $\Delta\Sigma$ DAC topology is chosen for this work because it offers high linearity, low power (no quiescent current) and potential for compact on-chip implementation. The modulator noise-to-output transfer function for 1st order noise shaping is given by (2):

$$N_{TF}(z) = 1 - z^{-1} \tag{2}$$

For a 1st order modulator, it can be shown that the noise falls by 9 dB and hence the effective resolution increases by 1.5 bits for every doubling of the OSR [15].

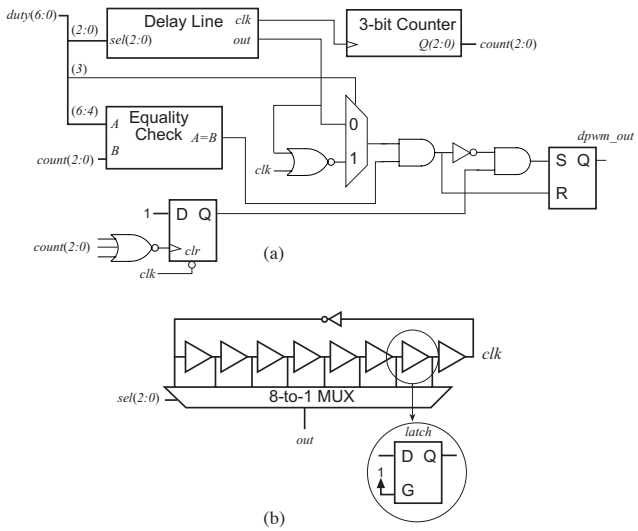


Fig. 3. (a) DPWM Architecture with a 7-bit resolution. (b) The self-oscillating delay-line requires only 8 latch-based delay elements.

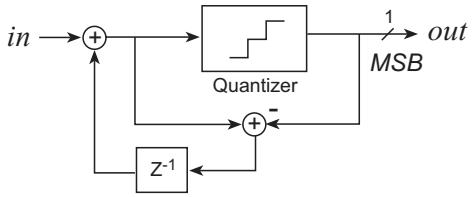


Fig. 4. Simple, 1st order all-digital modulator for the $\Delta\Sigma$ DAC.

III. Effects of Variable Switching Frequency on the Converter Operation

A. Converter Dynamics

One of the simplest and most practical digital compensator structures is shown in Figure 5. The digital compensator is used to implement the PID difference equation given by (3):

$$d[n] = d[n-1] + Ae[n] + Be[n-1] + Ce[n-2] \qquad (3)$$

where $d[n]$ is the duty cycle command and $e[n]$ is the error signal. In very low power SMPS ($\approx$ 1 W) applications, the multiplications in (3) are typically carried out using area-efficient lookup tables [16]. While so-called direct-digital controller design is gaining popularity, the digital compensator is traditionally designed using an equivalent continuous time model [16]. In the following analysis it is assumed that the digital compensator is clocked at the switching frequency, however this is not always the case. Dual-mode controllers have been reported for voltage [10] and current mode [17] control where the compensator clock frequency is varied to reduce power consumption. In addition, the changes in switching frequency occur only every 4096 cycles and therefore a linear model can be used to analyze the system at each frequency operating point.

The three coefficients in the PID difference equation can be derived from the optimized continuous time compensator using a variety of techniques, including pole-zero matching and the bilinear transform. This process is thoroughly covered in the literature and will not be covered here in further detail. The main focus in this work is the effect of varying the switching frequency on the controller structure of Figure 5.

The equivalent s-domain transfer function of the compensated system is given by:

$$H_{sys} = H_{A/D} \cdot H_{comp} \cdot H_{DPWM} \cdot H_{buck} \qquad (4)$$

where $H_{A/D}$, H_{comp}, H_{DPWM} and H_{buck} are the transfer functions of the A/D converter, compensator, DPWM and buck converter respectively. The ADC sampling delay and sensing gain are incorporated into $H_{A/D}$. The control-to-output transfer function of the buck converter is independent of the switching frequency as long the LC filter can be assumed to be frequency independent, and is given by:

$$H_{buck}(s) = \frac{\frac{V_g}{LC}}{s^2 + s\left(\frac{R_s}{L} + \frac{1}{R_p C}\right) + \frac{1}{LC}\left(1 + \frac{R_s}{R_p}\right)} \qquad (5)$$

where L and C are the buck converter filter components, R_s is the equivalent series resistance in the converter and R_p is the combination of the load resistance and the filter capacitor's equivalent series resistance (ESR). The buck converter has two complex conjugate poles at $f = 1/(2\pi\sqrt{LC})$ and a high Q factor. A high Q is desirable for efficient energy transfer but results in a low damping, making compensation more difficult [18] .

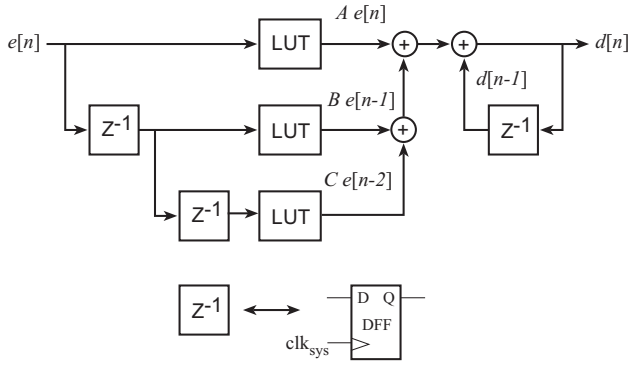


Fig. 5. Traditional LUT compensator used to implement the difference equation given by (3).

The magnitude and phase of H_{sys} are shown in Figure 6 for switching frequencies ranging from 1.74 - 2.84 MHz. The digital compensator operates with fixed coefficients and hence the compensation pole and zero shift with the switching frequency during spread spectrum operation. The resulting phase margin versus switching frequency is shown in Figure 7.

A transient simulation was carried out using MATLAB/Simulink to evaluate the dynamic response of the digital spread spectrum system. The synchronous buck power stage operation is accurately modeled using switches having a finite

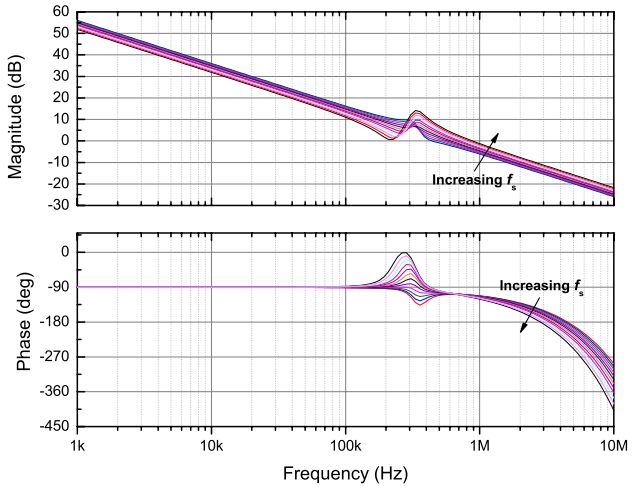


Fig. 6. Magnitude and phase of the digitally compensated system for different switching frequencies. The variation in the compensator clock frequency shifts the pole/zero location affecting system dynamics.

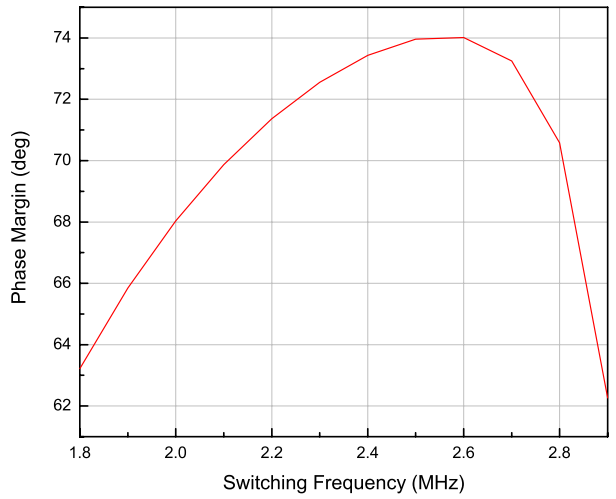


Fig. 7. Phase margin versus switching frequency for the digitally compensated system. The phase margin varies by over 10 degrees over the operating range.

on-resistance, output capacitance and body diodes. The inductor and capacitor ESR are included in the power stage model. A dead-time generator is also used, resulting in load-current dependent body diode conduction [19]. The compensator is modeled using the discrete architecture shown in Figure 5.

The transient simulation results are shown in Figure 8. The effect of a 1-200 mA load step is shown at three switching frequencies that cover the entire spread spectrum operating range. The system damping varies with the switching frequency, as predicted by the phase margin plot of Figure 7, despite the obvious limitations of the linear s-domain model.

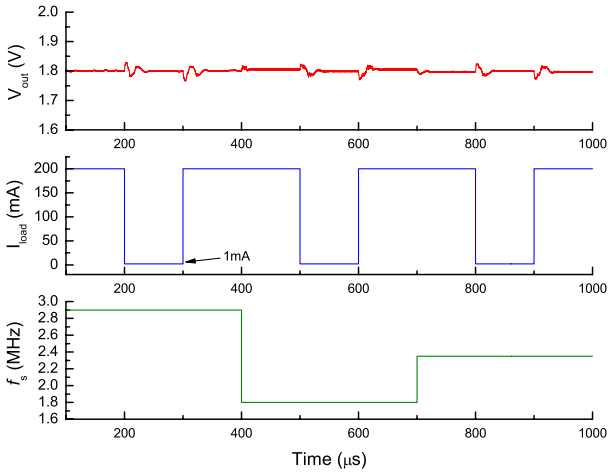


Fig. 8. Transient simulation showing the converter dynamic response for a 1-200 mA load step at three different switching frequencies.

B. Output Ripple Voltage and Efficiency

The presence of low-frequency ripple on the output voltage due to variable frequency operation is analyzed in [20] for a boost converter operating in open-loop. In addition to the frequency dependent voltage ripple, the frequency hopping introduces a perturbation due to the frequency dependence of the converter efficiency. The DC output voltage for the synchronous buck converter is obtained by setting s=0 and re-arranging (5) giving:

$$V_{out} = \frac{DV_g}{1 + \frac{R_s}{R_p}} \tag{6}$$

From (6) it is clear that the duty cycle should remain constant while f_s changes in order to maintain a constant output voltage during spread spectrum operation. Equivalently the $t_{on}f_s$ product should remain constant throughout the frequency range to avoid large perturbations in v_{out}. This requirement is automatically satisfied by the architecture of Figure 1 since t_{on} is set by the same delay cells which determine the switching period $1/f_s$.

The simple averaged model [21] from which (5) and (6) are derived does take into account the frequency dependence of the inductor current ripple [21] which leads to a decrease in RMS conduction losses as f_s increases. This reduction in losses is offset by increased switching losses in the output stage [22], resulting in a typical efficiency versus frequency plot shown in Figure 9. The variation in efficiency can be seen as a modulation of R_s in (6) and therefore a step change in the frequency causes a perturbation on v_{out} even if the duty cycle and load remain constant. This undesirable effect

is clearly visible in the transient simulation of Figure 8. The feedback loop eliminates the disturbance on v_{out} following the frequency step. In a practical implementation of the proposed spread spectrum technique, this voltage perturbation can be greatly reduced by setting the LDO bandwidth such that the change in $V_{dd,dl}$ is much slower than $1/f_s$. This in turn allows to the feedback loop to correct the duty cycle as the frequency changes slowly over many switching cycles. Alternatively a digital low-pass filter can be placed in between pseudo-random pattern generator and the DAC.

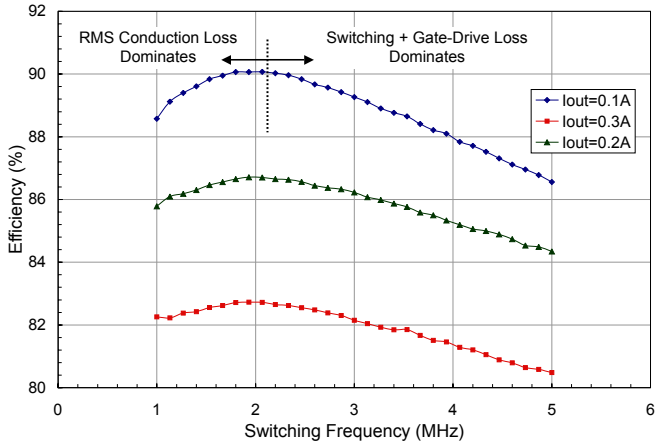


Fig. 9. Measured efficiency versus frequency for the synchronous buck converter. The variation in efficiency leads to a perturbation on the output voltage following a step change in the frequency even if the duty cycle and load are unchanged.

IV. Implementation of the Spread Spectrum Prototype

The spread spectrum system shown in Figure 10 was implemented using a combination of off-the-shelf analog ICs, a complex programmable logic device (CPLD) and a custom power IC. The power IC includes a high-speed power MOSFET half-bridge and gate drivers fabricated in 0.6 μm CMOS technology. The architecture shown in Figure 1 was slightly modified to accommodate the off-chip LDO IC. The LDO has an internal 1.22 V reference, V_{ldo} and is controlled by the buffered DAC output. The buffer and potentiometer would not be required in a fully integrated implementation since the internal LDO reference could be adjusted directly. In this experimental setup, $V_{dd,dl}$ actually corresponds to the core voltage of the entire CPLD chip since the delay-line DPWM supply voltage cannot be isolated. The potentiometer is used to adjust the amount of spread in $V_{dd,dl}$ and hence f_s. The DAC is implemented using the simple 1st order modulator and a first-order passive RC filter. This circuit topology operates over a wide range of input voltages, V_g and provides a low-noise supply voltage for the delay-line DPWM. The delay-line supply voltage is given by:

$$V_{dd,dl} = V_{ldo}\frac{R_1 + R_2}{R_1} - V_{ref}\frac{R_2}{R_1} \qquad (7)$$

A digital offset is introduced after the LFSR in order to position $V_{dd,dl}$ within the acceptable operating range of the CPLD core voltage, from 1.37 V to 1.85 V.

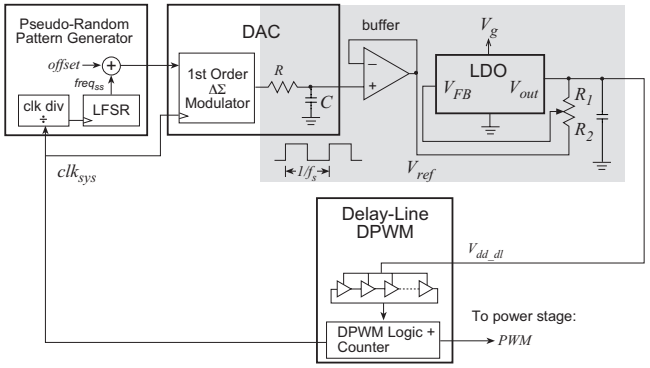


Fig. 10. (a) Topology of the spread spectrum DPWM prototype. The circuits outside the shaded box are implemented using a CPLD.

V. Experimental Results

The frequency versus supply voltage of the DPWM block is shown in Figure 11. The frequency changes from 1.74 MHz to 2.84 MHz for a 480 mV change in $V_{dd,dl}$. The DPWM pulse width tracks the period variation, resulting in a nearly constant effective duty ratio. The duty cycle varies by less than 0.3 % over the operating range. The measured pulse width versus the 7-bit DPWM input code is shown in Figure 12. The slight periodic non-linearity is typical of hybrid DPWMs since the logic delays are non-negligible compared to the delay-line element delay, especially in CPLD/FPGA implementations. This DPWM non-linearity can potentially lead to limit cycle oscillations [23] at certain operating points due to the reduction in the effective resolution. The non-linearity can be minimized in custom on-chip implementations by careful design and synthesis of the DPWM. The hybrid DPWM architecture is guaranteed to have a monotonic delay, avoiding possible instability in the controller feedback loop. The DAC and LDO output voltage waveforms are shown in Figure 14(a) and Figure 14(b), respectively. The digitally generated pseudo-random sequence has a period of approximately 900 ms, which is very close to the $\Delta T_f = 924$ ms predicted by (1). The spread spectrum technique produces a time varying inductor ripple, as shown in Figure 6(b). The drop in efficiency due to the spread spectrum was found to be below 0.1 % at 0.2 A output current. Finally, the EMI spectra shown in Figure 15 demonstrate that the peak conducted EMI is reduced by 23.4 dB with the proposed spread spectrum technique. The prototype specifications are listed in Table I.

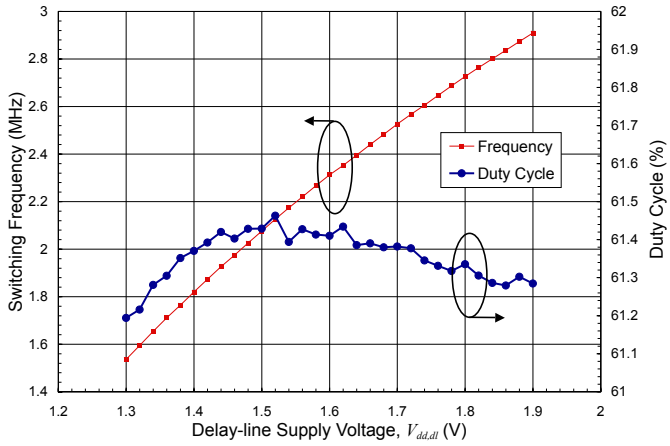


Fig. 11. Measured variation of switching frequency and effective duty cycle with delay-line supply voltage.

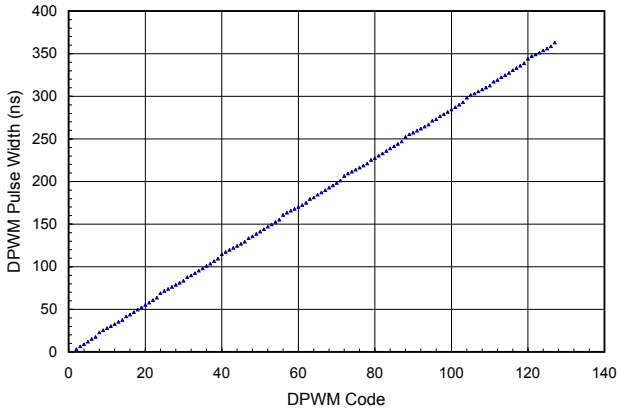


Fig. 12. Measured DPWM pulse width versus code for $V_{dd,dl}$ = 1.8 V.

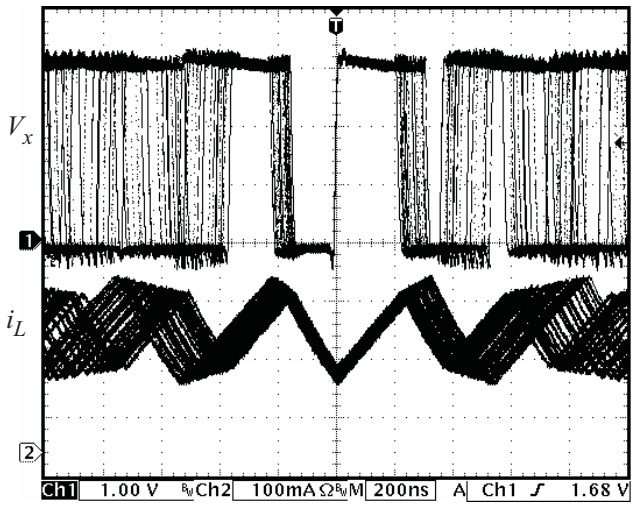
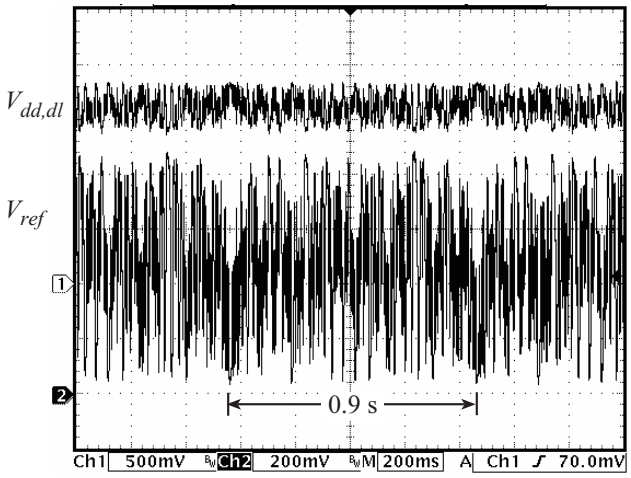
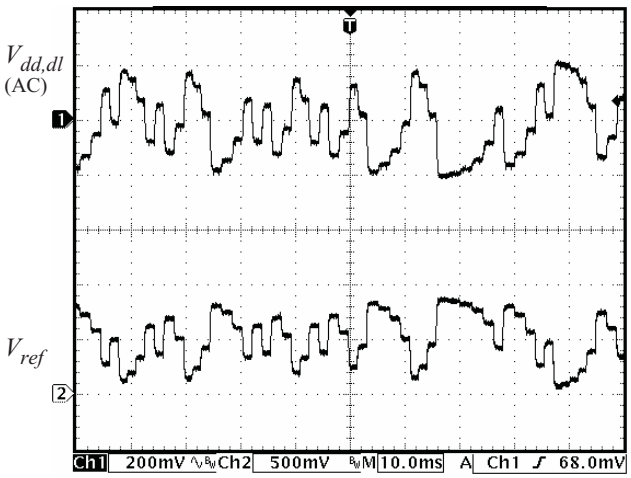


Fig. 13. Switching node voltage and inductor current during spread spectrum operation.



(a)



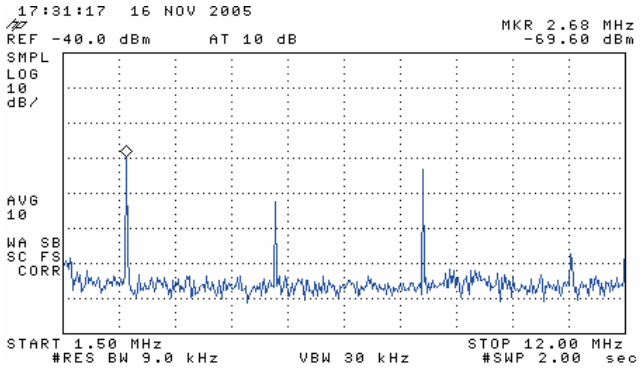
(b)

Fig. 14. (a) Waveforms of the buffered DAC output (channel 2) and delay-line supply voltage (channel 1) when the system operates in spread spectrum mode. (b) The same waveforms are shown with a reduced 10 ms/div time scale and $V_{dd,dl}$ is AC-coupled.

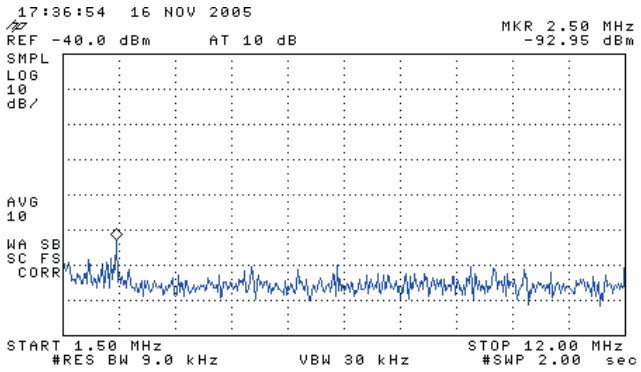
TABLE I

SPECIFICATIONS FOR THE SPREAD SPECTRUM PROTOTYPE

Specification	Value	Units
Input Voltage	2.7-3.6	V
Output Voltage	1.8	V
Rated Output Load	0.5	A
Buck Filter (L/C)	2/4.7	μH/μF
DPWM Resolution	7	bits
Switching Frequency	1.74-2.84	MHz
Delay line Supply Voltage	1.37-1.85	V
$\Delta\Sigma$ Modulator Over-sampling Rate	4096	
Frequency Steps	128	
Reduction in conducted EMI peak	23.4	dB
Period of Pseudo-Random Pattern	0.9	s



(a)



(b)

Fig. 15. (a) Averaged EMI spectrum of the input current to the DC-DC converter with fixed frequency and (b) with the spread spectrum enabled. The spectrum peak is reduced by 23.4 dB at a load current of 0.2 A, V_g = 3.3 V and V_{out} = 1.8 V.

VI. Conclusion

A low-cost spread spectrum architecture compatible with advanced delay- line DPWMs used in low-power digital controllers has been demonstrated. The switching frequency of the buck converter prototype is varied from 1.74 MHz to 2.84 MHz in 128 steps using a pseudo-random 512 cycle pattern, which results in a 23 dB reduction in the conducted EMI peak despite a non-uniform frequency distribution. The proposed architecture is well suited to low-power monolithic implementation can be applied to a wide variety of state-of-the-art digital controllers. Unlike analog controllers, the compensator pole and zero location are shifted due to the variable frequency operation. The resulting affect on the phase margin must be carefully analyzed to avoid stability problems.

VII. Acknowledgments

The authors would like to thank NSERC, CMC, Auto21, U of T open fellowship for their support. The high-frequency power stage used in this work was designed by T. Kawashima and provided by Fuji Electric Advanced Technology Co. Ltd.

References

[1] K. Tse, H. Chung, S. Hui, and S. H.C., "A comparative study of using random switching schemes for DC-DC converters," in *Proceedings, IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 160–166, 1999.

[2] H. Chang, J. Rye, and K. Lee, "Suppression of harmonic spikes in switching converter output using dithered sigma-delta modulation," *IEEE Trans. Industry Applications*, vol. 38, no. 1, pp. 159–166, 2002.

[3] M. Zigliotto and A. Trzymadlowski, "Effective random space vector modulation for EMI reduction in low-cost PWM inverters," in *IEE Int. Conf. on Power Electronics and Variable Speed Drives*, pp. 163–168, 1998.

[4] D. Stone, B. Chambers, and D. Howe, "Random carrier frequency modulation of PWM waveforms to ease EMC problems in switched mode power supplies," in *Proc. 1995 Int. Conf. on Power Electronics and Drive Systems*, vol. 1, pp. 16–21, 1995.

[5] A. Stankovic, G. Verghese, and D. Perreault, "Analysis and synthesis of random modulation schemes for power converters," in *Proceedings, IEEE Power Electronics Specialists Conference*, pp. 1068–1074, 1993.

[6] M. Kuisma, "Variable frequency switching in power supply EMI-control: an overview," *IEEE Aerospace and Electronic Systems Magazine*, vol. 18, pp. 18–22, Dec 2003.

[7] T. Regan and D. La Porte, "Easy-to-use spread spectrum clock generator reduces EMI and more," *Linear Technology Magazine*, pp. 6–12, Feb 2004.

[8] J. Paramesh and A. Jouanne, "Use of sigma-delta modulation to control emi from switch-mode power supplies," *IEEE Transactions on Industrial Electronics*, vol. 48, pp. 111–117, Feb 2001.

[9] D. Maksimović, R. Zane, and R. Erickson, "Impact of digital control in power electronics," in *Proceedings, IEEE International Symposium on Power Semiconductor Devices & ICs*, pp. 13–22, May 2004.

[10] Z. Lukić, K. Wang, and A. Prodić, "High-frequency digital controller for DC-DC converters based on multi-bit Σ-Δ pulse-width modulation," in *Proceedings, IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 35–40, 2005.

[11] K. Drissi, P. Luk, B. Wang, and J. Fontaine, "Effects of symmetric distribution laws on spectral power density in randomized PWM," *Power Electronics Letters*, vol. 1, no. 2, pp. 41–44, 2003.

[12] O. Trescases, G. Wei, and W. Ng, "A segmented digital pulse-width modulator with self-calibration for low-power SMPS," in *IEEE EDSSC'05. Hong Kong Tech. Digest*, pp. 367–370, Dec 2005.

[13] A. Syed, E. Ahmed, and D. Maksimović, "Digital pulse width modulation architectures," in *Proceedings, IEEE Power Electronics Specialists Conference*, pp. 4689–4695, July 2004.

[14] B. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC," *IEEE Transactions on Power Electronic Circuits*, vol. 18, Jan 2003.

[15] D. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, 1997.

[16] A. Prodić and D. Maksimović, "Design of digital PID regulator based on look-up tables for control of high-frequency DC-DC converters," in *Proc. IEEE COMPEL Conf.*, pp. 18–22, 2002.

[17] O. Trescases, Z. Lukic, W. Ng, and A. Prodic, "A low power mixed-signal current-mode DC-DC converter using a one-bit delta sigma DAC," in *Proceedings, IEEE Applied Power Electronics Conference and Exposition*, pp. 700–704, 2006.

[18] G. Wei and M. Horowitz, "A fully digital, energy efficient adaptive power-supply regulator," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 4, pp. 520–528, 1999.

[19] O. Trescases, S. Chen, and W. Ng, "Precision gate drive timing in a zero-voltage-switching DC-DC converter," in *Proceedings, IEEE International Symposium on Power Semiconductor Devices & ICs*, pp. 55–58, May 2004.

[20] M. Kuisma, T. Jarvelainen, and P. Silventoinen, "Analyzing voltage ripple in variable-frequency DC/DC boost converter," in *Proceedings, IEEE Power Electronics Specialists Conference*, pp. 1085–1089, 2004.

[21] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Kluwer Academic Publishers, 2001.

[22] O. Trescases and W. Ng, "Variable output, soft-switching DC/DC converter for VLSI dynamic voltage scaling power supply applications," in *Proceedings, IEEE Power Electronics Specialists Conference*, pp. 4149–4155, June 2004.

[23] H. Peng, D. Maksimović, A. Prodić, and E. Alarcon, "Modeling of quantization effects in digitally controlled DC-DC converters," in *Proceedings, IEEE Power Electronics Specialists Conference*, pp. 4312–4318, July 2004.