A Digital Predictive On-Line Energy Optimization Scheme for DC-DC Converters

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***Abstract*— This work presents a novel energy conservation technique based on predicting the load current of a DC-DC converter that may feed a variety of loads, such as speakers and displays. The predicted load current is used to dynamically adjust the size of the output stage transistors and to switch into PFM mode to maximize the instantaneous converter efficiency. By using a segmented output stage, the trade-off between the gate drive losses and RMS conduction losses can be continuously optimized over the full load current range. The technique relies on the fact that the digital data stream which feeds modern electronic loads can be processed in real-time to predict the load current without relying on explicit current sensing or slow steady-state calibration techniques. The experimental prototype includes a digitally controlled 3.6V-to-1.8V DC-DC converter with an integrated segmented power stage IC operating at 4 MHz. A high-fidelity class-D audio amplifier acts as the DC-DC converter load. The results show a good agreement between the digitally predicted and actual DC-DC converter load current. The total energy consumed for three music pieces was reduced by up to 38% using the automatic mode/segment control technique. The fully digital efficiency optimization technique is well suited to future monolithic integration in advanced CMOS processes.**

I. Introduction

Today's power management ICs targeted for low-power applications (up to several watts) usually employ a number of efficiency improvement techniques to extend battery life. These techniques include multi-mode operation such as PWM/PFM, as well as various forms of dynamic dead-time adjustment [1]–[4] and power stage optimization [5]. In all cases, the power stage operation is optimized according to input voltage and the load current, which may be sensed either directly, through senseFET, Rds_{on}, or indirectly, using sensorless digital algorithms. Existing sensorless digital optimization approaches [4], [6] are cost effective for certain applications but have a limited ability to maximize the efficiency under highly dynamic loads since they rely on the internal signals of the digital control loop under steady state.

There is a growing application sector within the hand-held market where the DC-DC converter load consists of a generic amplifier and a fixed/predictable load. The load may be an antenna, various types of displays/LEDs, a small motor or a power amplifier with speaker, as shown in Figure 1. The proposed efficiency optimization technique is based on load current prediction/feedforward. For a given load impedance, the digital data stream can be processed in real-time to estimate the current in the DC-DC converter and hence the converter efficiency can be optimized accordingly. The digitally fed amplifier is powered from a regulated DC bus and may be implemented using a variety of topologies including class-AB, RF PA or, more recently, class-D. The digital data stream that feeds the amplifier can be processed in real-time and applied as feed-forward to the DC-DC converter in order to reduce the total energy drawn from the battery when subjected to highly dynamic load currents. The technique shown in Figure 1 simplifies the process of efficiency optimization and eliminates the speed bottlenecks. The current estimation is truly predictive in the sense that the current draw can be computed even before it occurs. In this work, the converter efficiency is optimized by dynamically sizing the output stage MOSFETs as described in the following sections.

Increasing the communication and interaction between the load and DC-DC converter can be seen as the next frontier in digitally controlled SMPS. This work demonstrates one of the potential benefits, namely extending the battery life.

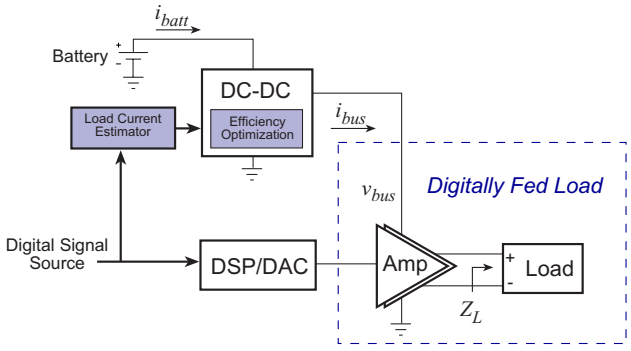

Fig. 1. The proposed efficiency optimization technique is based on load current prediction/feedforward. For a given load impedance, the digital data stream can be processed in real-time to optimize the converter efficiency.

II. Targeting Mid-to-Light Load Efficiency Through Adaptive Power Stage Sizing

The power MOSFETs in a switch-mode power supply are usually sized to achieve the target peak efficiency and current

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handling. For a given process technology, the MOSFET's fixed $Q_{gate}R_{on}$ product can lead to poor efficiency in the mid-to-light load range, where PFM operating mode is typically not effective [5]. This can be overcome by varying the output stage MOSFET's effective W/L ratio on-the-fly [7]–[9]. The total conduction losses in the buck converter are given by:

$$P_{cond} = P_{cond-DC} + P_{cond-AC} \quad (1)$$

$$P_{cond-DC} = I_{out}^2 (DR_{ds,P} + D'R_{ds,N}) \quad (2)$$

$$P_{cond-AC} = \frac{\Delta i_L^2}{12}(DR_{ds,P} + D'R_{ds,N}) \quad (3)$$

where $D' = 1 - D$, Δi_L is the peak-to-peak inductor current ripple, $R_{ds,P} \propto 1/(W/L)_P$ and $R_{ds,N} \propto 1/(W/L)_N$ are the PMOS and NMOS *on*-resistance respectively. The gate drive losses are given by:

$$P_{gate} = f_s(C_{gate,N}V_{gs,N} + C_{gate,P}V_{sg,P}) \quad (4)$$

where $C_{gate,P} \propto (W/L)_P$ and $C_{gate,N} \propto 1/(W/L)_N$ are the PMOS and NMOS lumped gate capacitance, including the gate driver. An approximate derivation in [8] leads to an optimal W/L ratio given by:

$$(W/L)_{opt} \propto \frac{P_{out}}{\sqrt{f_s}} \quad (5)$$

where P_{out} is the output power of the DC-DC converter. The trade-off between the gate drive losses and RMS conduction losses can thus be continuously optimized over the full load range. The block diagram and die photo of the segmented power stage IC, which was originally presented in [5] and used in this work are shown in Figure 2(a) and and Figure 2(b), respectively.

The PMOS and NMOS are each segmented into 7 identical cells whose gate driver inputs are connected in a binary weighted fashion to achieve 3-bits of control. There are 49 possible output stage configurations in synchronous PWM mode since the PMOS and NMOS can be controlled independently. The resulting efficiency curves for several segment enable codes (including PFM) are shown in Figure 3 for $f_{s1} = 4$ MHz. From this plot, it is clearly advantageous to operate with a smaller output stage as the load current is reduced.

III. Application to Class-D Audio Amplifiers

In this work, we demonstrate the load prediction/feedforward concept introduced in Figure 1 on a fully digital, high fidelity class-D amplifier. A popular architecture for a digital class-D amplifier is shown in Figure 4. A digital pulse code modulated (PCM) audio stream with a typical sampling rate of 44.1 kHz is up-sampled and fed to a digital ΔΣ modulator and then to a DPWM block. A one-bit ΔΣ modulator architecture may be used [10], thereby eliminating the need for the DPWM hardware and ensuring high linearity at the output. A passive reconstruction filter is used to extract the original audio signal from the PWM output. The H-bridge output stage is popular for achieving high power supply rejection ratio (PSRR), eliminating the need to AC-coupling capacitors and maximizing the output swing across the speaker terminals. While a THD+N as low as 0.07 % has been reported in a 240 W output stage [11], this class-D architecture operates in open loop with respect to the speaker terminal voltage and it is therefore highly susceptible to non-idealities in the output stage. The distortion introduced by the non-ideal H-bridge transistors can be suppressed using a local feedback loop [12].

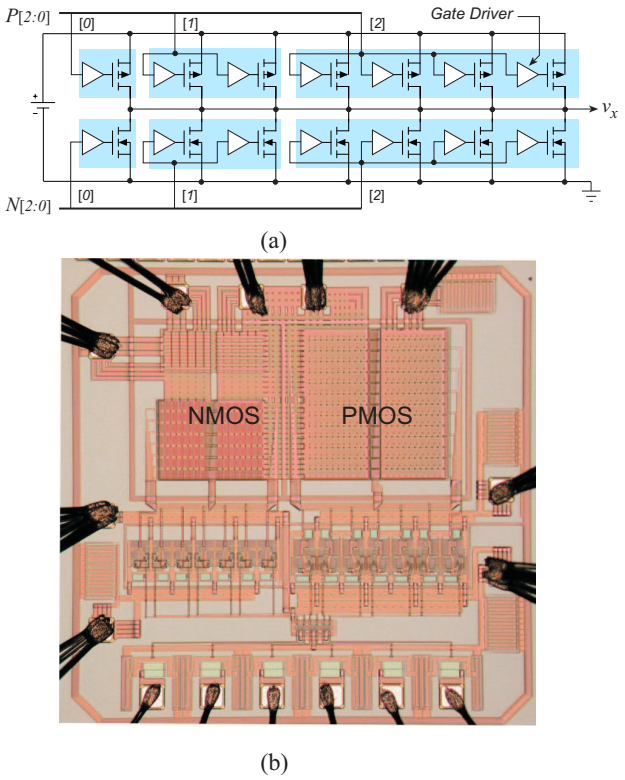

Fig. 2. (a) Architecture of the segmented output stage and (b) die photo of the IC fabricated in a 0.6 μm CMOS process.

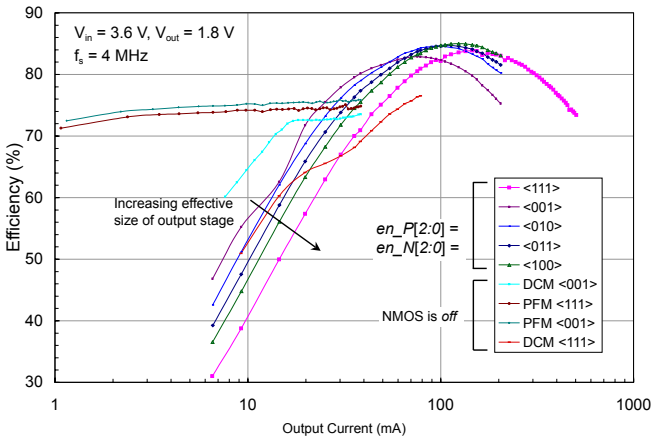

Fig. 3. Measured efficiency versus load for the different segment enable codes and mode of operation. The efficiency is improved by reducing the output stage size for $I_{OUT} \leq 200$ mA

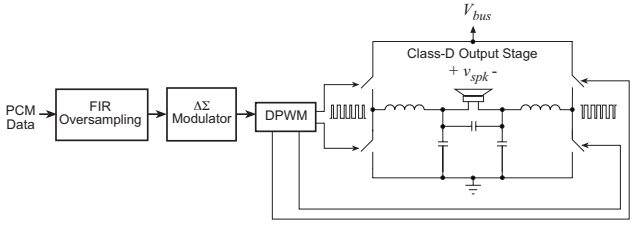

Fig. 4. Simplified architecture of a digital class-D amplifier with an H-bridge output stage.

A. Class-D Amplifier Powered by Upstream DC-DC Converter

Class-D amplifiers have higher efficiency than their class-AB counterparts due to switch-mode operation. In portable applications, the H-bridge may be connected directly to the noisy battery voltage in order to maximize the peak output power:

$$P_{max} = 4V_{batt}^2/R \tag{6}$$

where R is the speaker resistance and V_{batt} is the battery voltage. This generally requires a design with good matching and high PSRR, otherwise the power supply noise severely degrades the THD. In addition, the noise injected onto the battery terminals can lead to conducted EMI problems. A DC-DC converter with tight output regulation may be used to supply the class-D amplifier H-bridge rail, V_{bus}. The resulting combination is equivalent to two cascaded DC-DC converters, where the second converter operates in open-loop. The class-D amplifier therefore has a positive incremental resistance at its input. This greatly simplifies the DC-DC converter compensation compared to PFC applications for example, where a PFC stage is cascaded with a downstream closed loop DC-DC converter having a negative incremental resistance [13].

Using a buck topology in the DC-DC converter is common, though it reduces the maximum peak output power that can be delivered to the speaker compared to (7):

$$P_{max} = 4(V_{batt}D)^2/R \tag{7}$$

where $D \leq 1$ is the steady-state duty cycle of the buck converter. Alternatively, a boost converter may be employed to raise V_{bus} above V_{batt} to increase P_{max}. This is an attractive option in single-cell powered devices when the speaker impedance is constrained by the speaker form factor and high output power is desired. While directly using a boost topology within the class-D output stage is certainly more cost effective, it is not preferable since the inherently non-linear conversion ratio of the boost topology ($M = 1/(1-D)$) leads to high audio distortion.

The switching frequency of the DC-DC converter, f_{s1} can be significantly higher then the switching frequency of the class-D amplifier, f_{s2} . Again, this differs from classical cascaded DC-DC converter design, where the down-stream, or point-of-load converter has the highest switching frequency and bandwidth. In the case of open-loop digital class-D amplification with multi-bit ΔΣ modulators, the switching frequency is limited by the need for extremely high linearity in the DPWM block in order to achieve tight THD specifications ($\leq$0.1%). DPWMs based on delay-lines [14] which are used extensively in digitally controller DC-DC converters to allow multi-MHz switching frequency, are generally unsuitable for high-fidelity class-D amplifiers due to relatively poor linearity. Instead, counter-based DPWMs are used with a PLL-derived clock frequency of $2^N f_{s2}$ or $2^{N+1} f_{s2}$ for edge aligned and center aligned N-bit PWM respectively [15]. The power and THD trade-off between counter and delay-line based DPWMs for class-D amplifiers is well covered in the literature [16].

The single-channel class-D amplifier architecture used in this work is shown in Figure 5. It includes an audio DSP IC, a digital pulse-width modulator (DPWM), a full-bridge differential output stage and an analog *LC* reconstruction filter. The PCM audio data, which has a sampling rate of f_{s2} = 44.1 kHz, is processed by the specialized DSP IC that includes a PLL, a FIR 8× interpolator, and a ΔΣ modulator. The audio stream is also fed to the digital load current predictor and segment controller, as explained in the following section.

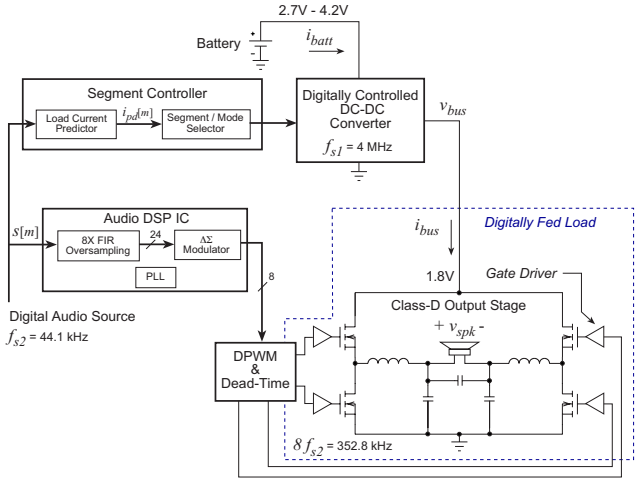

Fig. 5. Simplified diagram of the DC-DC powered class-D audio amplifier system. A sensorless digital current predictor is used to dynamically optimize the power stage sizing and switch between PFM/PWM based on the digital audio stream.

B. DC-DC Converter Load Prediction for Efficiency Optimization

The audio stream data, $s[m]$ is converted into a differential speaker voltage $v_{spk}(t)$ by the class-D amplifier. Assuming that the speaker load can be approximated with a linear admittance $Y(j\omega)$, then the speaker current $i_{spk}(t)$ can be predicted by feeding $s[m]$ into a $Y(z)$, where $Y(z)$ is the discrete-time equivalent of $Y(j\omega)$. For a sinusoidal speaker voltage $v_{spk}(t) = V_{spk}sin(\omega)$, the input current to the class-D amplifier is non-linear with respect to the audio data, since it is proportional to the instantaneous power in the speaker and occurs at 2ω:

$$i_{bus}(t) = \frac{i_{spk}(t)v_{spk}(t)}{V_{bus}\eta} = \frac{I_{spk}Vspk}{2V_{bus}\eta}(cos\phi - cos(2\omega t + \phi)) \tag{8}$$

where V_{bus} is the regulated output voltage of the DC-DC converter, ϕ is the phase between $v_{spk}(t)$ and $i_{spk}(t)$ and η

is the class-D amplifier efficiency. For many loads, even a crude resistive approximation of $Y(j) \approx 1/R$ can lead to a reasonably accurate prediction of the DC-DC converter load current $i_{bus}(t)$, as demonstrated by the experimental results. In this case, (8) can be simplified to the frequency independent estimate given by,

$$i_{bus}(t) = \frac{v_{spk}^2(t)}{V_{bus}\eta R} \propto v_{spk}^2(t) \tag{9}$$

The block diagram of the segment/mode controller and digitally controlled DC-DC converter used in this work are shown in Figure 6. The segment/mode controller is clocked at the audio sampling rate of f_{s2} = 44.1 kHz and thus consumes very little dynamic power despite the need for a hardware multiplier. The 8 most significant bits of the audio signal $s[m]$ are first squared, truncated and then fed to an array of digital comparators to generate the thermo-code CMP[6:0]. A 2-to-1 multiplexer is used with each comparator to implement hysteresis in the segment selection process. An area efficient look-up table (LUT) stores the thresholds based on the efficiency measurements presented in Figure 3. The output of the comparators is encoded into the 3-bit segment enable codes enP and enN. The combination of enP= enN = 0 is used to encode the PFM operating mode, where the synchronous rectifier is disabled. Finally the data is sent asynchronously to the DC-DC converter, allowing independent selection of f_{s1} and f_{s2} for maximum flexibility. In general, it is desirable to synchronize the DC-DC converter clock to the class-D amplifier clock to reduce the ripple on the V_{bus} capacitor, however this might not be practical in multi-chip solutions where the high frequency clocks should remain on-chip to minimize noise. Using the flexible approach of Figure 5, the optimal segment code is computed every audio sample. A programmable delay buffer is used to account for the inherent latency of the class-D audio signal path.

The DC-DC controller includes a self-oscillating hybrid delay-line based DPWM, a digital compensator, a windowed ADC, a dead-time circuit and a PFM regulator. The 3-bit gating pulses for the power stage are generated within the dead-time block based on the received enable codes. The internal enable codes are updated on the falling edge of the DPWM signal to ensure glitch-free operation.

IV. Experimental Results

The system shown in Figure 5 was implemented using a combination of off-the-shelf and custom designed components, including two low-cost FPGAs and two custom designed ICs. A miniature speaker was used to provide a realistic load for the amplifier. A standard CD player having an optical output was used as the digital audio source. The output of the digital current predictor block, $i_{pd}[n]$ is shown in Figure 8 and Figure 9, along with the actual DC-DC converter load current $i_{bus}(t)$. An 8-bit FLASH D/A was used to display $i_{pd}[n]$ on an analog oscilloscope for convenience. A good matching between $i_{pd}[n]$ and $i_{bus}(t)$ is achieved despite the complex impedance of the speaker. Slight phase and amplitude errors in $i_{pd}[n]$ are inevitable due to simplified load prediction

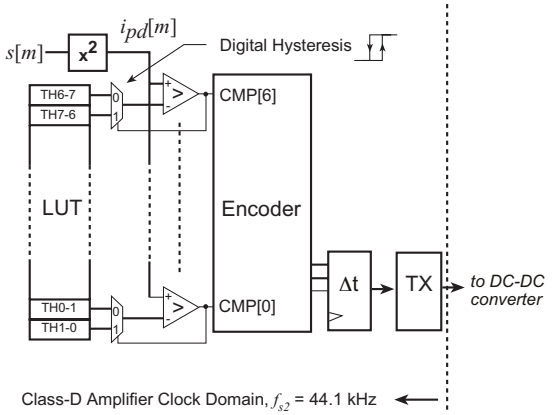

Fig. 6. The segment controller and digitally controlled DC-DC converter communicate using an asynchronous interface.

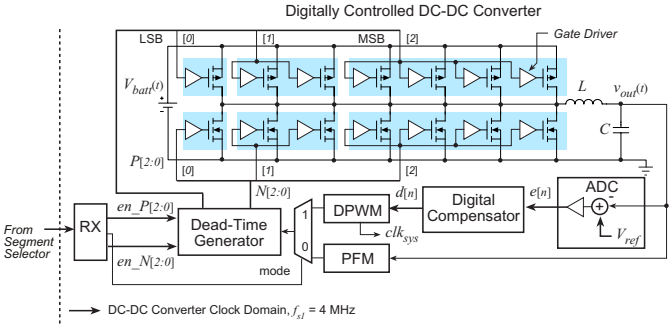

Fig. 7. Digitally controlled DC-DC controller architecture.

technique. These phase errors result in the temporary selection of the non-optimal segment code but the overall energy is still significantly reduced.

The dynamic operation of the segment controller during audio playback is shown in Figure 10. The converter remains in PFM mode for $seg[2:0] = 0$. The segment codes clearly follow the changes in $i_{pd}[n]$. The automatic PWM-PFM transition is shown in Figure 11 during audio playback. The opposite situation in shown in Figure 12.

The total energy flowing into the DC-DC converter was measured for three varieties of music pieces in order to gauge the effectiveness of the segment/mode control scheme. The results are given Table I. Despite the obvious limitations in the accuracy of the load current estimation, the total energy was reduced by a maximum of 38 %, when compared to operating without PFM mode and with all segments *ON*, proving the merit of this sensorless efficiency optimization technique. In a separate test, PFM mode was disabled and energy savings of up to 20 % were observed when segment control was activated. Similar power savings can be expected with other loads present in handheld devices, such as displays. The distribution of selected segment enable codes can be computed based on the thresholds which were programmed in the segment selector of Figure 6. The result is shown in Figure 13 for the audio sample listed as song 1 in Table I. Based on the current thresholds extrapolated from the efficiency characterization of Figure 3, the converter seldom operates with all segments *on*, which

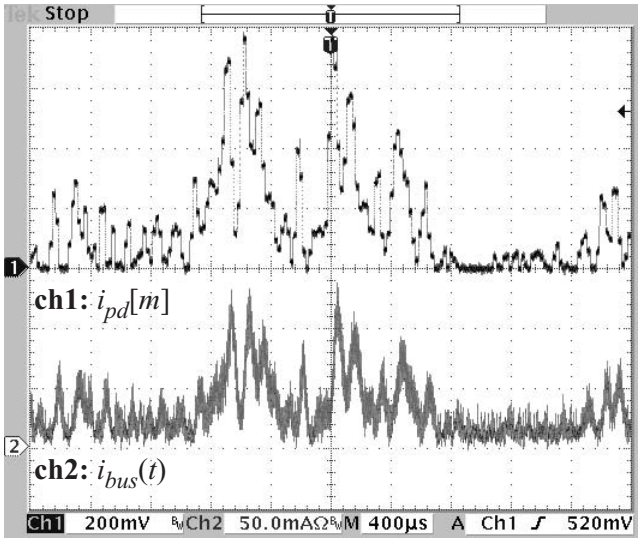

Fig. 8. Predicted (ch1) and actual (ch2) DC-DC converter load current with a speaker load. The predicted current $i_{pd}[n]$ is shown using an 8-bit FLASH D/A.

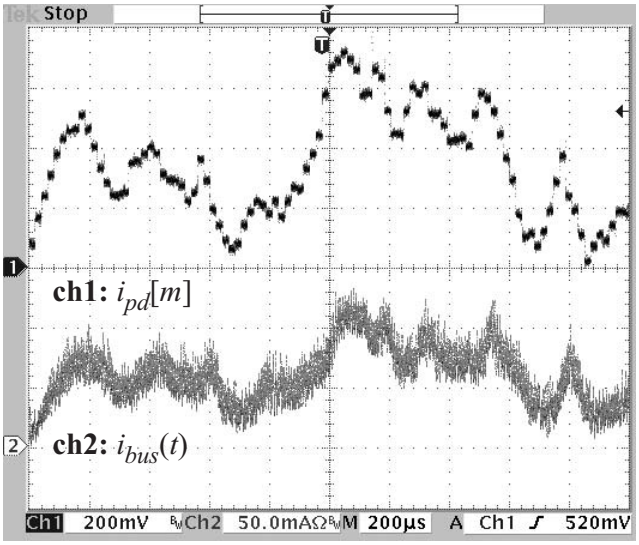

Fig. 9. Predicted (ch1) and actual (ch2) DC-DC converter load current with a speaker load. The predicted current closely tracks the actual load current in the class-D amplifier.

explains the efficiency improvement observed in Table I. In general, it can be concluded that while the power stage must be sized to delivered the desired peak power, it is more efficient to operate with a smaller effective W/L ratio during most of the audio playback. Clearly the overall energy consumption reduction varies on a number of factors including the DC-DC converter power stage sizing, the energy distribution of the audio sample and the playback volume.

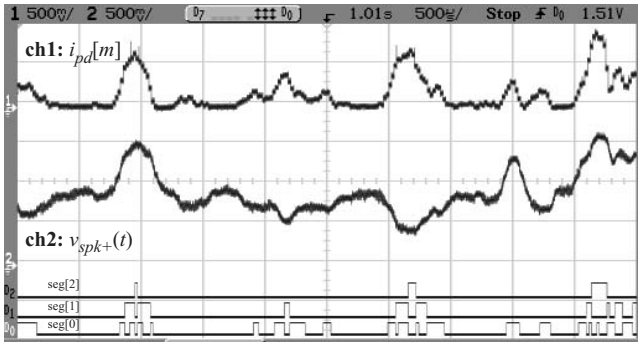

Fig. 10. Predicted DC-DC load current: (ch1) speaker terminal voltage (ch2); and segment enable codes during audio playback. A segment code of *seg*=0 indicates that the converter operates in PFM mode

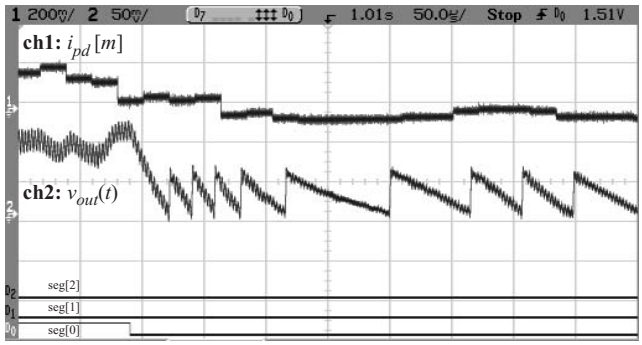

Fig. 11. Predicted DC-DC load current: (ch1) and regulated output voltage (ch2-AC coupled) during a transition from PWM to PFM mode. The load current varies continuously during audio playback and hence this does not correspond to a traditional load step response.

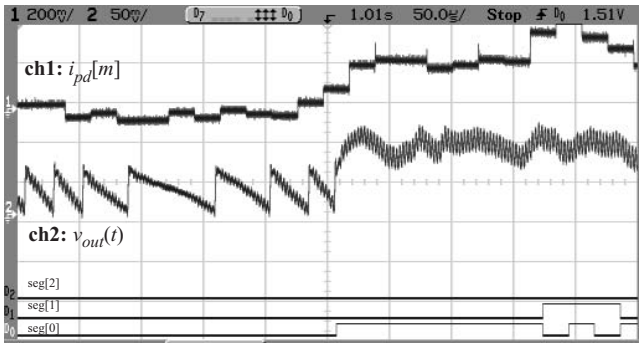

Fig. 12. Predicted DC-DC load current: (ch1); and regulated output voltage (ch2-AC coupled) during a transition from PFM to PWM mode.

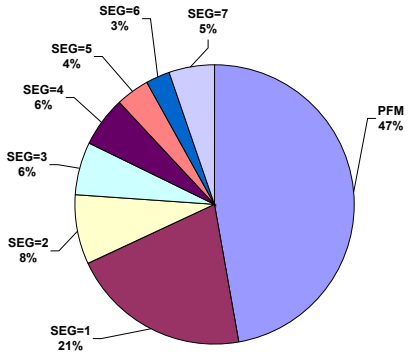

Fig. 13. Plot showing the percentage of audio samples falling into each category of the enable code range used in this work. This data was calculated using the current thresholds encoded in the segment selector and the full scale audio sample listed as song 1 in Table I.

TABLE I

TOTAL ENERGY CONSUMPTION WITH AND WITHOUT AUTOMATIC SEGMENT/MODE CONTROL

Song Type	Length (s)	Total Energy Consumption (J)		**Savings** (%)
		All ON	Automatic Control	
1. Rock	149	11.16	8.80	**21.2**
2. Classical	380	23.77	17.18	**27.7**
3. Jazz	140	7.08	4.36	**38.3**

V. CONCLUSION

A novel energy conservation technique based on predicting the load current of DC-DC converters has been demonstrated. The predicted load current is used to dynamically adjust the size of the output stage transistors operating at a switching frequency of 4 MHz and to switch into PFM mode to maximize the instantaneous converter efficiency in real-time. Energy savings of up to 38 % were observed when automatic segment/mode control was enabled. The simple current prediction technique is fully digital/synthesizeable and hence is well suited to future monolithic integration in advanced CMOS processes. In general, it can be concluded that while the power stage must be sized to delivered the desired peak power, it is more efficient to operate with a smaller effective W/L ratio during most of the audio playback.

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