Output Stages for Integrated DC-DC Converters and Power ICs

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\textbf{Abstract} – Integrated switched mode power supplies and incorporate large amount of complex mixed-signal control circuits as well as the power transistors on the same die. CMOS compatibility is a very important consideration when designing monolithic DC-DC converters. This paper examines the different power output stage designs and identifies the key device characteristics such as on-resistance, gate capacitance, switching speed that ensure optimized power conversion efficiencies. An integrated 1W, 4MHz multi-mode DC-DC converter with Segmented Output Stage and a peak power conversion efficiency of 88\% is used to illustrate various design trade-offs.

\section{I. \textbf{POWER OUTPUT STAGES}}

The output stage configuration in smart power integrated circuit (PIC) is highly dependent on the availability of the power devices and choice of fabrication process. The key design issues are the device breakdown voltage, current handling capability, switching speed and process compatibility. Once these initial requirements are satisfied, the attention should be turned to the optimization of the performance of the output stage(s) and the overall system.

Most smart PICs are designed for switched mode operation. With the power devices operating in fully on or fully off modes, on-chip power dissipation can be minimized. The half and full or H-bridges (Fig. 1 and 2) are the most common switching output configurations in smart PICs: In both cases, the output transistors are called the high side (HS) driver or the low side (LS) driver, depending on its placement with respect to the power supply rail. The LS driver is normally an n-channel power MOSFET (n-MOS) with both its source and body connected to ground potential. The HS driver can be either another n-MOS (Totem pole output stage) or a p-MOS (push-pull output stage).

\section{II. \textbf{N-MOS HIGH-SIDE DRIVER}}

The choice on which configuration to use is normally determined by the output power level. For high voltage and high current applications (e.g. 10's of volts and several amperes) it is more advantageous to use n-MOS as the HS driver. The higher electron surface and bulk mobilities would lead to a smaller device area when compared to a p-MOS for a given on-resistance. However, the drawback using an n-MOS as the HS driver is due to fact that a floating source n-MOS is required. In addition, in order to turn the HS driver on and off properly, a gate drive voltage that is higher than the supply rail \(V_{DD}\) is required. This voltage is normally generated using an on-chip bootstrap circuit (with integrated diode as seen in Fig. 2.).

Since the power devices are required to support high supply voltage, the extended drain MOSFET (EDMOS) structure is normally employed [1]. An integrated H-bridge fabricated using a 40V CMOS compatible process [2] with floating source n-type EDMOS transistors for the HS and LS drivers is as shown in Fig. 3. This output stage was designed for a 40W Class D power amplifier. The use of n-type EDMOS as the power transistors allowed an area efficient design with on-chip protection circuits, gate drivers, and bootstrap circuits. Both the HS and LS drivers have on-resistances of 220m\(\Omega\). With a supply voltage of 25V, the maximum efficiency achieved was 88\%.

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III. CMOS PUSH-PULL OUTPUT STAGE

In low power, low voltage DC-DC converter applications (e.g. battery powered, 1W operation), the amount of current that needs to be handled by the HS driver is normally less than 1A. In this case, conventional CMOS device structures such as those shown in Fig. 4 would be idea candidates for the HS and LS drivers. No additional process changes to the standard CMOS technology is needed, making this approach highly economical and attractive. In addition, the fact that a p-MOS is used as the HS driver, the gate drive signal can be the same PWM (Pulse Width Modulation) waveform with appropriate dead-times.

Although the hole surface mobility is approximately three times lower than that for electron, it is often not necessary to design the HS p-MOS driver to have three times the area as the LS n-MOS driver. Since the duty cycle of PWM signal is approximately equal to the ratio of the output to input voltage,

\[
\text{Duty Cycle} \approx \frac{V_{\text{out}}}{V_{\text{in}}}
\]

the average duration that the HS driver turns on is not 50%. For example, with a Li-ion battery input voltage of 4.2V and an output voltage of 1.0V, the duty cycle for the HS and LS drivers are 24% and 76%, respectively. In order to achieve the best conduction loss versus efficient use of area, the on-resistance of the p-MOS can be approximately three times higher \((76/24 \approx 3)\). Therefore, the device areas for both the n-MOS and p-MOS do not necessarily have to be in a ratio of 1:3.

IV. SEGMENTED OUTPUT STAGE

Once the size of the HS and LS drivers are determine for a particular peak conversion efficiency, output current and switching frequency, the overall performance of the output stage can be further improved by optimizing the switching loss. The typical source of power losses in a DC-DC converter is as shown in Fig. 5. The output stage is responsible for the gate drive and conduction loss. The gate drive loss, \(P_{\text{gate}}\) is dominant at low output current (see Fig. 6) and is given by

\[
P_{\text{gate}} = \frac{f_s}{2} \left( C_{\text{gate},N} + C_{\text{gate},P} \right) V_{\text{in}}^2
\]

\(P_{\text{gate}}\) is proportional to the size of the n-MOS and p-MOS drivers. If smaller size power transistors can be selected at low output current, \(P_{\text{gate}}\) can be reduced. This will maintain high power conversion efficiency over a wide range of output current.

![Various power losses in a DC-DC converter.](image)

![Typical power conversion efficiency versus output current. Gate drive and controller losses dominate in the low output current range. Conduction loss is more prominent at high output current.](image)
The circuit configuration of the \textit{p}-MOS and \textit{n}-MOS drivers in a traditional output stage, as shown in Fig. 7, can be partitioned into parallel combinations of identical transistors. These transistors can be further grouped into three independently controlled segments to achieve a binary weighting of size 1, 2, and 4. The gate drive signals are connected to individual gate drivers such that only the gate capacitances of the selected segments are switched. With a digitally controlled DC-DC converter [3], different segment size can be selected according to output current. This allows dynamic optimization of \( P_{\text{gate}} \).

This segmented output stage (see Fig. 8) was implemented using a 0.18\( \mu \)m standard CMOS technology with a maximum breakdown voltage of 5V. The active device areas for the HS and LS drivers were chosen to minimize the conduction loss for an input voltage range of 2.7 to 4.2V and an output voltage of 1.8V with a maximum output current of 500mA. The \textit{n}-MOS and \textit{p}-MOS transistors have active areas of 0.075 and 0.20mm\(^2\), respectively. The layout of the output stage employed a hybrid waffle configuration as shown in Fig. 9. The transistor fingers are arranged in a square grid where the source and drains are connected using diagonally running metal lines. Initial observation suggests that most silicon area is allocated to in-active area and may result in high on-resistance. However, the diagonal metal lines used to connect drain and the source terminals can now be made wider than if minimum geometry was used. This approach allows the device on-resistance and interconnect resistance to be optimized.

The measured range of on-resistance and gate drive power loss (Gen2) and previously published data (Gen1) are as plotted in Fig. 10. As the transistor size changes from a normalized size of 1 to 7, the gate drive power also increases proportionally for both \textit{n}-MOS and \textit{p}-MOS. However, the on-resistance reduces from 1.72\( \Omega \) to 0.3\( \Omega \) for the \textit{n}-MOS.

The efficiency measured at low output current range. By contrast, with en for \( V_{\text{in}} = 2.7V \) with different enable codes are shown in Fig. 11. Enable code of \(<111>\) is equivalent to pMOS Drivers

\begin{itemize}
\item \textit{p}-MOS
\item \textit{n}-MOS
\end{itemize}

nMOS Drivers

\begin{itemize}
\item \textit{p}-MOS
\item \textit{n}-MOS
\end{itemize}

Fig. 8. A segmented output stage fabricated using a 0.18\( \mu \)m CMOS technology. The \textit{n}-MOS and \textit{p}-MOS have active areas of 0.075 and 0.20mm\(^2\), respectively.

![Fig. 7. Schematic of a traditional CMOS push-pull output stage with two large gate drive circuits for the high-side and low side switches. The segmented output stage is basically a re-organization of the same layout with transistor segments grouped into size of 1, 2 and 4.](image)

Fig. 9. Basic cell for the power MOSFET hybrid-waffle layout structure.

![Fig. 10. Measured on-resistance and gate drive loss for the segmented output stage, ranging from the smallest to the largest segment size. Generation 2 is an improvement over previously published data [3].](image)

![Fig. 11.](image)
select all transistor segments, hence the largest transistor size. The power conversion efficiency is highest for large current, but suffers significantly at low output current range. By contrast, with enable code of $<001>$, only the smallest segment is selected. The power conversion efficiency is now highest at low current and reduces as the output current increases. Also included in Fig. 11 are the power conversion efficiencies for the PFM (Pulse Frequency Modulation) and DCM (discontinuous mode) for the largest and smallest power transistor sizes. For very low output current, it is much more advantageous to switch from PWM to PFM mode. With the use of a digital controller [3], the optimal enable codes and operating mode (PWM or PFM) can be selected such that the peak power conversion efficiency can be maintained over the widest possible output current range. Using this approach, the converter achieved a peak efficiency of 88%. This is a significant improvement by a maximum of 6.2% when compared to the non-segmented case as shown in Fig. 12. The peak efficiency is limited by the relatively high inductor series resistance and high-switching losses in the power stage at 4 MHz.

V. CONCLUSIONS

This paper examined different CMOS compatible output stage configurations that are suitable for smart PIC implementation. $n$-channel EDMOS structures are more attractive for the HS driver in totem pole output stages in high voltage, high current applications. Standard CMOS technologies can be used to implement push pull output stages in battery operated low power applications. The Hybrid Waffle layout technique is effective in providing a better trade-off between device on-resistance and metal interconnect resistance. Further optimization of the power conversion efficiency over a wide range of output current can be realized by using segmented output stages and multi-mode operations.

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VII. REFERENCES


Fig. 11. Measured efficiency versus output current for $V_{in} = 2.7$ V. The curves correspond to 5 different segment combinations out of 49 since the NMOS and PMOS use the same enable code.

Fig. 12. Measured efficiency versus output current for $V_{in} = 2.7$ V. In the top curve, the optimal segments are enabled by selecting the appropriate segment size according to the output current. The bottom curve is achieved if segmentation is not used.