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High Performance Low-Voltage Power MOSFETs with Hybrid Waffle Layout Structure in a 0.25µm Standard CMOS Process

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***Abstract*—This paper reports on a low-voltage CMOS power MOSFET layout technique, implemented in a 0.25µm, 5-metal layers CMOS process that is suitable for high speed switching power devices. The proposed hybrid waffle (HW) layout technique organizes MOSFET fingers in a square grid (waffle) arrangement. It is designed to provide an effective trade-off between the width of diagonal source/drain metal and the active device area, allowing more effective optimization between switching and conduction losses. In comparison with conventional multi-finger (MF) layouts, the HW layout is found to exhibit a 30% reduction in overall on-resistance with 3.6 times smaller total gate charge for CMOS devices with a current rating of 1A. Integrated DC-DC buck converters using HW push-pull output stages are found to have higher simulated power conversion efficiencies at switching frequencies beyond multi-MHz.**

I. INTRODUCTION

In recent years, extensive research activities are focused in the area of low-voltage (sub-10V) smart power integrated circuits for various portable applications. For integrated switch mode power supplies (SMPS), power MOSFETs have become the standard choice for the switching devices. Also, today's integrated DC-DC converters, for mobile applications, require low-voltage power MOSFETs with low on-resistance (R_{ON}) and low gate charge (Q_G) to provide a high power conversion efficiency in the multi-MHz (>5MHz) range. Since gate-drive and switching loss are proportional to Q_G and the switching frequency (f_s) while the conduction loss depends on the on-resistance (R_{ON}) [1], it is necessary to minimize both parasitic resistance and capacitance as illustrate in Fig 1. Traditionally, large CMOS transistors are designed with multi-finger layout structure (see Fig. 2a) to maximize the channel width (W) per unit area (A). Alternatively, regular waffle layout design was introduced to further improve the W/A ratio by sharing each source/drain contact with four neighboring transistors. This layout structure was able to offer a lower R_{ON} via a higher W/A ratio [2]. However, the MF and regular waffle layout approaches can no longer satisfy the quest for high switching frequency and power conversion efficiency simultaneously. Large parasitic interconnect resistances and capacitances arising from the narrow metal and poly-silicon line width and spacing are the limiting factors.

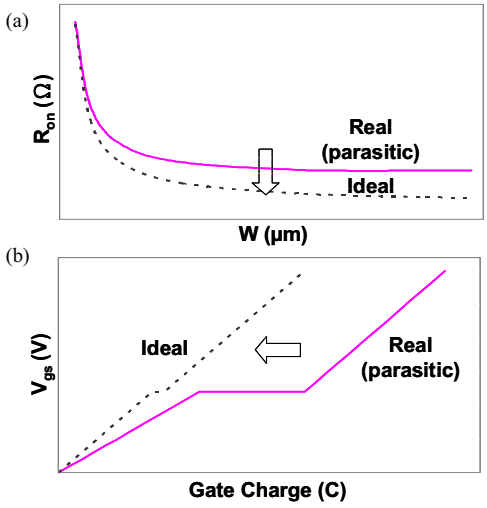

Fig. 1. Parasitic effects: (a) On-Resistance and (b) Gate Charge Trends

In this paper, we introduce a new layout strategy named the "hybrid waffle" structure that will further minimize parasitic interconnect resistances and capacitances. For verification purpose, the performance of a DC-DC converter with different types of transistor layout for the output power stage is studied. The power transistors are n- and p-MOSFETs based on a standard 0.25µm CMOS process technology. The power conversion efficiencies for the DC-DC converter with power transistors in multi-fingers (MF) and hybrid waffle

(HW) layout structures are simulated. The power transistors have the same voltage rating and operate under the same switching frequency and loading condition.

II. Device and Efficiency Simulation Models

In order to compare the dynamic and DC characteristics of the multi-fingers (MF) and hybrid waffle (HW) layout structures, several sample devices with different layouts and schematics were constructed in Cadence Virtuoso to facilitate HSPICE simulation. Fig. 2 and 3 illustrate the simplified layout and schematic model representation of the MF and HW structures, respectively. It is important to note that parasitic resistances from each physical design layer were considered in these schematic models. For more precise simulation analysis, each transistor finger is partitioned into several small unit transistors with one contact for each source/drain.

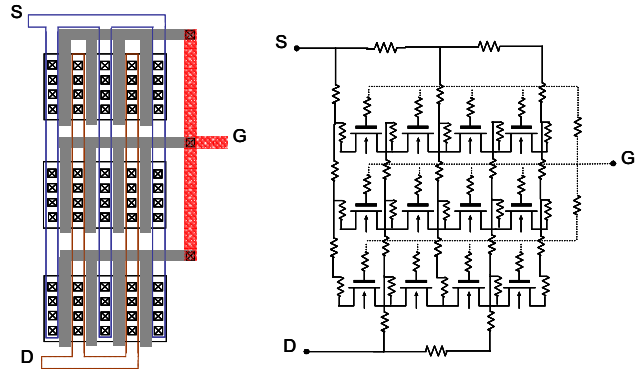

Fig. 2. Multi-fingers structure: (a) Layout and (b) Schematic.

At first inspection, the hybrid waffle layout, as show in Fig. 3(a), appears to have sub-optimal use of silicon area. Much of the layout area is occupied by metal interconnection rather than the active area. However, the wider metal interconnections can in fact lower the overall on-resistance of the power transistors, especially for low voltage CMOS devices. In addition, the reduced overall W and source/drain junctions will result in a lower gate and parasitic capacitance. In this layout, metal runners are composed of stacks of 3 levels of metallization to reduce de-biasing effects and the possibility of electromigration. Also, metal 2 is used exclusively to connect all the poly-gate electrodes. This further reduces the distributed gate resistance and allows much faster switching operation.

To verify device performance, a synchronous buck converter shown in Fig. 4 is implemented with Simulink in MATLAB to calculate the overall efficiency. Device parameters required for efficiency calculation are extracted from the corresponding HSPICE models. Efficiency calculations are performed with power loss analysis described in [3, 4]. Simulations are performed with high-side (HS) and low-side (LS) switches in MF or HW layout structures. The simulation results of a buck converts based on both MF and HW power MOSFETs will be summarized in the next section.

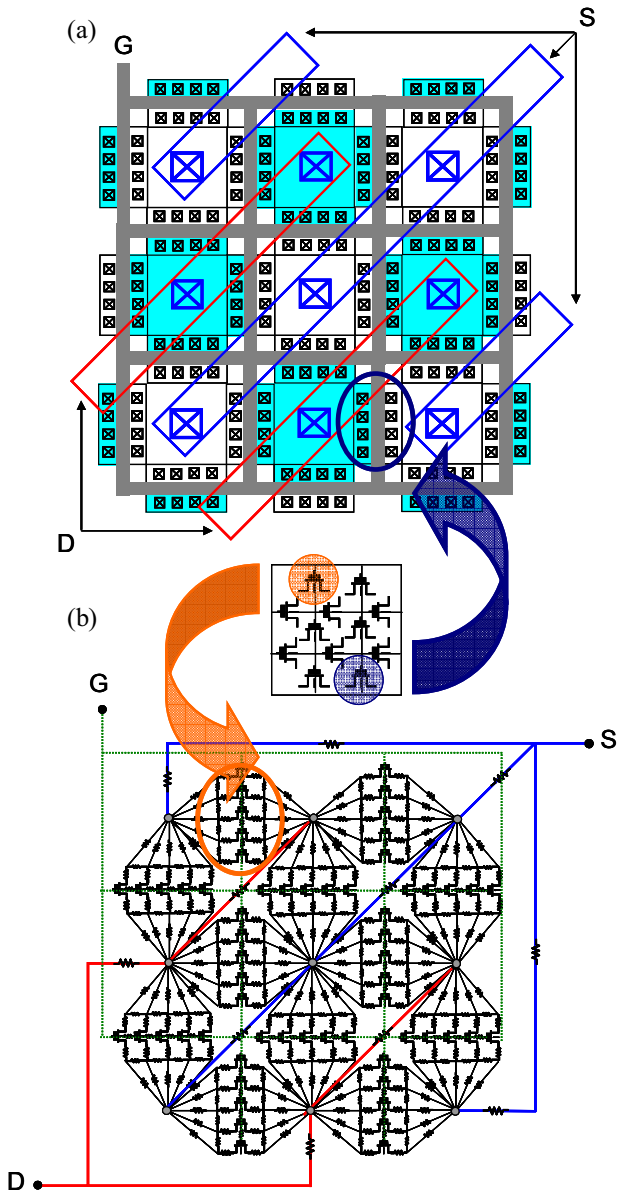

Fig. 3. Hybrid waffle structure: (a) Layout and (b) Schematic.

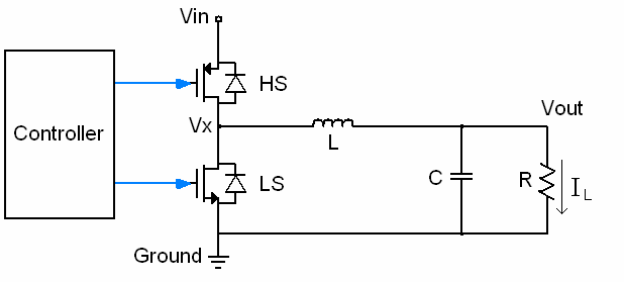

Fig. 4. Synchronous Rectifier Buck Converter.

III. Simulation Results and Discussions

The nonlinearity of the parasitic capacitances, and the often incomplete specification on their variation over the full range of relevant voltages, make gate circuit design by conventional methods exceedingly difficult. To overcome this problem, it has become standard practice to calculate the total gate charge (Q_G) that has to be supplied in order to establish a particular drain current under given test condition. Therefore, instead of extracting parasitic capacitances, the gate charge waveforms for both MF and HW structures are simulated based on our earlier schematic models, as shown in Fig. 5.

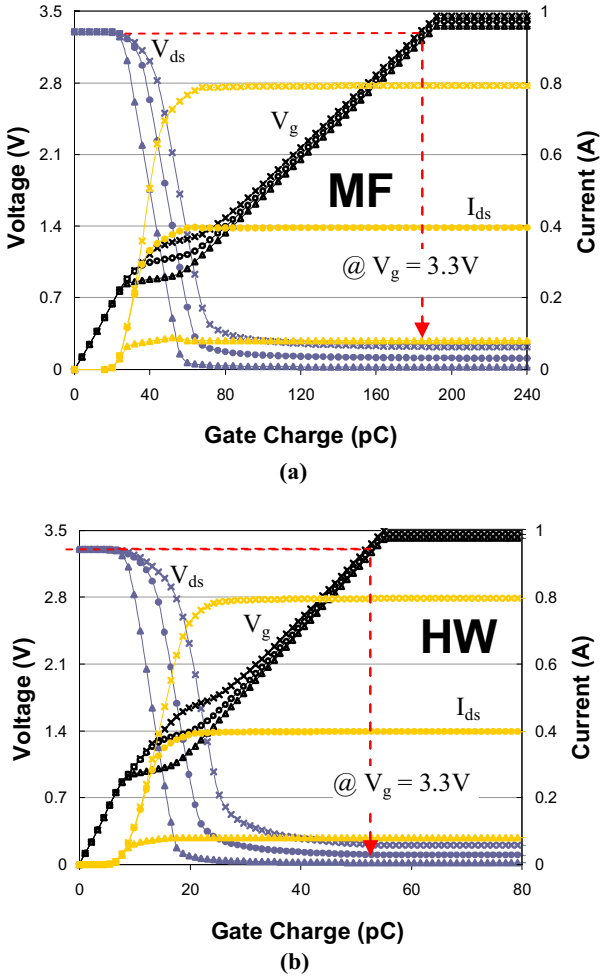

Fig. 5. Gate charge characteristics of (a) MF and (b) HW structures

X: @ I_{ds}=800mA, ○: @ I_{ds}=400mA, △: @ I_{ds}=80mA

When V_{GS} reaches a threshold voltage, its drain current starts to rise. However, the rise of V_{GS} is only continued until its drain current starts to saturate. At this point, the drain voltage of the device starts to fall and this makes the gate current to discharge the Miller capacitance, C_{GD}. Since the time to discharge this parasitic capacitance is mainly depending on the magnitude of C_{GD}, it is required to minimize the C_{GD} or Q_{GD}. However, the change in I_{DS} affects Q_{GS} rather than Q_{GD}. Nevertheless the total gate charge of HW structure is about 3.6 times smaller than that for the MF structure at V_G = 3.3V. This is due to the fact that the total W for the MF structure is more than 3 times wider than the HW structure for the same chip area, thus smaller Q_{GD}.

Fig. 6 illustrates the R_{ON} and Q_G trends for the MF and HW structures as a function of transistor size. It is interesting to note that the R_{ON} trends for MF and HW structures cross over at Area = 0.066 mm^2. This indicates that with a large enough device area, the HW structure can minimize and achieve smaller overall R_{ON} through reduction of parasitic resistances due to wide metal connections even though the W/L ratio of HW structure is smaller than the MF's. Since a small FOM = $R_{ON} \times Q_G$ value for power MOSFET generally leads to a high DC-DC converter efficiency, HW structure is expected to have a higher power conversion efficiency than that of MF's.

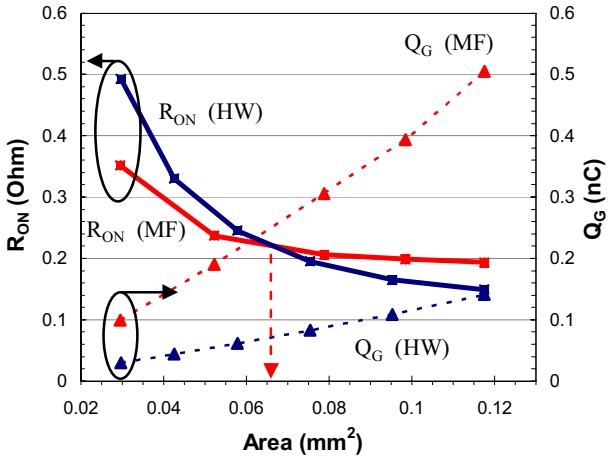

Fig. 6. R_{ON} and Q_G plots as a function of MF and HW power MOSFET active areas.

Finally, for verification purpose, the power conversion efficiencies under different load conditions have been simulated using the Simulink model described in section II. Efficiencies are plotted versus switching frequency. As expected, MF structure provides a better power conversion efficiency at lower MHz switching operations, thus is the choice of switching device nowadays. However, the cross-over of efficiency as frequency increases shows that HW is the preferred structure for power MOSFETs. Also, at light loads, the switching and gate drive losses (which are directly proportional to Q_G) dominate over conduction loss. Thus, with a smaller gate charge or input capacitance, HW structure provides higher light-load efficiency.

Comparing with the conventional MF layout structure, the proposed HW design demonstrates smaller FOM even if its overall on-resistance at the small die area is higher than that of MF's. This is due to a relatively smaller Q_G data of HW structures, as summarized in Table 1. Lastly, it is interesting to

note that this performance gain can be achieved based on layout techniques without additional processing step or change, and will be very attractive for future low voltage integrated DC-DC converter designs.

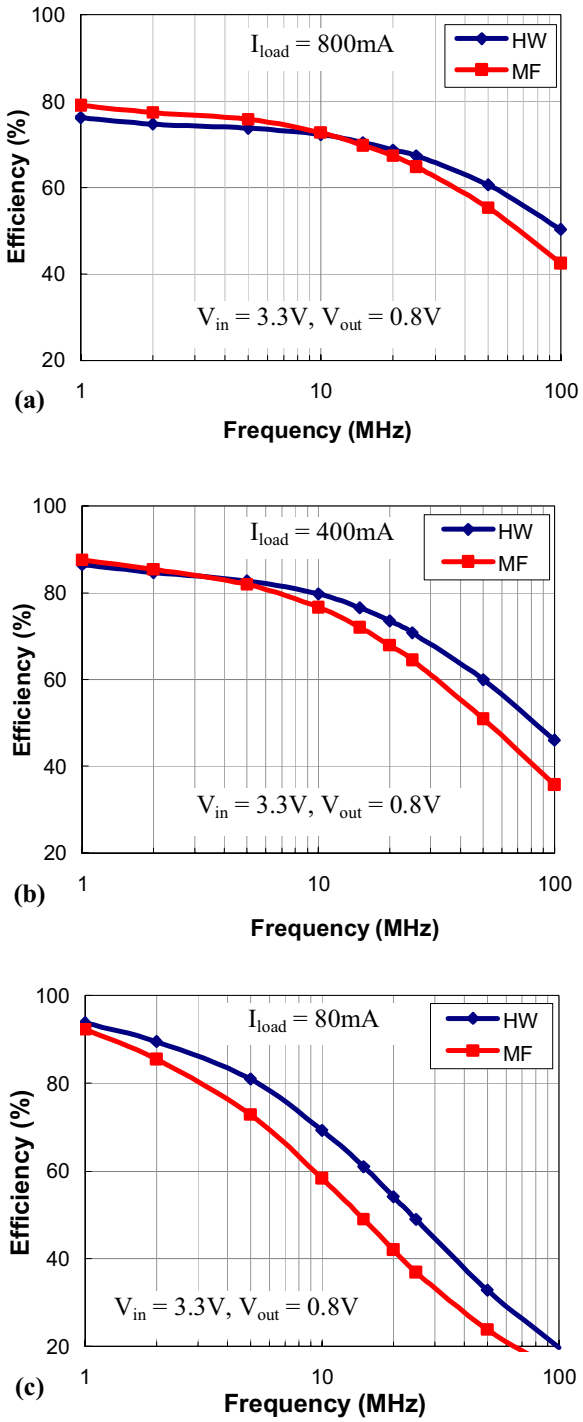

Fig. 7. Comparison of power conversion efficiencies for both MF and HW structures as a function of switching frequency and for different load currents: (a) 800mA, (b) 400mA, and (c) 80mA

Table 1. Data comparison between MF and HW layout structures

	@ Vin=3.3V, Vdd=3.3V, Id=400mA					
	L (µm)	W_{total} (µm)	Area (mm^2)	R_{ON} (mΩ)	Q_G (nC)	FOM (nC·mΩ)
Multi-Fingers (MF)	0.50	20172	0.0295	352	0.099	34.80
	0.50	36388	0.0523	237	0.190	44.96
	0.50	54582	0.0788	206	0.306	63.00
	0.50	71354	0.0985	199	0.393	78.16
	0.50	86520	0.1175	194	0.504	97.71
Hybrid Waffle (HW)	0.50	6000	0.0297	493	0.030	14.78
	0.50	8700	0.0426	330	0.044	14.50
	0.50	11900	0.0578	245	0.061	15.01
	0.50	15600	0.0754	195	0.083	16.12
	0.50	19800	0.0953	165	0.109	17.97
	0.50	24500	0.1175	149	0.141	20.99

IV. Conclusion

This paper reports on a low-voltage CMOS power transistor layout technique, implemented in a 0.25µm, 5 metal layers standard CMOS process that is suitable for multi-MHz integrated switched mode power supplies. In comparison with conventional multi-fingers layout geometries, the proposed HW layout structure for the power MOSFET is found to exhibit about 30% drop in on-resistance with 3.6 times smaller total gate charge. In addition, push-pull output stages using this layout technique are found to have higher simulated efficiency at switching frequencies beyond multi-MHz. The proposed layout technique will improve the performance of next generation low-voltage integrated power converters.

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