Closed-Loop Control of Gate-Charge Recycling in a 20 MHz DC-DC Converter

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***Abstract*—Dynamic power consumption in the gate-drive circuitry limits the light-load efficiency of high frequency integrated dc-dc converters. In this paper a power MOSFET gate charge recycling technique is introduced, where the output capacitor is used to store a portion of the gate charge between switching events. The charge is transferred between the gate of power MOSFET and the output capacitor using transmission gates with precise timing control. The timing of the charge transfer is regulated using a simple digital delay-locked loop. The entire system is designed in 0.13 μm CMOS technology, and simulation results show a total saving of 25% in gate driver power and an overall efficiency improvement of 5% at light load. The converter operates at 20 MHz and converts 2.5 V to 0.8 $\sim$ 1.6 V at up to 300 mA.**

I. Introduction

In sub 1-W power converters operating at heavy load, the dynamic gate-drive power consumption, P_{gate} is typically negligible compared to the load-dependent conduction and switching losses. However at light-load conditions, P_{gate} becomes significant compared to the output power P_{out}, especially for integrated converters operating beyond f_s = 10 MHz. As a result, P_{gate} limits the efficiency of integrated dc-dc converters operating beyond 10 MHz, despite recent advances in the $R_{on} \times Q_{gate}$ product of low voltage power MOSFETs. The dynamic gate-drive power consumption of a power MOSFET is given by

$$P_{gate} = Q_{gate} \cdot V_{dr} \cdot f_s \tag{1}$$

where Q_{gate} is the total gate charge, V_{dr} is the gate swing voltage and f_s is the switching frequency. Existing variable frequency control techniques that mitigate P_{gate}, such as pulse frequency modulation (PFM) and pulse skip mode [1], [2] are frequently employed in integrated controllers. These techniques also lead to poor output voltage regulation and electromagnetic interference (EMI) concerns due to the load dependence of f_s.

In applications such as automotive electronic control units (ECUs), operating a dc-dc converter over an unpredictable range of f_s in PFM is usually forbidden due to strict electromagnetic compatibility (EMC) requirements. Several fixed frequency techniques have been proposed to mitigate the gate-drive losses. In the first approach [3]–[5], portions of a segmented power stage (SPS) can be turned off at light-load condition to optimize the trade-off between the effective gate and R_{on}. SPS has a modest overhead compared to a lumped power stage, since the segmentation is easily achieved by separating the gate of power MOSFET cells in the layout. In an alternative approach known as adaptive gate swing control (AGC), Q_{gate} is reduced at light loads by reducing V_{dr}. AGS has been implemented in combination with the SPS technique [6]–[8]. A third method involves the use of a resonant circuit in the gate driver. Numerous resonant gate drivers have been implemented in the past twenty years, including LC resonance [9] and discrete inductor with constant gate current control [10]–[13]. These techniques inevitably require a dedicated inductor or a transformer for energy storage. Certain resonant gate drivers have demonstrated more than 5 % in overall efficiency improvement over a wide load range [11]–[13], however most of them are implemented with discrete components and with open-loop control on converters running lower than 4 MHz, and none of these techniques have been demonstrated above 10 MHz in which the rise and fall times of the gating signals are within a few nanoseconds.

Capacitor-based charge recycling has been used for power reduction in various digital circuits and energy harvesting systems [14]–[16]. In this paper, charge recycling is used to reduce gate-drive loss of a 20 MHz synchronous dc-dc buck converter with a high-precision, closed-loop timing control scheme. Unlike SPS and AGS, this gate-charge recycling technique reduces P_{gate} without compromising R_{on}. Unlike resonant gate drivers, this technique does not require additional magnetic components, which makes it more attractive for integrated converter applications. The concept is explained in Section II. The closed-loop timing control is discussed in Section III and simulation results are reported in Section IV.

II. Charge Recycling to Reduce Gate-Drive Losses

Unlike the efficiency optimization techniques that actively reduce one or more of the the factors in (1), charge recycling involves storing a portion of Q_{gate} in a capacitor during the gate discharge phase, then re-using it during charging phase. The charge from the driver supply is therefore recycled, leading to a maximum power savings of 50 % when the voltage on the storage node is 1/2 of the drive voltage. In [17]–[19], charge recycling is implemented by stacking the gate drivers so that the charge can directly be transfered from the high-side gate to the low-side gate. The mid-rail node is either regulated to power other circuit blocks, or connected to the switching node through a diode connected transistor. Although this technique provides a significant reduction in P_{gate}, stacked

drivers are not practical in a low voltage process. Alternatively, a linear regulator a regulator can be used to provide a mid-rail voltage as the charge storage node. The implementation of an on-chip, high-bandwidth linear regulator to provide the mid-rail voltage is relatively expensive, since the gate drivers require very high peak currents [20]. In [21], a gate charge modulation and recycling technique (GCMR) is implemented with a on chip LC tank for a 3 MHz converter with 5% efficiency improvement at light load. The charge recycling techniques require, an additional capacitance that is at least one order larger than the effective gate capacitance of the power MOSFET. A large storage capacitance is needed to ensure that the storage tank maintains a constant voltage throughout the charge-sharing phase.

In order to alleviate the need for an additional large on-chip capacitor, we propose to use the output capacitor of the converter C_{out} as the charge storage component, since C_{out}. C_{out} is at least two orders of magnitude higher than the effective gate capacitance the power MOSFETs, and V_{out} is precisely regulated by the controller. A simplified diagram of the charge recycling system and ideal gating waveforms are shown in Fig. 1(a) and (b), respectively. The gates of the power MOSFETs M_p and M_n are connected to C_{out} through transmission gates T_{x1} and T_{x2} during charge recycling. The last stage of the gate drivers has four separated gating signals c_1 to c_4, in order to allow the gate to be driven by the transmission gates while it is being charged or discharged through the output capacitor. Ideal switching waveforms for M_p and T_{x1} are shown in Fig. 1(b). During the charging phase, the $V_{g,p}$ is first charged to V_{out} through T_{x1}, while the driver is left in a high impedance state. Ideally, T_{x1} is turned off precisely when $V_{g,p}$ reaches V_{out}, after which the driver charges $V_{g,p}$ to V_{dr}. A similar procedure applies for the discharging phase. When the charge taken from C_{out} during charging and discharging phases are not equal, there is a net charge accumulated onto or withdrawn from C_{out}. This is generally not problematic since the converter feedback regulates V_{out} to compensate for this effect. Notice that when C_{out} is used as the storage element, using charge from C_{out} to charge up the gate is not necessary, since the charge removed from the gate has gone to the output, which reduces input current when load is fixed. In this case the ideal power savings is $Q_{gate} \cdot (V_{dr} - V_{out}) \cdot f_s$, thus the lower the output voltage is, the less input current is consumed.

Allowing $V_{g,n}$ and $V_{g,p}$ to reach V_{out} results in optimal charge recycling, however it leads to extensive delays in the turn-on and turn-off of the power stage. This delay is caused by the time constant formed by the gate capacitance and the on-resistance of the transmission gates. Any significant delay is undesirable due to the increased switching loss in hard-switching converters. The delay can be minimized by increasing the sizes of T_{x1} and T_{x2}, at the expense of higher dynamic power consumption, which decreases the effectiveness of charge recycling. An alternative method to minimize the turn-on/off delay is to terminate the charge sharing phase slightly before reaching V_{out}. The ideal termination thresholds for Δt_{x1} and Δt_{x2} are denoted V_{out}^+ and V_{out}^-, respectively, where $V_{out}^- < V_{out} < V_{out}^+$.

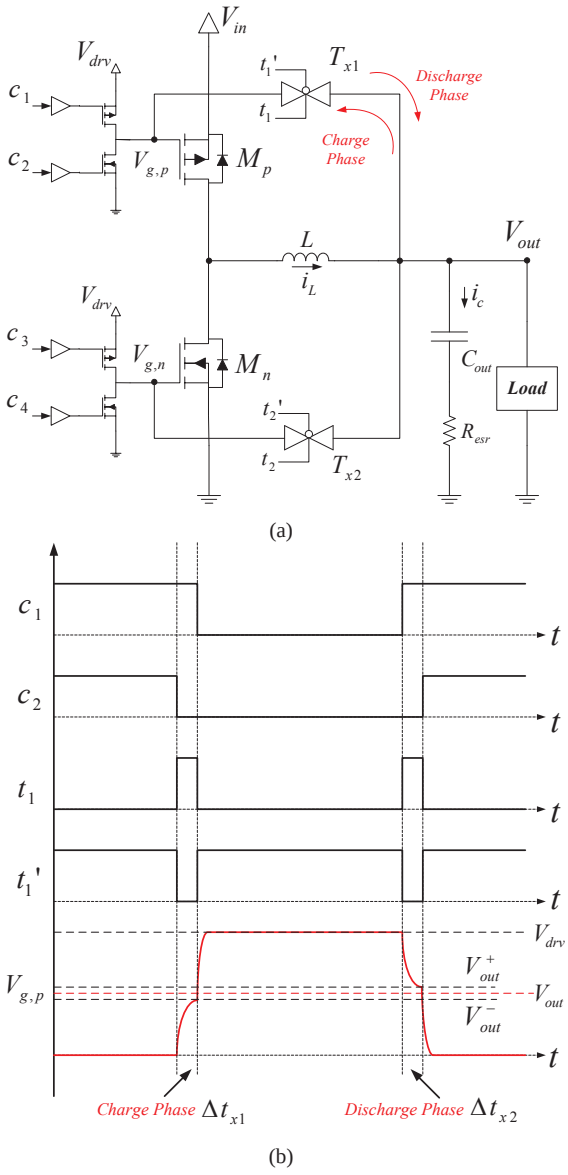


Fig. 1. (a) Simplified system diagram and (b) Ideal switching waveforms for the high-side switch.

III. Control Scheme

Achieving the maximum reduction in P_{gate} requires precise closed-loop control of the timing in the charge recycling circuit of Fig. 1(a) due to process, voltage and temperature (PVT) variations. The major challenge is to control the on-time of the transmission gates T_{x1} and T_{x2}, Δt_{x1} and Δt_{x2}, such that $V_{g,p}$ and $V_{g,n}$ are fully charged and discharged to V_{out} before activating the main drivers. The optimal timing for Δt_{x1} and Δt_{x2} is not known a-priori due PVT variations and uncertainties in the device parasitics. Simulations can therefore only provide a first-order estimate.

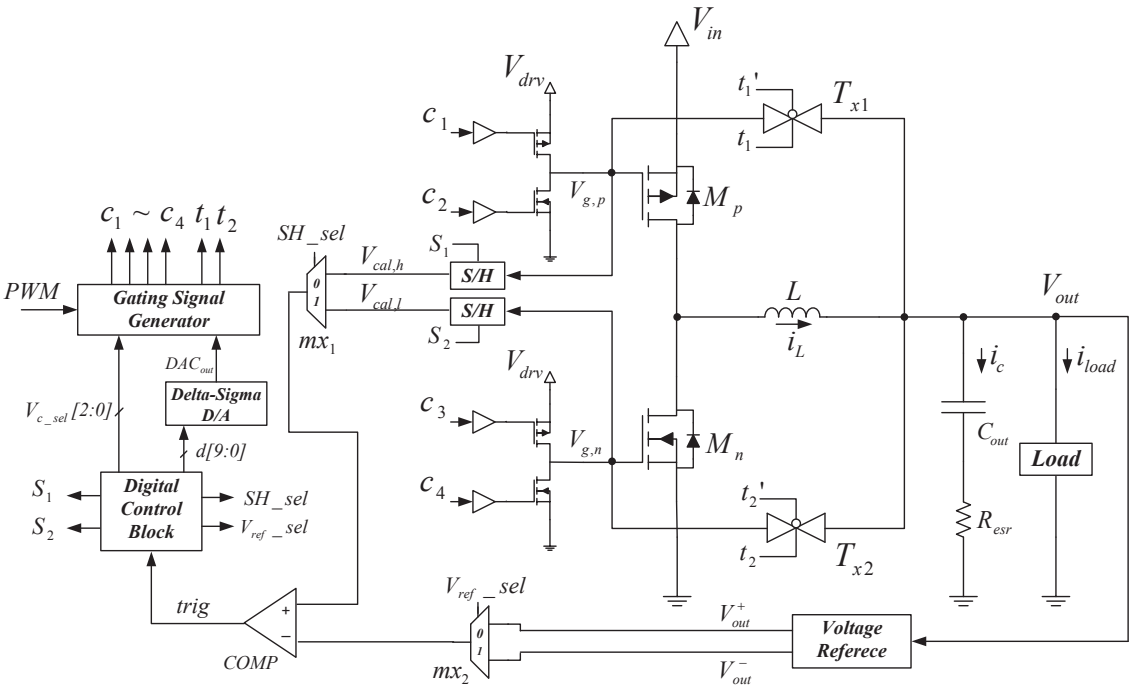


Fig. 2. System architecture of the closed-loop gate-charge recycling timing control.

Using a continuous-time comparator to trigger the end of the charge-sharing phases Δt_{x1} and Δt_{x2} in a single switching-cycle is not feasible due to the finite comparator delay and turn-on time of the transmission gates. The 20 MHz converter targeted in this work has a switching period of 50 ns, therefore the rise/fall times at $V_{g,n}$ and $V_{g,p}$ should be within several ns. This imposes a delay requirement in ps for the comparator, and as f_s increases, designing a low-power comparator with such a small delay is impossible. We therefore propose a closed-loop delay-locking control scheme that is insensitive to the aforementioned delays. As most calibration schemes, the process should only be performed periodically to conserve power.

A. Implementation

The proposed closed-loop control architecture shown in Fig. 2 employs a central digital calibration module to maximize the resource sharing. The timing for the four charge-sharing intervals are sequentially calibrated. Two sample-and-hold circuits are used to sample $V_{g,n}$ and $V_{g,p}$ when T_{x1} and T_{x2} are turned off at the end of the respective charge-sharing phases. The sampled voltages $V_{cal,h}$ and $V_{cal,l}$ are compared to the thresholds V_{out}^+ or V_{out}^-, which are generated by the reference generator shown in Fig. 3. The reference generator gives V_{out}^+ = 1.1×V_{out} and V_{out}^- = 0.9×V_{out}. The reference generator only tracks the DC value of V_{out} and therefore only requires a low-bandwidth, power-efficient OTA. Two analog multiplexers mx_1 and mx_2 are used to select the appropriate sampled voltage and reference. The delay in each of the four charge-sharing phases is adjusted such that sampled voltage reaches the target reference. The gating signals c_1 to c_4, t_1 and t_2 are generated through a non-overlapping clock generator with voltage controlled delays (VCD) as shown in Fig. 4. The VCD is designed with a current starved inverter, and different delay ranges can be selected digitally using the V/I gain as shown in Fig. 5. The VCD has a tuning range of 0.6 V $< V_{cntrl} <$ 1.1 V, which is generated from a 2nd order Δ-Σ DAC, as shown in Fig. 6, similar to the one used in [22]. The dead-time generator is also implemented with this VCD structure and a larger delay range. A total of six VCDs are therefore controlled by the same Δ-Σ DAC through a 6-to-1 analog multiplexer with a shared resistor R_{ctrl} as the resistance of the first order filter for the Δ-Σ DAC(see Fig. 7). A digital controller sequences the select inputs for the multiplexers, and sets the 10-bit digital inputs $d[9:0]$ to the Δ-Σ DAC.

B. Operation

The control voltage for each VCD is held on a capacitor C_{ctrl}(which also serves as the capacitance of the first order filter for the $\Delta - \Sigma$ DAC) to maintain proper delays, and over time the leakage will affect the accuracy of the control voltage. In addition, converter will experience different operating condition such as temperature and change in output voltage. Therefore it is essential to periodically re-calibrate the timing circuit to maintain the optimal power saving, and as long as this calibration period is small comparing to the period of stable state, the power used to do the calibration can be justified. The operation of the closed-loop control is described as the following, and the algorithmic state machine

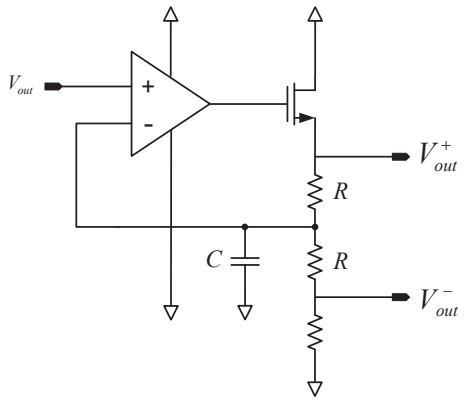


Fig. 3. Voltage reference generator for V_{out}^{+} and V_{out}^{+}.

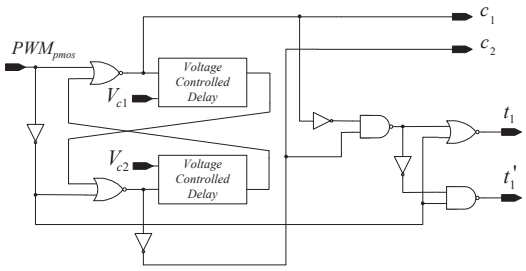


Fig. 4. Gate-drive timing generator.

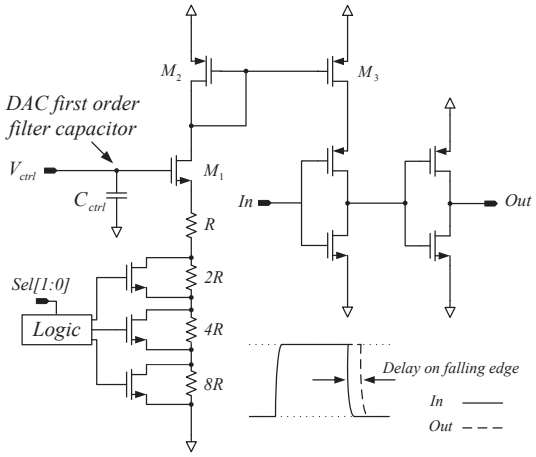


Fig. 5. Voltage controlled delay generator.

(ASM) chart is shown in Fig. 8:

1) Before converter start-up, the DAC initially sets a dead-time for converter to start up. After the output voltage has reached the desired value, calibration starts by enabling voltage reference, comparator and DAC clock. The controller also sets a large dead-time to begin with to allow all possible on-times of the transmission gates. A counter is served as a timer to indicate this process is finished.

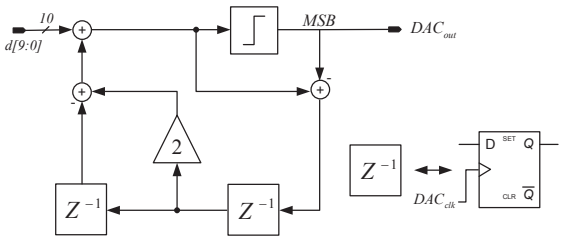


Fig. 6. 10-bit, 2nd order Σ-Δ DAC used to set the control voltages for the timing generators.

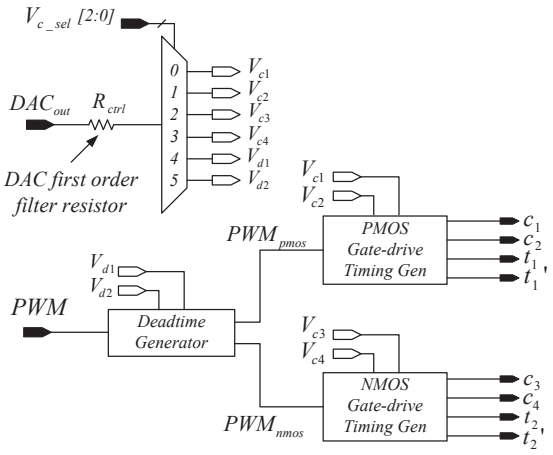


Fig. 7. Gating signal generator for MOSFET and transmission gate drivers.

2) Then controller starts to find the optimal Δt_{x1} and Δt_{x2} for each transmission gate. The DAC inputs are initially set to have the maximum control voltage to achieve minimum delay and then slowly reduced until sampled gate voltage has passed the corresponding reference. A 10 bit DAC is used such that very fine resolution of 20 ps delay step can be achieved. The time to find the optimal timing depends on the delay step and also the clock speed and the time constant of the DAC filter. This process is repeated for rising and falling edges of both $V_{g,p}$ and $V_{g,n}$. The controller coordinates all the select, timing and DAC input signals.
3) After the optimal Δt_{x1} and Δt_{x2} found, the controller takes consideration of these times and reduce the dead-time with some margin. A timer is used to ensure the dead-time has reached the desired value. The a calibration loop is completed.
4) The controller then disables the voltage reference, comparator and DAC to save power. A calibration timer is started to indicate the instance when next calibration is required. The time should be set to the maximum time which the control circuit can maintain its accurate timing. In this design, this depends on the value of the capacitor that holds the control voltage for each delay generator and its leakage. Other factors could be changes in operating temperature and output voltage.

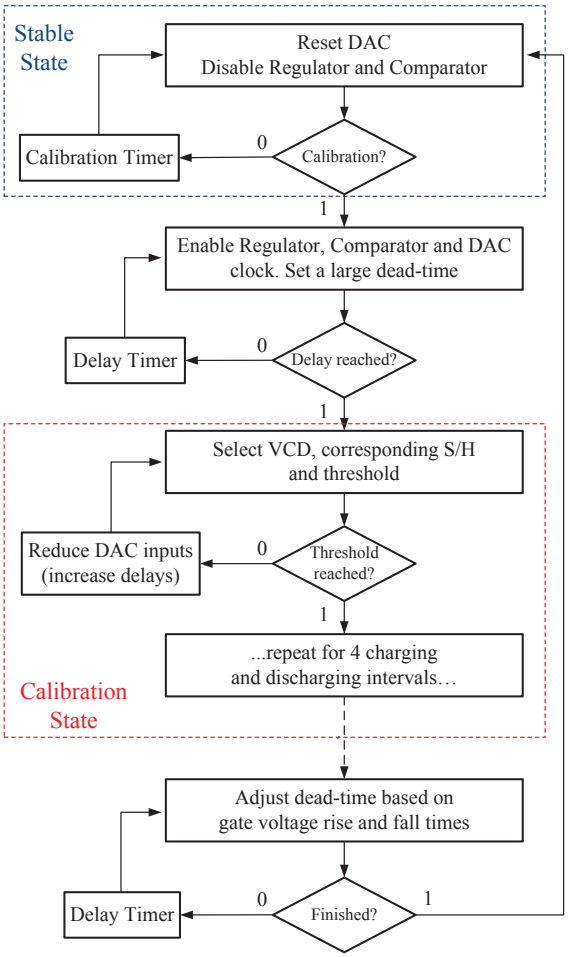


Fig. 8. ASM chart for the close-loop control scheme.

IV. Simulation Results

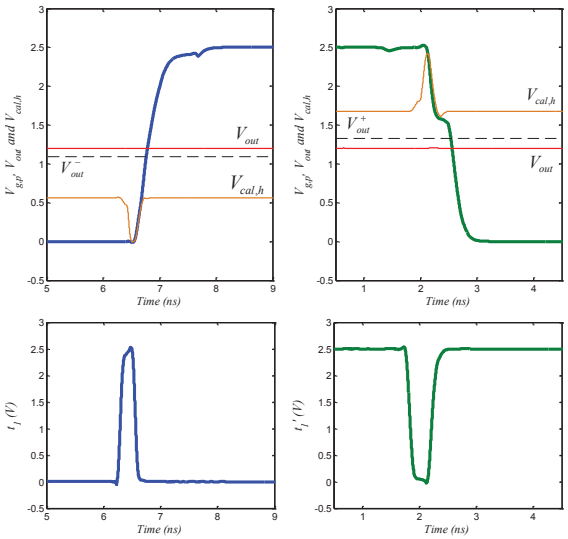
Simulation of the complete system was performed in Cadence Analog-Mixed-Signal simulation with IBM 0.13 μm technology kit. The converter specifications are listed in Table I. The on-resistance and gate-charge values are extracted from layout, and parasitic elements due to layout and bond wire resistance are also estimated and applied in the simulation. Simulated switching waveforms are shown in Fig. 9, where both before and after calibration waveforms are shown. T_{x1} and T_{x2} are sized such that the turn-on of the power MOSFETs is only slowed down by less than 1 ns. The converter is simulated with in voltage mode control at fixed input voltage of 2.5 V, and the converter efficiency is plotted for output voltages at 0.8, 1.2 and 1.6V from 15 mA to 180 mA(see Fig. 10). The charge recycling technique exhibits from 3 to 5% efficiency improvements up to 100 mA. In Fig. 11, the power savings at every output voltage is broken into driver and input power savings. When V_{out} is at 1.2 V near half of V_g, the amount of charge transfered to the output capacitor is nearly the same as the charge taken from it to charge up the gates of M_p and M_n. Therefore there is almost no change in input power, and majority of the saving comes from driver power,

TABLE I
Simulated Converter Specifications

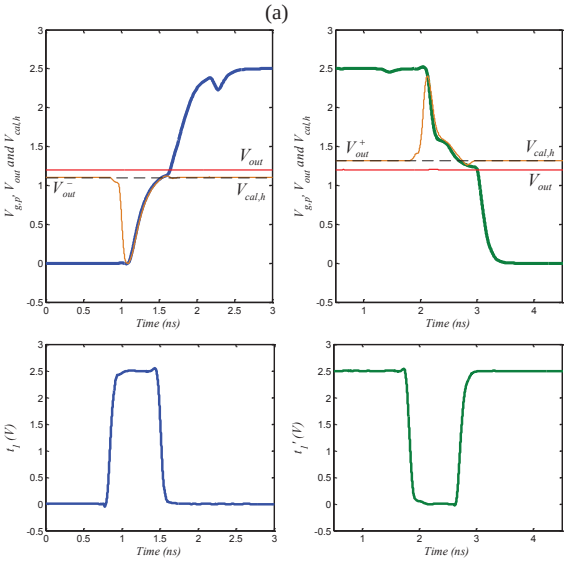
Specification	Value	Units
Input Voltage, V_g	2.5	V
Driver Voltage, V_{drv}	2.5	V
Output Voltage, V_{out}	0.8 to 1.6	V
Rated Load, I_{load}	300	mA
R_{on} for $M_{1,2}$	185, 90	mΩ
Q_{gate} for $M_{1,2}$ @ 2.5V	230, 120	pC
R_{on} for T_{x1} pmos, nmos	1.4, 2.5	Ω
R_{on} for T_{x2} pmos, nmos	2.8, 3.5	Ω
Output Capacitor C_{out}	1	μF
Total Capacitor ESR R_c	10	mΩ
Filter, L	1.5	μH
Inductor DCR, R_L	100	mΩ
Switching Frequency, f_s	20	MHz
DAC Clock Frequency, DAC_{clk}, adjustable	67 to 140	MHz
VCD Range	0.2 to 1.5	ns
Dead-time Range	0.5 to 2	ns
Total calibration time	< 20	μs
Re-calibration period	5	ms

which consists the power to drive T_{x1} and T_{x2} subtracted from the driver power saved from charge recycling. When output voltage reduced to 0.8 V, the gate charge delivered to the output is larger comparing to that in charging phase(net charge is accumulated onto the output capacitor). Therefore driver power saving is reduced to around 6% whereas there is more reduction in input power, and as load increases, the input power saving reduces from 8% to 2%. At $V_{out} = 1.6$ V, the opposite occurs. More charge is taken from the output to charge up the gates, which greatly reduces driver power by almost 40%. However, more input power is drawn to compensate the net charge loss at the output, which translates into a negative input power saving as shown in Fig. 11(b). This is the uniqueness of gate-charge recycling, which is, the driver supply produces power to the converter output during discharging phase and taken power from the output during charging phase. The net effect depends on the output voltage in relevance to the drive supply voltage.

As discussed, since the gate charge is going to the output during discharging phase, it is not necessary to re-use it during charging phase because the overhead in power to drive T_{x1} and T_{x2}. Therefore it is expected to have further efficiency improvement when only discharge phase is activated. This case is simulated at V_{out} equals to 1.2 V and compared to with and without charge recycling conditions in Fig. 12. Simulation shows when only using discharge phase overall efficiency is on average 2% lower than employing charge recycling for both phases. This can be explained as the follows. When the charging phase is disabled, there is no saving in the driver power but the input power is reduced because part of the driver power is delivered to the load during discharge phase. However this reduction in input current puts the converter operate at a lower efficiency, because at light load the efficiency drops rapidly as the load decreases. In Fig. 13, the driver and input savings are compared between charge recycling and discharge phase only mode. As shown at V_{out} = 1.2 V, charge recycling has major savings in driver power whereas discharge phase



(a)



(b)

Fig. 9. Switching waveforms (a) Before calibration (Δt_{x1} and Δt_{x2} are set to minimum) and (b) Optimal timing achieved after thresholds are reached.

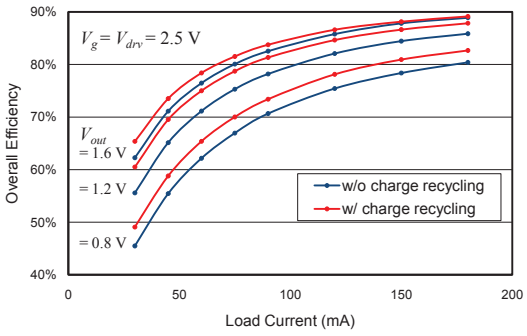
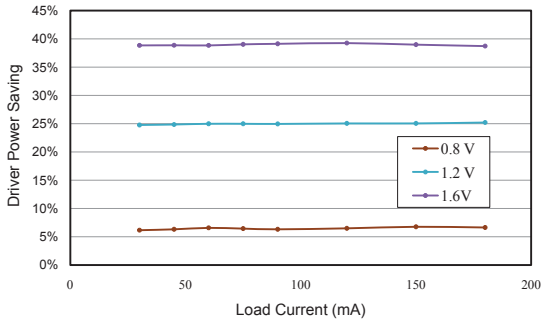


Fig. 10. Efficiency improvements at V_{out} = 0.8, 1.2 and 1.6 V

only mode has greater savings in input power, which is again is a strong function of the load current.



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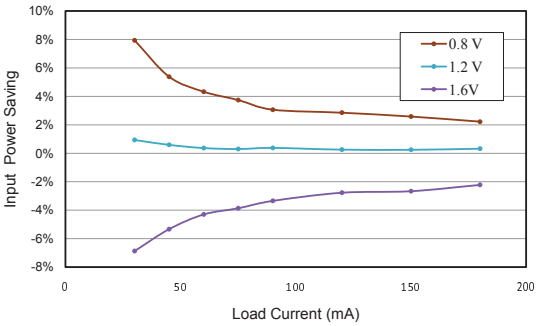

(b)

Fig. 11. (a) Driver power saving and (b) Input power saving, comparison at different V_{out}.

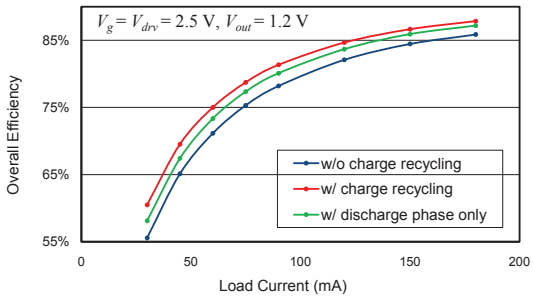

Fig. 12. Efficiency improvements at V_{out} = 1.2 V with discharging phase operating only

V. Conclusion

The proposed closed-loop charge recycling gate driver was shown to have an overall efficiency improvement up to 5% at light load conditions and a 25% equilvalent saving in gate driver loss across all loads. The savings in driver and input power were simulated and discussed for a range of output voltages. The effect of operating only in discharge mode is also illustrated. Future work involves experimental verification of the efficiency improvements.

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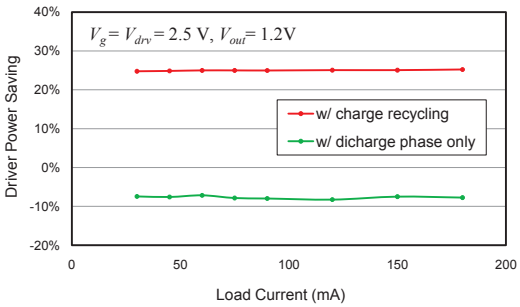
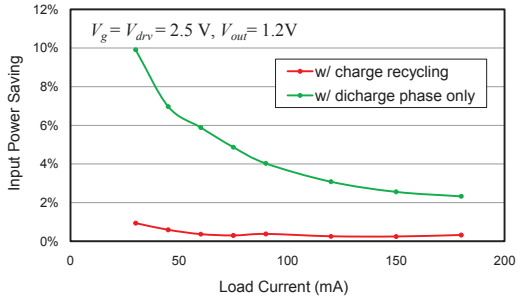


(a)



(b)

Fig. 13. (a) Driver power saving and (b) Input power saving, comparison between charge recycling and discharge phase only at V_{out} = 1.2 V.

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