Abstract—Using a variable frequency, or spread spectrum clock in switched-mode power supplies is a popular method for reducing EMI in noise-sensitive applications. A system that operates with a fixed frequency-spread must inevitably be over-designed to compensate for the uncertainties in the parasitic components, as well as aging and temperature effects. In this work, a self-calibrated, adaptive spread spectrum system is simulated using an integrated boost converter in a high voltage 0.35 µm CMOS technology. The converter operates with a programmable spread of \( f_s = 100-350 \text{ kHz} \). The EMI spectrum is calculated from the sampled input current using a short-time FFT and compared with programmable limits based on EMC regulations. The spread is actively minimized under different conditions, while meeting EMI targets.

I. INTRODUCTION

Increasing the switching frequency in switched-mode power supplies (SMPS) has allowed a drastic increase in the power density, however meeting tough electromagnetic compatibility (EMC) standards is a serious challenge in modern automotive, industrial and consumer applications. In addition to careful PCB layout, there are several popular techniques to mitigate EMI in these converters. Dedicated filtering through the use of snubbers is normally considered as a last resort to achieve compliance, since it leads to considerable costs and additional volume. A number of active techniques have been introduced as an alternative to these filter-based solutions. All active solutions with the exception of the soft switching schemes employ a variable switching frequency to spread the conducted and radiated emissions over a broader range of frequency, hence limiting the EMI [1,2]. When operating in spread spectrum, both the amount of spread \( \Delta f \) and the time-domain variation in \( f_s \) must be carefully selected. In [1], it is shown that increasing this range beyond the optimal value can lead to an increase in peak amplitudes at certain frequencies due to overlapping harmonic bands, leading to EMC failure. The parasitic components that influence the EMI spectrum change with temperature and aging. In addition, it is clear that the load current, which can vary frequently plays an important role on the EMI spectrum. This inevitably results in a wide variation in the EMI spectrum for a single SMPS. Choosing a frequency spread that is larger than necessary leads to stability issues and over-design. Ideally, \( \Delta f \) should be actively minimized by the controller to achieve EMC with a sufficient margin. This ensures that the converter operates with the best performance over a wide range of operating conditions and eliminates the need for over-design and expensive snubbers.

Recently fast techniques have been developed for monitoring the electromagnetic spectrum of the device under test (DUT) [3,13]. Based on these studies in this paper a closed-loop technique is proposed to achieve this goal, namely to actively control \( \Delta f \) for achieving optimal EMI mitigation. Using this technique, the conducted EMI spectrum is calculated in real-time using a digital approach and then compared to the standard. A simple algorithm can be used to either decrease or increase \( \Delta f \) if the spectrum violates the programmable limits, which are based on EMC standards. The technique is only applicable to conducted emissions, since it is not practical to measure radiate emissions on the fly.

This is organized as follows. Section II describes the proposed closed-loop spread spectrum architecture. Section III presents the simulation results based on the co-simulation run by MATLAB and Cadence. Section IV highlights the feasibility of the proposed technique for implementation in SMPS applications above 10 W. The resource usage in the Field Programmable Gate Arrays (FPGA) are reported to provide an indication of the implementation cost.

II. CLOSED-LOOP SPREAD SPECTRUM ARCHITECTURE

Fig. 1 shows the system architecture for an automotive boost converter. The input current is sampled and analyzed to measure the EMI injected from the dc-dc converter to the input supply. A low-noise amplifier (LNA), which must be band-limited to act as an anti-aliasing filter, is followed by an Analog to Digital Converter (ADC) having sufficient resolution to measure the EMI spectrum in the TDEMI block. It can be shown that the number of bits of the ADC for a certain dynamic range and maximum error in the calculations is given by [3]:

\[
b_t = -\log_2(10^{X_{er,\text{dB}}} + \frac{X_{SFDR}}{6\text{dB}})
\]

where \( X_{er,\text{dB}} \) is the maximum acceptable error in dB and \( X_{SFDR} \) is the dynamic range of the output. For example a 9-bit ADC can cover a 42 dB range with maximum 1.1 dB error. This is already compliant with the CISPR standard, which requires an effective 36 dB dynamic range for an EMI analyzer.
The digital EMI measurement block has been designed based on the method introduced in [3]. This method estimates the frequency spectrum of the measured current in the digital domain by calculating the Short Time Fast Fourier Transform (STFFT) of the input current. Fig. II shows how this STFFT can be implemented in hardware. The FFT is calculated as follows:

\[ X[t,n] = \sum_{k=0}^{N-1} x[k+t]w[k]e^{-j2\pi kn/N} \]  

where \( w[k] \) is a Gaussian window function that is used to represent the IF-filter of a real EMI-Receiver. The signal in frequency domain is passed through a quasi-peak detector module that is implemented to model the detector modules in real EMI receivers.

The ADC operates at 80 Msamples/s, thus the calculated EMI spectrum is valid up to 40 MHz due to Nyquist criterion, which is more than sufficient for the 30 MHz bandwidth defined in CISPR-25 standard [4]. An overlapping ratio of 75 % is chosen for this case which requires the use of four FFT cores in parallel for real-time operation. However, in order to reduce the computational resources the necessary data can be stored first and then processed by the FPGA or microcontroller. This eliminates the need for multiple FFT cores in the system. In this case, The 9-bit ADC output is fed to the 32-bit shift registers, which can hold up to 2^{20} = 1,048,576 samples. This implies that a minimum memory of about 2 Mbytes would be necessary in the system to save the samples and perform the calculations.

In this paper the STFFT function is first implemented in Matlab to allow a flexible parameter variation during the concept phase. Then the STFFT block, along with other signal processing features, is implemented in a FPGA platform to demonstrate the feasibility of the system. Ideally, the proposed technique can be implemented in applications where an existing micro-controller and memory are already available to periodically run the computation. This scenario, which is common in automotive electronic control units (ECUs) for example, limits the incremental cost of the EMI mitigation. Also a massively parallel implementation can be used for System-On-Chip SMPS applications in deep sub-micron technologies.

Traditional EMI receivers probe the signal at the output of a Line Impedance Stabilizing Network (LISN) circuit, which is placed between the input supply and the SMPS [4]. The LISN decouples the input power supply’s injected noise from that of the SMPS and also provides a stable impedance for...
measuring EMI spectrum. The transfer function of a LISN is provided in the CISPR standard [4]. In the proposed method, the LISN transfer function is digitally implemented on the calculated frequency spectrum. The digital implementation provides a great deal of flexibility in this respect. The matching between the sensed spectrum from the EMI receiver and the on-board circuitry can potentially be improved through digital calibration, which is beyond the scope of this paper.

A 9-element linear feedback shift-register (LFSR) is used to generate a pseudo-random 512-cycle pattern which is sent to the \( \Delta \Sigma \) DAC [11,2] every 100 switching periods. The DAC is used to generate a voltage for the voltage-to-frequency converter (V2F). The LFSR is operated at the 80 MHz system clock, while the limiter block is used to implement the adaptive spread \( \Delta f \). The limiter simply accepts or rejects the LFSR output based on the digital modulation index \( M_r = \Delta f / f_s \).

The probability that the system will not accept a new switching frequency within the desirable range after 100 cycles is given by

\[
P = \left( \frac{1 - M_r}{M_{VCO}} \right)^{100}
\]

where \( M_r \) is the modulation index and \( M_{VCO} \) is equal to \( \Delta f_{VCO} \). Further calculations can be done to show that this situation rarely happens in a 9-element LFSR and thus the uniform distribution of the desirable switching frequencies remains intact. This means that uniformly-distributed random numbers within a programmable range are generated in the system. The system settles with the proper modulation index after performing at most 9 EMI calculations by doing a binary search for a 9-bit spread spectrum resolution.

A simple 2\(^{nd}\) order \( \Delta \Sigma \) DAC shown in Fig. 5 together with a 1\(^{st}\) order RC low-pass filter are used to transform the output value for the frequency into a corresponding voltage. The simple modulator can be implemented using only two registers and two adders. The one bit \( \Delta \Sigma \) DAC offers high-resolution, low-power (no quiescent current) and potential for compact System on Chip (SoC) solutions.

### III. Simulation Results

The proposed method has been simulated using Cadence for a boost converter having the specifications shown in Table I, which are typical for SMPS used in (ECUs). The complete power stage is based on a test-chip in a 0.35 \( \mu \)m CMOS high voltage technology from Austria Microsystems. The remaining parts of the controller have been simulated using behavioural modeling to demonstrate the system’s feasibility with a reasonable simulation run-time.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>24</td>
<td>V</td>
</tr>
<tr>
<td>Rated Output Load</td>
<td>0.35</td>
<td>A</td>
</tr>
<tr>
<td>L/C</td>
<td>30/40</td>
<td>( \mu H/\mu F )</td>
</tr>
<tr>
<td>( R_L/R_{on}/R_C )</td>
<td>0.15/0/250/0.07</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Switching Frequency Range</td>
<td>100-350</td>
<td>kHz</td>
</tr>
<tr>
<td>DAC’s Output Voltage Range</td>
<td>0.5-2</td>
<td>V</td>
</tr>
</tbody>
</table>
Fig. 6 shows the Voltage controlled Oscillator’s topology and output frequency versus the DAC’s output voltage. Fig. 7 shows the DAC’s output for two different modulation indices. As shown the proposed digital algorithm results in a proper range-limited switching frequency $clk_s$ which is then fed to the converter’s output regulation block.

![Voltage Controlled Oscillator circuit and (b) switching frequency versus DAC output voltage.](image)

Fig. 6. (a) Voltage Controlled Oscillator circuit and (b) switching frequency versus DAC output voltage.

The EMI spectra of the converter are shown in Fig. 8 for different values of the modulation index. The converter is operated in open-loop to isolate the effect of the closed-loop control. In practical implementations, the modulation in $f_s$ is sufficiently slow such that the converter effectively operates in pseudo steady-state at each value of $f_s$.

With $M_r = 0 \%$ there are multiple EMI regulation violations, as shown in Fig. 8a. As expected, increasing the modulation index disperses the noise spectrum in a wider range, resulting in a EMC-compliant system. Further increase of the modulation index might result in violations in other parts of the spectrum, especially at higher frequencies due to the excessive widening of the spectrum. Fig. 8b represents the final settling point for the closed loop EMI system as 26 % is the minimum modulation index at which the EMI spectrum complies with the standard.

![EMI Spectrum](image)

Fig. 8. (a) EMI Spectrum for $M_r = 0 \%$ (b) $M_r = 26 \%$ and (c) $M_r = 75 \%$.

Fig. 7. (a) DAC output for $M_s = 18 \%$ and (b) $M_r = 72 \%$.

IV. COST AND FEASIBILITY ANALYSIS

The main advantage of the RTEMI system is its reduced computation time compared to conventional techniques which allows it to be used in applications where real-time EMC control is useful. It should be noted that the the EMI measurement and modulation calibration procedure only needs to run periodically to conserve power. An estimated runtime is calculated for the algorithm on both standard FPGA and microcontroller platforms. The logic gate resource usage and power consumption are reported for the Xilinx FPGA platforms.
The number of samples per transform \( M \) is directly related to the sampling rate of the signal \( f_s \) and frequency bin width \( f_{BW} \) which is determined by the frequency response of the Guassian window that models the IF filter:

\[
M = \frac{f_s}{f_{BW}} \tag{4}
\]

As the sampling frequency of the system is 80 MHz, for a bin-width of 2 kHz, each FFT transformation would contain 40000 real data points. As the overlapping factor in this work is considered to be 75 %, each point in the measuring time is considered in four transformations. If a dwell time of 2 seconds is used to measure the spectrum, as defined by the CISPR standard, 16000 FFT transforms are needed to cover the whole range. Today’s FFT IP cores can support up to 65536 (16 bit) FFT transformations [12]. According to [12], a processing of 40000-points FFT in a Spartan III Xilinx FPGA with clock frequency of 80 MHz takes about 1.7 ms. This gives out a processing time of less than 30 seconds for 16000 FFTs. This number is increased in practice due to the RAM access times for reading and writing the stored data. Taking the measurement time into account, fulfilling a complete spectrum estimation and EMC compliance checking can be done in below 135 seconds, which means that the system should stabilize in less than three minutes with an optimal spread spectrum range.

Using a simple non-optimized radix-2 algorithm to compute the FFT with size \( M \) requires \( \frac{M}{2} \log_2 M \) multiplications and \( M \log_2 M \) additions [10]. For \( M = 40000 \), this corresponds to 212000 multiplications and 424000 additions. Assuming a simple low power microcontroller with performance capability of 3 million instructions per Seconds (MIPS), this takes about 21.2 ms to perform. For a dwell time of two seconds, the calculation time will be no more than 340 seconds. This ensures a calibration time of a few minutes for the system to come to the final result. It should be noted that due to the very long simulation time of a FPGA code on a personal computer, the simulation was restricted to a fraction of the whole data that is the dwell time was considered to be significantly lower than the traditional two seconds period.

Xilinx ISE estimation tools together with [12] were used to report the area usage and power consumption of the introduced method on two FPGA platforms. The FFT size \( M \) is determined to satisfy the following equation:

\[
2^{N-1} < M < 2^N \tag{5}
\]

where \( M \) denotes the total number of points in a single FFT which in this case is 40000. Therefore \( N \) is determined to be 16. The result of the analysis is listed in Table II. The power consumption and dynamic current are relatively high, which is not surprising considering the large number of computations performed by the RTEMI block. However, as the closed loop EMI spectrum adjustment only needs to be performed periodically with a relatively low duty-cycle, the total energy consumption will be scaled down accordingly.

To demonstrate the feasibility of implementation, the introduced method in this paper has been coded and simulated on a FPGA platform. Fig. 9 shows the resulting output frequency components for \( M_r = 100 \% \) and \( M_r = 50 \% \). However, it should be noted that due to the very long simulation time of a FPGA code on a personal computer, the simulation was restricted to a fraction of the whole data that is the dwell time was considered to be significantly lower than the traditional two seconds period.

![EMI Spectrum](image)

**Fig. 9.** (a) EMI Spectrum for \( M_r = 50 \% \) (b) \( M_r = 100 \% \) based on FPGA simulation.

**V. Conclusions**

The closed-loop spread-spectrum calibration method is effective for real-time EMI mitigation in SMPS. The spread-spectrum frequency range is actively minimized while meeting
targeted EMC specifications, resulting in fewer system EMI problems due to aging and different operating conditions. This approach simplifies controller design for high stability and minimizes over-design and unnecessary stress in the passive components. The implementation cost, in terms of FPGA and CPU resources, is deemed reasonable in SMPS applications above several watts, especially if spare memory and digital resources are already available in the application. The cost of digital resources is constantly dropping, making this approach promising for future deployment. Simulation results based on Cadence and MATLAB were provided to prove the effectiveness of the system. Furthermore, the feasibility of the implementation of the heavy signal processing components was demonstrated by Verilog and HDL coding through simulation on a real FPGA platform. Two major concerns need to be addressed with future work. Firstly, the relative matching between the RTEMI and the traditional EMI receiver and LISN spectra should be investigated. Secondly, the RTEMI operation in the presence of dynamic loads with the converter operating in closed-loop over several minutes cannot be readily simulated and must be tested experimentally.

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REFERENCES