Thermal Management for Multi-Phase Current Mode Buck Converters

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Abstract — This paper deals with thermal management and power sharing in multi-phase buck converters. In conventional designs, each phase is regulated to share the load current equally. However, due to variations in PCB layout, parasitic resistances, airflow, and transistor on-resistance ($R_{on}$), it is common to observe significant temperature variations between the converter phases, leading to reliability issues and suboptimal device utilization. Several past research efforts have demonstrated closed-loop analog and digital techniques to achieve a uniform temperature in all phases. In this work, a thermal management unit (TMU) with four independent linear controllers is proposed to regulate the phase temperatures in a four-phase mixed-signal peak-current mode converter. The digital TMU is designed based on a lumped thermal model of the system and dynamically adjusts the peak current in each phase to match the moving average temperature. Experimental results from a digitally controlled 12 V to 1 V, 50 A, 250 kHz four-phase peak current mode buck converter demonstrate the effectiveness of the proposed thermal management technique in the presence of uneven air flow and dynamic load currents.

I. INTRODUCTION

Multi-phase interleaved voltage regulator modules (VRMs) provide fast dynamic response, small voltage and current ripple, and high power density [1-2]. They have been widely adopted for low output voltage, high output current, and fast load-transient applications [2]. Precise current sharing has been emphasized to reduce voltage and current ripple, while presumably minimizing thermal stress [2-3]. Average current mode control (ACMC) is commonly used to precisely match the current between each phase [4-5]. However, due to variations in PCB layout, parasitic resistances, air-flow, and transistor on-resistance ($R_{on}$), it is common to observe significant temperature variations between the converter phases, which lead to reliability issues and suboptimal device utilization [1, 6-7]. Temperature differences between phases lead to an increase in the peak temperature on the PCB, reduced mean-time-before-failure (MTBF) and reliability [8].

To the author’s best knowledge, active thermal compensation in a multi-phase converter was first suggested in [9], with simulation results provided in [10], where the highest phase temperature is placed on a common analog bus. The local temperature within each phase is compared to this reference and the error is added to the voltage error of each phase’s error amplifier. An alternate analog implementation was introduced by [11] with subsequent experimental validation [8], where a thermistor was introduced into the feedback network of off-the-shelf converters. More recently, a fully-digital thermal management scheme was demonstrated for ACMC, where the losses in each phase are calculated on-line using a sensorless estimation approach [12,13]. The controller in [12,13] was shown to achieve temperature regulation and superior transient response compared to conventional current-mode designs, while eliminating the need for of-chip temperature sensors and high-bandwidth current sensors.

Fig. 1. Block diagram of the four-phase interleaving CPM buck converter with thermal management unit.

One of the major objectives of this work was to develop a set of linear thermal loops, decoupled from the voltage regulation loop, while investigating the time-domain response of the TMU under realistic load conditions and non-uniform airflow. The fan position and airflow in typical applications are optimized for the dominant source of heat, namely the CPU. The VRM cooling is a secondary consideration and hence the phases are not necessarily symmetric with respect to the cooling. In this work, a thermal management unit (TMU) with four independent linear controllers is demonstrated to regulate the phase temperatures in a four-phase mixed-signal peak-current programmed mode (CPM) converter. The system block diagram is shown in Fig. 1. The gate-driver supplies are...
separated in order to emulate $R_{on}$ variations in the experimental setup. CPM was used instead of ACMC to allow for faster transient response and inherent cycle-by-cycle current limiting. Slope compensation in the current-loop is not required in this application, since the duty-cycle is well below 50% for 12 V to 1 V applications.

This paper is organized as follows. The lumped thermal model used for designing the TMU is outlined in Section II. Implementation details of the TMU and system-level simulation results are provided in Section III. Finally results for the experimental prototype are reported in Section IV.

II. LUMPED THERMAL MODEL

A relatively simple lumped element thermal model for the VRM is shown in Fig. 2. The three dominant power losses in each phase are the high-side transistor loss, the low-side transistor loss and the inductor loss, denoted as $P_{HS}$, $P_{LS}$ and $P_{Ind}$, respectively. The model includes a coupling between the phase temperatures through $R_{th1-3}$. Thermal capacitances are included in the model to account for the thermal time constants in the real system. Extracting the exact model parameters from the experimental system and the component datasheets is certainly challenging and error-prone. Commercial packages are available for fine-grained PCB thermal analysis using finite element methods [14]. These CAD tools can provide both steady-state and transient thermal profiles; they are useful for component placement and PCB design, however they cannot be easily integrated into closed-loop system-level simulators for switched-mode power supplies, as used in this work. The lumped model of Fig. 2 was used as a starting point for designing and simulating the TMU, as described in Section III.

III. SYSTEM IMPLEMENTATION AND SIMULATIONS

The proposed control system shown in Fig. 1 consists of a centralized digital PI compensator to regulate $v_{out}(t)$ and a TMU to regulate the phase temperatures, $T_{1-4}$. A peak current control loop is implemented in each phase. Temperature sensors are located near the power stage in each phase and the sampled temperature data is transmitted to the TMU using a shared serial bus. The architecture of the TMU is shown in Fig. 3. Adaptive voltage positioning (AVP) was not implemented in this project; however, the proposed TMU is fully compatible with AVP. For each temperature sample, the average temperature, $T_{avg}$, is computed. This average temperature is then used as a reference for four independent linear PI compensators. Each thermal PI compensator outputs a temperature offset $\Delta i_{t,i}$. The final current commands for the CPM current loops are generated by adding the $\Delta i_{t,i}$ to the central current command $i_t$ that is generated by the voltage loop compensator. The dynamics in the thermal loops are several orders of magnitude slower than the voltage loop due to the long thermal time constants. This effectively decouples the voltage and temperature regulation loops and simplifies the controller design. During normal operation, the voltage compensator can easily maintain regulation while the thermal PI compensators slowly adjust the current distribution. In fact, the zero frequency $\omega_c$ in the thermal PI must be so low that implementing the compensator with on-chip analog circuits would require prohibitively large passive components. Digital implementation of the PI is much more convenient since $\omega_c$ can be shifted to arbitrarily low frequencies, given a sufficient register size. The thermal PI compensators effectively store the current offsets needed to maintain a uniform temperature distribution. Ideally the sum of the offset currents, $\Delta i_T$ is zero:

$$\sum_{i=1}^{4} \Delta i_{ci} = \Delta i_T = 0$$

This condition guarantees that the current-command from the voltage compensator $i_{ct}$ represents the average of the peak currents at all times. Unfortunately this condition is not inherently guaranteed by the control scheme. In fact, an offset gradually grows in $\Delta i_T$ as the converter runs in closed-loop with multiple load steps. This is clearly problematic since the registers in the PIs can overflow as $i_t$ and $\Delta i_{t,i}$ grow in opposite directions to give a constant $i_t$. This problem is solved by introducing an offset control block that actively monitors $\Delta i_T$. When $\Delta i_T$ exceeds a pre-determined threshold $\Delta i_{th}$, the offset control block subtracts $\Delta i_T/4$ from the thermal PIs and adds $\Delta i_T$ to the voltage compensator’s
internal register. This effectively resets the offset, without disturbing the actual current commands \( I_{c1-4} \). This offset cancellation process happens automatically during normal operation.

![Fig. 4. On-Resistance versus Gate to Source Voltage [15].](image)

A mixed-signal simulation of the complete system of Fig. 1 with the parameters is given in Table I was performed using MATLAB Simulink to investigate the TMU concept. The power electronic components are modeled using the SimPowerSystems toolbox. For each phase the average power losses from the switches and inductor are fed into the thermal model of Fig. 3. The junction temperatures of the individual switches are also fed back into the electrical model to set the \( R_{on} \) according to Fig. 4. The resulting setup provides a flexible platform for investigating the TMU operation. All thermal capacitances can be scaled by a factor \( K_t \) in order to accelerate the thermal settling time and reduce the simulation time. The parameters in the thermal PI compensators are scaled accordingly.

**TABLE I. VRM SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, ( V_{in} )</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, ( V_{out} )</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>Number of phases, ( N )</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Inductance, ( L )</td>
<td>10</td>
<td>( \mu )H</td>
</tr>
<tr>
<td>Total output capacitance, ( C_{out} )</td>
<td>2</td>
<td>mF</td>
</tr>
<tr>
<td>Switching frequency, ( f_s )</td>
<td>250</td>
<td>kHz</td>
</tr>
<tr>
<td>Maximum output current, ( I_{out} )</td>
<td>50</td>
<td>A</td>
</tr>
<tr>
<td>Nominal On-resistance for ( M_{hs}, M_{ls} )</td>
<td>8</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Fan air-flow</td>
<td>0.23</td>
<td>m(^3)/min</td>
</tr>
</tbody>
</table>

To speed up the MATLAB simulation, the thermal capacitance is scaled down by about 130k times. The simulation was performed for a 30 A to 50 A current load step at \( t = 7 \) ms. The transient responses are as shown in Fig. 5 and Fig. 6 with the TMU disabled and enabled, respectively. Due to the large acceleration factor, there are slight oscillations in the response as the voltage and thermal loops interact. Two methods of introducing thermal mismatch were considered in this work. The gate-driver supply in each phase, \( V_{drv1-4} \) is independently regulated to intentionally introduce \( R_{on} \) variations according to the power MOSFET characteristics shown in Fig. 4. The devices used in this work were chosen to have relatively high \( R_{on} \) (8 m\( \Omega \) nominal) in order to investigate the thermal behavior. Secondly, a 12 V fan is used to control the airflow across the VRM.

![Fig. 5. Simulated phase temperature with TMU disabled.](image)

![Fig. 6. Simulated phase temperature with TMU enabled.](image)

### IV. EXPERIMENTAL RESULTS

A digitally controlled four-phase VRM with the specifications given in Table I was built to verify the performance of the proposed active TMU under non-uniform air-flow conditions. The PCB layout for the converter was designed to achieve symmetry between the four phases. The digital compensator and TMU are implemented on an FPGA platform. A first test was conducted with the fan off. The power-stage temperature for one of the phases is shown in
Fig. 7 as a function of the total output current. The temperature was measured with two different gate drive voltages ($V_{drv}$) to show the effect of the increased $R_{on}$. As expected, the higher gate drive voltage generates less heat and is more efficient, since the MOSFET’s on resistance is inversely proportional to $V_{drv}$. Measured efficiency curves for four operating conditions are shown in Fig. 8, where the TMU and fan were enabled or disabled. In all cases, the increased airflow results in a slightly higher efficiency as expected. The TMU has a minor impact on the efficiency, while it improves the reliability by reducing both the average and peak temperatures, as shown in subsequent tests.

Infrared (IR) images were taken using a FLIR T300 camera to illustrate the temperature distribution of the VRM with the TMU enabled and disabled, under the presence of a non-uniform air-flow. The IR image with the TMU disabled is shown in Fig. 9, where all phases operate with an equal peak current command of $i_{c,1-4} = i_{c}/4$. The fan was positioned parallel to the plane of the PCB with an airflow direction as indicated in Fig. 9. The IR camera provides peak and average temperatures for the boxes defined around each power-stage, as shown in Fig. 9.

The tabulated data from Table II indicates a mismatch of 8.9°C between average temperature of phase 1 and phase 3 when the TMU is off. This is mainly attributed to the non-uniform airflow, in addition to layout and parasitic component variations. A subsequent IR image taken with the TMU enabled is shown in Fig. 10. The maximum difference in the average temperature between all phases is reduced from 8.9 °C to 1.4 °C, and the peak phase temperature is reduced from 64 °C to 60 °C within the power-stage area. This clearly shows the effectiveness of the TMU for

<table>
<thead>
<tr>
<th>Phase No.</th>
<th>Current (A)</th>
<th>Peak Temperature (°C)</th>
<th>Average Temperature (°C)</th>
<th>Current (A)</th>
<th>Peak Temperature (°C)</th>
<th>Average Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10.16</td>
<td>50.1</td>
<td>43.6</td>
<td>12.72</td>
<td>59</td>
<td>48.3</td>
</tr>
<tr>
<td>2</td>
<td>9.96</td>
<td>57.4</td>
<td>48.9</td>
<td>10.43</td>
<td>60</td>
<td>49.1</td>
</tr>
<tr>
<td>3</td>
<td>10.25</td>
<td>64.2</td>
<td>52.7</td>
<td>8.18</td>
<td>55.9</td>
<td>48.4</td>
</tr>
<tr>
<td>4</td>
<td>10.1</td>
<td>62.6</td>
<td>52.5</td>
<td>9.17</td>
<td>58.1</td>
<td>49.7</td>
</tr>
</tbody>
</table>

Fig. 7. Measured temperature for the multi-phase converter with the fan disabled.

Fig. 8. Measured efficiency for the four-phase converter.

Fig. 9. IR image with TMU disabled, and a total $I_{out} = 40$ A. The arrow indicates the direction of air-flow.

Fig. 10. IR image with TMU enabled, with a total $I_{out} = 40$ A. The arrow indicates the direction of air-flow.
achieving a uniform steady-state temperature distribution. The temperature data is measured independently from the embedded sensors using the IR camera, which confirms correct operation. It should be noted that the air-flow distribution used in this work is not necessarily typical for VRMs, but was used to intentionally generate a significant temperature differential in order to verify the TMU performance in extreme cases. The steady-state peak inductor currents $i_{c1-4}$ from TMU values are given in Table II. There is a ±16% variation in the $i_{c1-4}$.

A transient load step was carried out to investigate the dynamics of the TMU. The sampled temperature and peak current distributions for the multi-phase converter with the TMU disabled and enabled for a 30-50-20 A load step are as shown in Fig. 11 and 12, respectively. The TMU successfully maintains a uniform temperature distribution in all four phases, while the currents are re-distributed. The current offsets $\Delta i_{c1-4}$ remains fixed immediately following a load step due to the low bandwidth of the thermal compensators. Feedforward from the current loop to the thermal loop could be added, however it does not seem necessary, given the superior response seen in Fig. 12.
A final test was performed by subjecting the converter to a realistic current profile, obtained experimentally from a processor in a video decoding application. The current profile was programmed into the memory of an electronic load. The resulting thermal transient response is as shown in Fig. 13 and 14 with the TMU disabled and enabled, respectively. The TMU maintains a uniform current distribution even in the presence of realistic dynamic loads. The effectiveness of the TMU can be easily observed from the measured standard deviation of the phase temperatures with TMU disabled and enabled as shown in Fig. 15.

V. CONCLUSIONS

An active thermal management control technique for multi-phase peak current mode controlled VRMs is introduced. A simple lumped parameter thermal model served as the basis for the development of the TMU. IR images and on-board temperature measurements confirm the effectiveness of the TMU even under rapid load transient. The ability to equalize the temperature across different converter phases ensures greater reliability.

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REFERENCES