

# 10 MHz Peak Current Mode DC-DC Converter IC with Calibrated Current Observer

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**Abstract**— Current program mode controllers have not been widely adopted in low-power high frequency dc-dc converters due to the need for an integrated high gain-bandwidth current sensor circuit. This paper presents a peak current program mode controller IC with integrated power-stage that operates at 10 MHz and does not require any high gain-bandwidth analog circuitry in current or voltage loops. A custom bi-directional hybrid delay-line architecture emulates the inductor current based on input and output voltages. A novel calibration circuit is introduced to remove the mismatches between the actual and observed inductor current slopes. The controller consumes 210  $\mu\text{A}$  when the calibration block is off and 430  $\mu\text{A}$  during calibration and the peak efficiency of the converter is 87%.

## I. INTRODUCTION

Peak current program mode (CPM) controllers are widely used in dc-dc converters for their advantages over voltage mode controllers such as inherent current-protection, reduced audio susceptibility and simpler controller implementation [1]-[4]. Despite these benefits, CPM controllers have found limited use in low-power high frequency switch-mode power supplies (SMPS) [5]. This is due to the requirement of a high bandwidth current sensing circuit that significantly increases the power consumption and reduces the overall system efficiency compared to a voltage mode controller [6]-[7]. Observer based CPM controllers eliminate the need for an explicit current sensing and are therefore suitable for low-power high frequency SMPS. In [8]-[9] an emulated current program mode (ECM) controller is proposed where the inductor current is artificially reconstructed by integrating the time varying inductor voltage. This technique, which relies entirely on analog circuitry for reconstructing the inductor current, does not take advantage of the full capabilities of modern low-voltage digital CMOS processes. In [10] a digital sensorless current mode (SCM) controller based on a bi-directional delay-line architecture was presented. The design was implemented on a CPLD device as a proof of concept. However due to the limited speed and flexibility of the

device, the proposed architecture is only suitable for DC-DC converters operating below 1 MHz. An additional drawback of the designs proposed in [8]-[10] is that no calibration circuit was implemented in order to eliminate mismatches between the actual and observed inductor current slopes. In general this is an inherent disadvantage of ECM techniques. The mismatches grow over multiple switching cycles due to the integral nature of the ECM controller, and eventually saturate the ECM causing stability problems. Therefore any implementation of ECM controller requires a calibration circuit for proper operation. In this work a mixed-signal ECM integrated circuit (IC) is presented that consists of a current observer, a calibration circuit and integrated power-stage as shown in Fig.1. The main feature of this work is a simple and power efficient CPM controller that is capable of operating with an integrated dc-dc converter switching at 10 MHz. The proposed architecture eliminates the need for a high gain-bandwidth sensing circuit and therefore is suitable for integration with latest CMOS technologies. The current observer provides an instantaneous mapping of the inductor current in digital domain. Since the observed current,  $i_{obs}$ , and controller reference  $i_c[n]$  are both digital, the high speed analog comparator is also eliminated. Additionally a novel calibration circuit is introduced to mitigate the mismatches between observed and actual inductor current slopes.

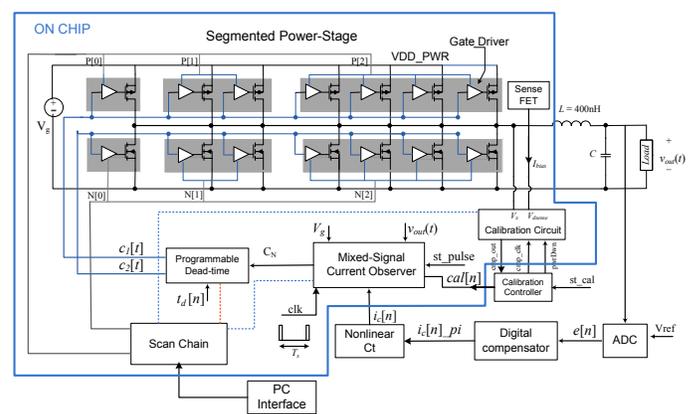


Fig.1: Architecture of mixed-signal ECM controller.

## II. MIXED SIGNAL CURRENT OBSERVER MODULE

A key block of mixed-signal ECM IC is the current observer module as shown in Fig.1. This section discusses the design of the current observer and its key building blocks and also explains its operation as illustrated in Fig.2.

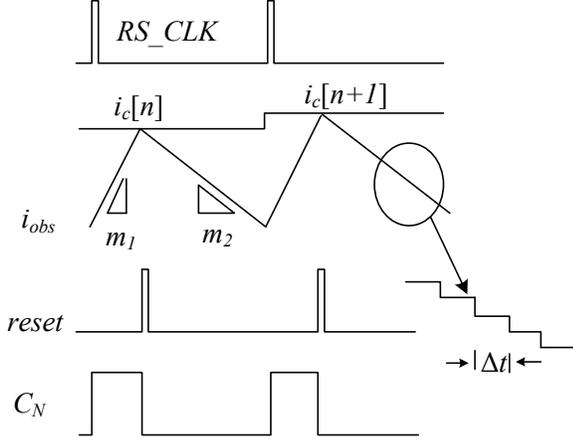


Fig.2: Simplified operation of current observer module.

### A. Hybrid Bi-Directional Delay-Line-Counter Architecture

The current observer architecture is essentially a mixed-signal equivalent of the analog ECM controller [8]-[9]. The observer module shown in Fig.3 consists of a delay bias control block and a hybrid bi-directional delay-line-counter architecture that maps the instantaneous inductor current.

The schematic of the bi-directional delay element used in the observer delay-line is also shown in Fig.3. Similar to voltage mode digital pulse-width modulator (DPWM) architectures [11]-[15], a hybrid combination of delay-line and counter is used in the design of the current observer. The hybrid structure reduces the total number of delay cells required to map the entire range of the instantaneous inductor current, significantly decreasing the power consumption and area of the current observer. The operation of the current observer is as follows: Upon start-up, a pulse,  $st\_pulse$ , is injected in the delay-line. The pulse propagates in the forward (FW/BW, DIR = 1) direction with a propagation delay,  $t_{d1}$ , which is inversely proportional to the slope of rising inductor current:

$$m_1 = (V_g - v_{out}) / L \quad (1)$$

When the pulse reaches the last delay-cell it clocks and increments the counter as demonstrated in Fig.3. The pulse continues to wrap around the delay-line until the counter output is equal to  $i_c < 9:6 >$  and the pulse reaches the delay cell selected by the 6 LSB bits of  $i_c[n]$ ,  $i_c < 5:0 >$ . At this point the reset pulse goes high and the direction of the pulse in the hybrid delay-line-counter structure is reversed (FW/BW, DIR = 0). Subsequently, the pulse propagates in the backward direction with a propagation delay  $t_{d2}$  that is

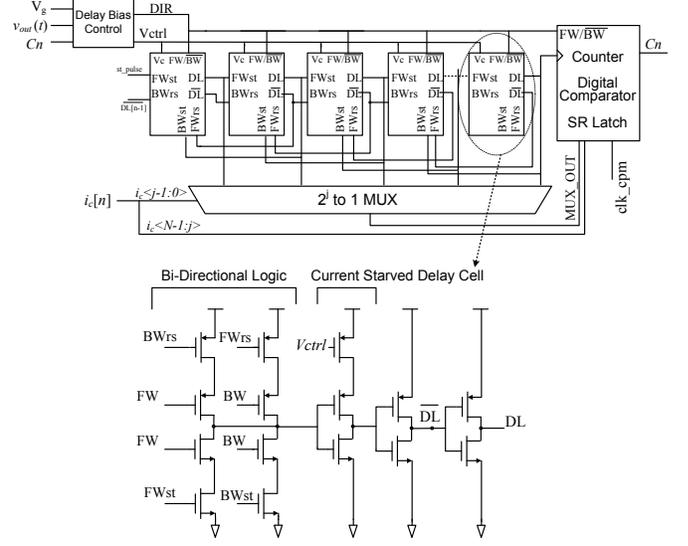


Fig.3: Architecture of the mixed-signal current observer.

inversely proportional to the slope of falling inductor current:

$$m_2 = v_{out} / L \quad (2)$$

The propagation delay in the backward direction is tunable using the 5-bit calibration signal which is used for adjusting the slope ratios. The dynamic range of the hybrid delay-line defines the range of inductor current mapping from  $i_{Lmin}$  to  $i_{Lmax}$ . The quantization interval of  $i_L(t)$  is hence given by

$$\Delta i_{obs} = \frac{(i_{Lmax} - i_{Lmin})}{2^N} \quad (3)$$

### B. Delay Bias Control Block

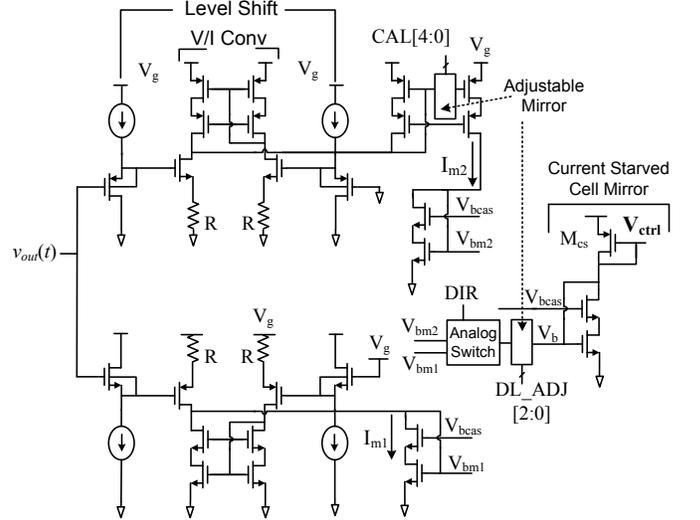


Fig.4: Delay bias control block.

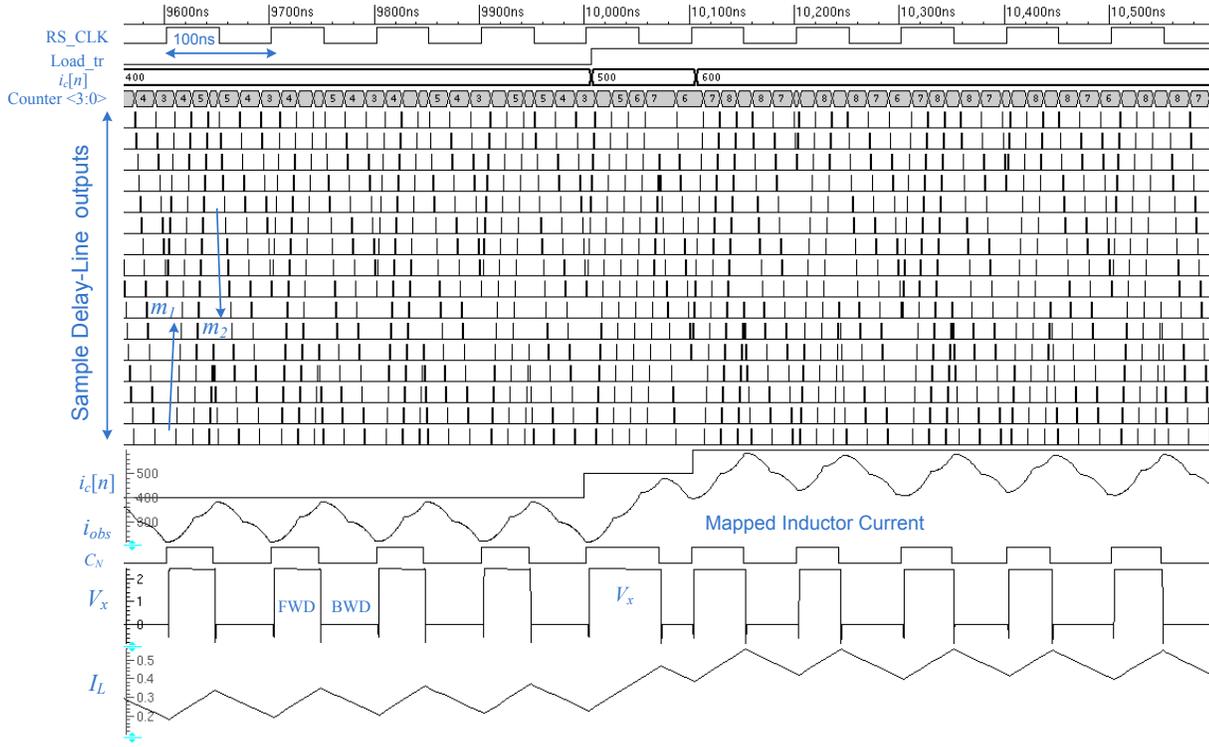


Fig.5: Open loop simulation of current observer with integrated power stage. When the load transient occurs  $i_c[n]$  also changes.

The delay bias control block shown in Fig.4 sets the propagation delay of the pulse in both directions proportional to the inductor current slopes  $m_1$  and  $m_2$ . The circuit is a modified version of the architecture used in [10]. The transistor  $M_{cs}$  mirrors currents  $I_{m1}$  and  $I_{m2}$  to the current starved delay element of Fig.3, when the current observer operates in forward and backward direction, respectively. A combination of level-shifters and wide-swing current mirrors are used to create offset-free V/I converters that generate  $I_{m1}$  and  $I_{m2}$  as given below:

$$I_{m1} = \frac{V_g - v_{out}(t)}{R} \quad (4)$$

$$I_{m2} = \frac{v_{out}(t)}{KR} \quad (5)$$

Where  $K$  is adjusted by 5-bit calibration code, CAL[4:0]. Therefore for the forward operation of the current observer shown in Fig.2,  $I_{m1}$  is mirrored to current starved delay element and  $\Delta t_1 \propto 1/(V_g - v_{out})$ . Similarly for the backward operation,  $\Delta t_2 \propto K/v_{out}$ . A 3-bit delay calibration code, DL\_ADJ [2:0] is programmed using the scan chain shown in Fig.1 in order to compensate for  $t_{d1}$  and  $t_{d2}$  due to process, voltage and temperature (PVT) variations.

### C. Current Observer Simulation

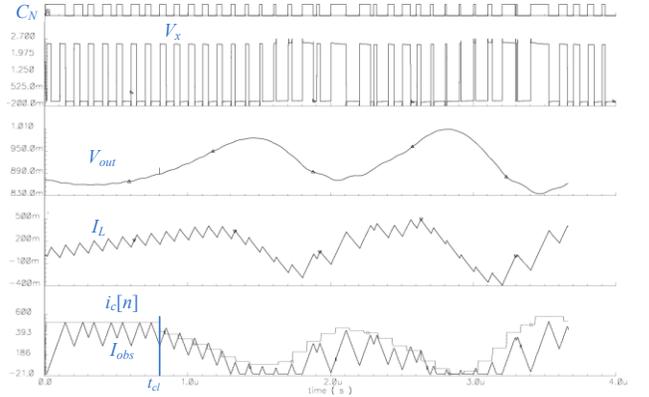


Fig.6: Closed loop Simulation of the current observer where the actual slope ratio is different from the ideal slope ratio.

Transistor-level Spectre simulation of mixed-mode ECM IC of Fig.1 with power-stage operating in open voltage loop is shown in Fig.5. When the load transient occurs at  $t = 10 \mu s$ ,  $i_c[n]$  is also changed to reflect the change in the load current. The operation of current observer in closed current loop is shown in Fig.5. An analog version of the observed current,  $i_{obs}$ , is reconstructed in the simulator test-bench based on the delay-line and counter outputs to simplify comparison with actual inductor current  $i_L$ . When the RS\_CLK goes high at the beginning of the switching period, the main switch turns on and the pulse propagates in the forward

direction with propagation speed proportional to  $m_1$ . When the observed current,  $i_{obs}$  reaches the current command  $i_c[n]$ , the direction of the pulse reverses. As shown in Fig.5 the current observer provides an instantaneous mapping of the inductor current in both directions with power-stage running at 10 MHz.

As discussed before, if the current observer is not calibrated periodically, the ratio of observer slopes defined by the ratio of propagation delays  $t_{d2}/t_{d1}$ , will differ from the ideal inductor current slope ratio  $m_1/m_2$ . In this case as the controller tries to regulate the output voltage by adjusting  $i_c[n]$ , the observer saturates due to its limited dynamic range causing stability problems. This situation is demonstrated in the simulation waveforms of Fig.6. The CAL[4:0] is selected such that the observer slope ratio is different from the actual inductor current slope ratio. The converter initially operates in open loop. When the loop is closed at  $t_{cl}$ ,  $i_{obs}$  gradually saturates to zero as the error between  $i_L(t)$  and  $i_{obs}$  grows with each cycle and the output voltage starts to oscillate. In this case the observer incorrectly predicts that the inductor current is discontinuous. Under this condition the controller does not operate in current-mode and the current observer module behaves as a DPWM.

### III. CALIBRATING THE OBSERVER SLOPES

Various sources contribute to the mismatch between the reconstructed and actual inductor current slopes. The most important factor is the non-linearity of the voltage to delay conversion within the hybrid delay-line. Additionally inductor parasitic introduces non idealities in the actual inductor current waveform that are not mapped onto the observed current. Propagation delays due to gate drivers,  $R_{dson}$  variations and other power-stage related non-idealities also contribute to errors in the observed inductor current. If the ideal ratio of  $m_1/m_2$  is not accurately implemented by the observer, the error is accumulated every switching cycle. Since the digital current observer has a finite range, this will eventually saturate  $i_c[n]$ . The schematic of the calibration block proposed in this work and implemented in mixed-signal IC of Fig.1 is shown in Fig.7.a. To perform calibration, an accurate senseFet is used to periodically compare the peak observed current with the actual peak inductor current and adjust the observer slopes until the peaks are equal. The simulation of calibration scheme with a step input in  $i_c[n]$  is shown in Fig.7.b. A simple sigma-delta DAC [14] converts the  $i_c[n]$  to an analog voltage that is fed to a  $V/I$  converter. The  $V/I$  converter, which does not require high bandwidth analog circuits, creates a bias current based on the analog representation of  $i_c[n]$  and tunable resistor value  $R_s$ . This bias current is mirrored to a senseFET that is  $K$  times smaller than the PMOS switch. The voltage drop across the  $R_{dson}$  of senseFET is then compared with  $V_x$  when the main switch turns off using a clocked comparator. Since the sampling point corresponds to the peak inductor current, this calibration circuit will allow adjusting the peak of the observed current with the

actual inductor current as follows: During calibration mode, the current through senseFET can be represented by

$$I_{Bias} = i_c[n]/R_s \quad (6)$$

If this current is smaller than the peak inductor current ( $I_{Bias} < I_{Lp}$ ), the voltage drop across senseFET is smaller compared to the PMOS switch. Therefore the  $V_{dsense}$  is larger than the  $V_x$  and the comparator output is equal to zero. The calibration controller, shown in Fig.1 then updates the 5-bit calibration code which changes the propagation delay of the reconstructed current's falling slope  $m_2$  such that  $i_c[n]$  increases. This process continues until the comparator output becomes one, at which point  $I_{Lp} = I_{Bias}$ . Due to the integral nature of observer controller the mismatches accumulate over many switching cycles. Therefore the calibration phase needs to repeat with a minimum frequency to prevent saturation of observer controller. When the calibration phase is completed all calibration circuits are powered down to reduce the power consumption of the controller.

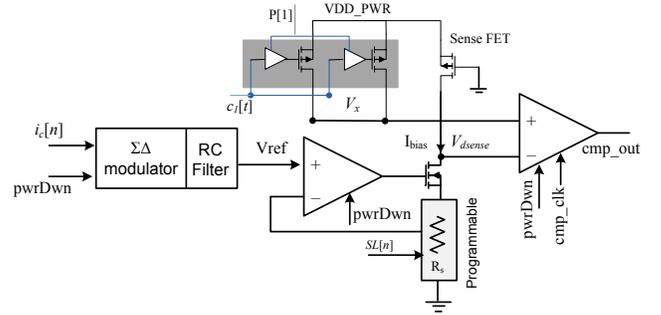
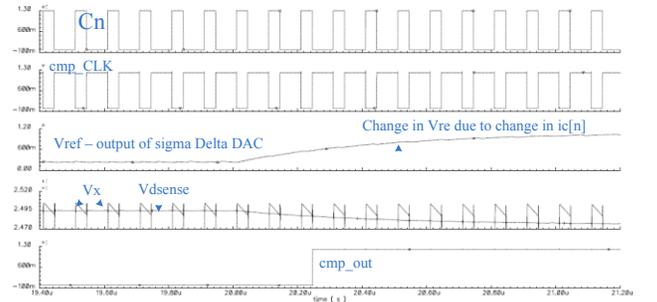


Fig.7: a) Schematic of calibration circuit.



b) Simulation waveforms of calibration circuit for a step in  $i_c[n]$  converter is running in open loop with fixed duty.

### IV. EXPERIMENTAL RESULTS

The digital current observer architecture with the proposed calibration mechanism and a segmented power-stage were fabricated in 0.13 $\mu$ m technology. The chip micrograph is shown in Fig.8 and Table I summarizes its main specifications. While the power-stage can operate above 10 MHz, the current observer is designed for operation below 10 MHz. The total current consumption of the observer

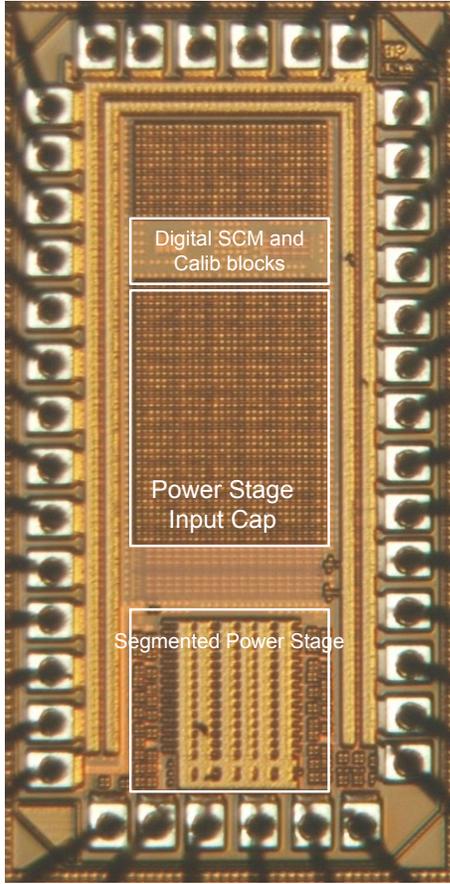


Fig8: Die photo of ECM IC, 1 x 2 mm<sup>2</sup>.

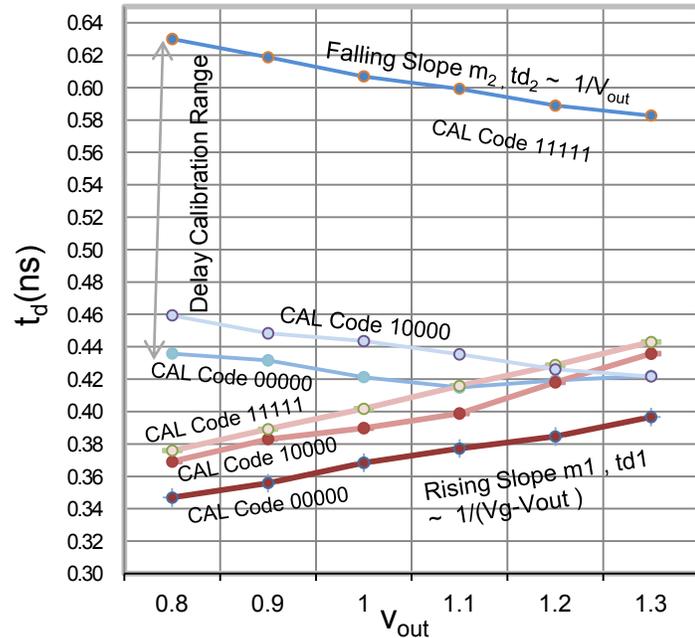


Fig.9: Propagation delays of hybrid delay-line-counter observer.

Specifications	Value	Units
CMOS Process	0.13	$\mu\text{m}$
Area	1 x 2	mm <sup>2</sup>
Input Voltage	2.5	V
Output Voltage	0.8-1.3	V
Rated Load	350	mA
Filter L,C	400, 2	nH, $\mu\text{F}$
Switching Frequency ,	10	MHz
Ron Pmos , Nmos	0.272 , 0.22	m $\Omega$
Supply Analog , Digital	1.2, 2.5	V
Peak Efficiency	87	%
SCM current consumption	210	$\mu\text{A}$
Calib current consumption	250	$\mu\text{A}$

block is 210  $\mu\text{A}$ . The calibration circuit consumes 250  $\mu\text{A}$  of current during the calibration phase and nearly zero when powered down. The measured propagation delay of the hybrid delay-line observer in both forward and reverse directions and versus different output voltages and calibration codes is shown in Fig.9. It also demonstrates the full range of variations in propagation delay based on the highest and lowest calibration codes. Comparison of ideal steady-state slope ratios with that of the observed current is given in Fig.10, for different output voltage and calibration code. In order to demonstrate the operation of the digital

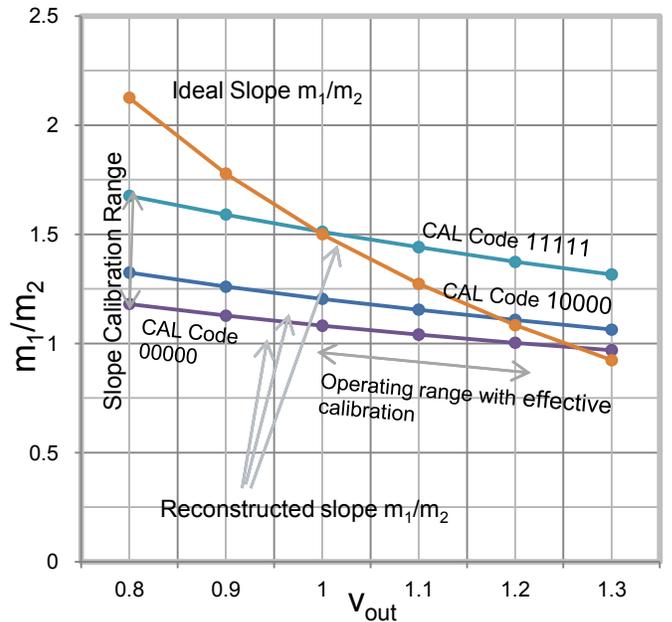


Fig.10: Ideal steady state slope ratio of inductor current and observed current.

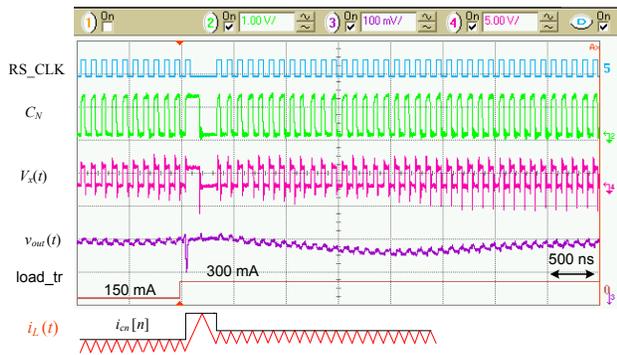


Fig.11: Light to heavy load step response of ECM IC with time-optimal controller. Ch2: CN, 1V/div. Ch4:  $V_x$ , 5V/div. Ch3:  $v_{out}(t)$ , 100mV/div

observer controller with integrated power-stage in closed loop and verify the current loop operation, a simple nonlinear time- optimal controller [17]-[18] is used. Compared to voltage mode, a time-optimal controller can be easily implemented in CPM since only two values of  $i_c[n]$  are required for the peak current and new steady state value. Fig.11 shows the results of the converter operation with time optimal controller. Before load transient occurs, the digital observer block is switching the converter at 10 MHz in closed-loop steady-state mode. Upon receiving the load-transient signal,  $i_c[n]$  is set to the new calculated peak value. The pulse then propagates through the hybrid observer over multiple switching cycles, until it reaches the new current command value. Subsequently, the main switch is turned off and observer is reconfigured so that the pulse prorogates in the reverse direction until it reaches the new steady-state  $i_c[n]$  value. At this point the PI controller resumes its operation. The inductor current  $i_L(t)$  is reconstructed graphically based on the switching waveform, since there is currently no current probe with sufficient bandwidth and

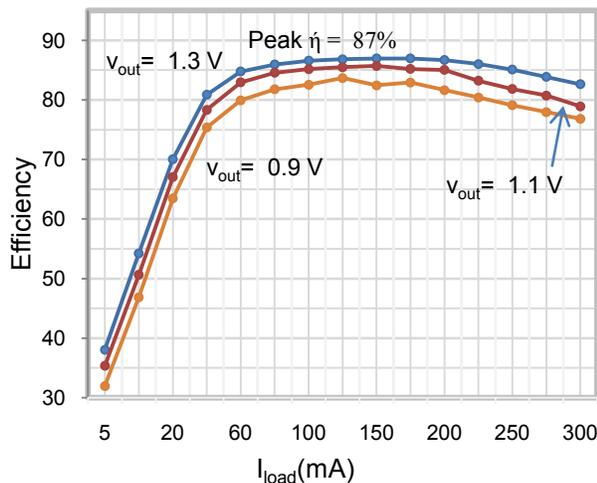


Fig12: The efficiency of the converter running 10MHz,  $V_g = 2.5$

current capability to properly show the inductor current at 10 MHz. Fig.11 demonstrates that the system recovers to the new steady-state value in a single on-off switch operation. Fig.12 shows the efficiency of the converter running at 10 MHz for various output voltages. As shown the peak efficiency of 87% is achieved with all segments enabled. The closed-loop test of calibration remains under investigation.

## V. CONCLUSION

In this paper, an observer based current program mode controller IC with integrated power stage that operates at 10 MHz was presented. The main advantage of this work is elimination of high-gain bandwidth analog circuitry form the controller loop. Additionally, a novel technique for calibrating the observed inductor slopes was presented.

## ACKNOWLEDGMENT

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