DC-DC Converter with Digital Adaptive Slope Control in Auxiliary Phase to Achieve Optimal Transient Response

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***Abstract*— In this paper, a new non-linear control scheme is presented to improve the dynamic response of a current-mode buck converter using a low-cost auxiliary phase. The problems associated with the existing solutions such as undesirable output voltage deviation and insufficient utilization of the auxiliary phase are addressed. This technique employs a digital adaptive slope control in the auxiliary phase, which can accommodate a range of auxiliary phase inductance values while maintaining optimal transient response. A calibration scheme is presented to calibrate the controller against variance in the main and auxiliary phase inductance. The control scheme is experimentally verified on a 500 kHz, 10 V to 2.5 V current-mode buck converter prototype. Charge balancing and optimal transient response are achieved for a range of both positive and negative load steps.**

I. Introduction

In recent years, extensive research has been aimed at improving the dynamic response of dc-dc converters for point-of-load (PoL) applications. Non-linear voltage mode [1]–[4] and current mode [5] controllers have been developed to push the dynamic response of dc-dc converters to the physical limit imposed by the LC filter. Various control techniques using auxiliary circuits have been developed to achieve further improvements in dynamic response without sacrificing efficiency. In [6]–[8], additional power switches are used to increase the voltage across the inductor during transients, thus increasing the inductor current slope. The transient response improvement of this scheme is moderate due to the limits of converter's input and output voltages. This scheme also requires an additional switch to be placed in series with the power-train, which impacts the conduction losses in steady-state. In [9]–[16], a small auxiliary inductor L_x and switches are employed during large load transients to achieve a faster recovery without negatively impacting the efficiency. Among them, two schemes have demonstrated precise voltage recovery using charge balance techniques. In the first scheme, an auxiliary phase was demonstrated with a single turn on-and-off operation during transients in voltage [13] and current mode [14] dc-dc converters. However, it was shown in [14], the value of L_x with respect to L must be chosen precisely according to the V_{out}/V_g ratio, in order to achieve the optimal response. Furthermore, the optimal ratio differs for positive and negative load steps. The second scheme utilizes the auxiliary phase as a constant current source [15], [16] to achieve charge balancing. The drawbacks are the need for a high-bandwidth current sensor and potentially, slope compensation on the high-frequency auxiliary phase, which increases the complexity of the auxiliary phase implementation. In addition, the limited current in L_x leads to sub-optimal response as shown in this paper.

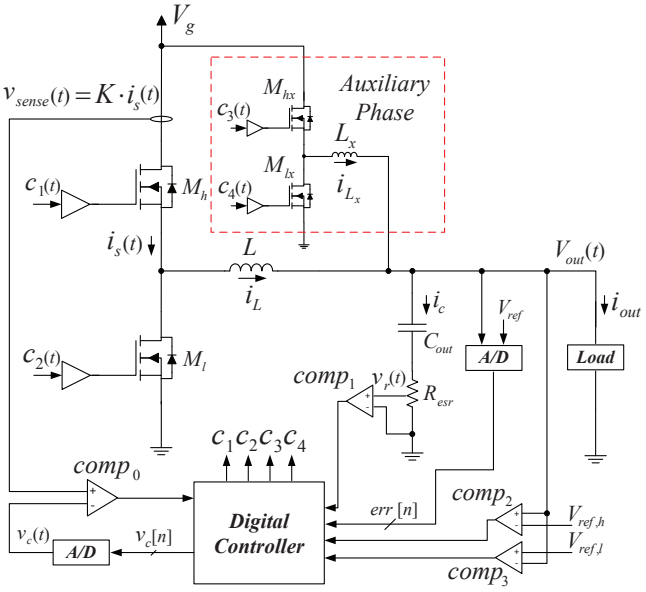


Fig. 1. Simplified architecture of the current-mode buck converter with auxiliary phase.

In this work, the auxiliary phase topology used in [14] and shown in Fig. 1, is developed with a new control scheme to address the limitation on the selection of the auxiliary inductor L_x, while achieving optimal transient response for both positive and negative load transients. The main phase is implemented with current-mode control, which has the advantages of simpler dynamics, inherent cycle-by-cycle current protection and excellent line rejection. The auxiliary phase is controlled with digital pulse-width-modulation (DPWM), which minimizes the incremental cost of the auxiliary phase. The proposed scheme is closely compared to the existing techniques to demonstrate its benefits and trade-offs.

This paper is organized as follows. Section II discusses

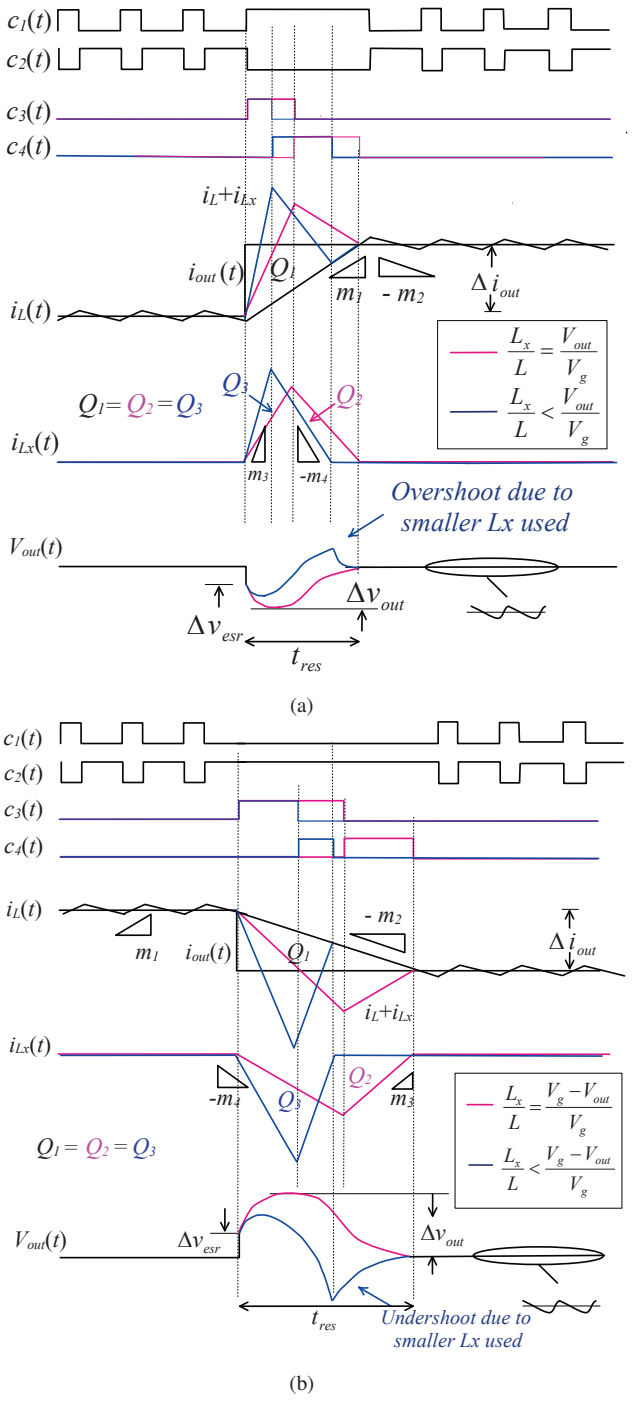


Fig. 2. Ideal waveforms of the existing solution [13], [14] for (a) positive load step and (b) negative load step.

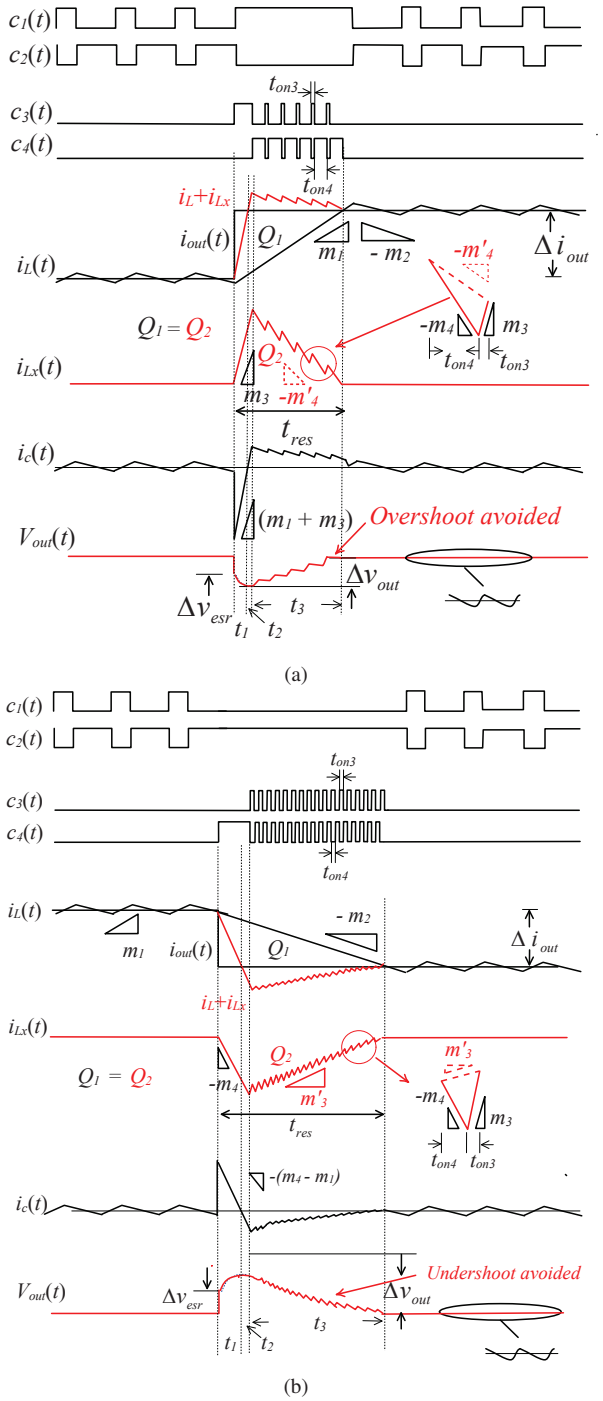


Fig. 3. Ideal waveforms of the proposed solution for (a) positive load step and (b) negative load step.

the existing techniques in detail and introduces the proposed approach. Section III and IV describes the practical implementation of the digital controller and the calibration scheme. Section V presents the simulation results. Experimental results for the prototype are reported in Section VI.

II. Existing and Proposed Control Scheme

In [14], a buck converter with a small auxiliary phase as shown in Fig. 1, is controlled to perform charge balance during load transients with a single turn on-and-off action. $L_x << L$ is chosen to provide rapid energy transfer during transients, while the large L maintains high steady-state efficiency. The RMS current in M_{hx} and M_{lx} is limited by the frequency of large load transients and hence small, low-cost transistors can be used without degrading the efficiency. In future high frequency converters, L_x can potentially be implemented on chip together with M_{hx} and M_{lx}. As shown in Fig. 2, During a transient event, i_L goes directly to i_{out}, and the auxiliary

phase provides the function of charge balancing. The switching pattern of the auxiliary gating signals c_3 and c_4 can be precisely calculated from the load step Δi_{out} and inductor current slopes m_{1-4}:

$$\begin{bmatrix} m_1 & m_2 \\ m_3 & m_4 \end{bmatrix} = \begin{bmatrix} \frac{V_g - V_{out}}{L} & \frac{V_{out}}{L} \\ \frac{V_g - V_{out}}{L_x} & \frac{V_{out}}{L_x} \end{bmatrix} \quad (1)$$

TABLE I

OPTIMAL Δv_{out} AND t_{res} ACHIEVED USING AUXILIARY PHASE

Load Step	Δv_{out}	t_{res}
Positive	$\frac{\Delta i_{out}^2}{2C_{out}\cdot(m_1+m_3)}$	$\frac{\Delta i_{out}}{m_1}$
Negative	$\frac{\Delta i_{out}^2}{2C_{out}\cdot(m_2+m_4)}$	$\frac{\Delta i_{out}}{m_2}$

To achieve the optimal response, charge balancing has to be achieved right at the instant when i_L reaches i_{out}. At the same time, i_{Lx} reaches zero, and the auxiliary phase turns off. This yields the optimal output voltage droop Δv_{out} and best-case response time t_{res}, which are given in Table I. Unfortunately, to satisfy both of the above conditions, the ratio of $L_x/L = V_{out}/V_g$ must be used in order to achieve the optimal response for a positive load step [14]. The corresponding ratio for a negative load step is $L_x/L = (V_g - V_{out})/V_g$. This restriction prevents the reduction of L_x to further improve the transient response and power density. If L_x is not chosen according to the ideal ratio, undesirable overshoot and undershoot are inevitable, as illustrated in Fig. 2.

In the proposed novel approach shown in Fig. 3, the auxiliary switches are controlled such that the effective current slopes of L_x are adaptively set to m_4' and m_3' for positive and negative load steps, respectively. The values of m_4' and m_3' are chosen according to Table II such that optimal response is achieved for any L_x that satisfies $L_x/L < V_{out}/V_g$ and $L_x/L < (V_g - V_{out})/V_g$, and undesired output voltage deviations are avoided. The current slopes of m_4' and m_3' are achieved by switching the auxiliary phase at a fixed duty cycle, and the ratios of the on-times of M_{hx} and M_{lx}, t_{on4}/t_{on3}, are listed in Table II. The choice of the switching frequency of the auxiliary phase should be based on the acceptable voltage ripple caused by its switching and the targeted accuracy of the charge balance. This technique does not require a high resolution DPWM for the auxiliary phase, since the regulation is carried out by the main phase.

TABLE II

PARAMETERS FOR THE ADAPTIVE SLOPE CONTROL SCHEME

Load Step	Effective Slope	t_{on4}/t_{on3}
Positive	$m_4' = \frac{V_g - V_{out}}{L - L_x}$	$\frac{\frac{V_g}{V_{out}} - 1}{1 - \frac{V_g}{V_{out}} \cdot \frac{L_x}{L}}$
Negative	$m_3' = \frac{V_{out}}{L - L_x}$	$\frac{1}{\frac{V_g - V_{out}}{V_{out}} - \frac{V_g}{V_{out}} \cdot \frac{L_x}{L}}$

Unlike using the auxiliary phase as constant current source [15], [16], the proposed approach maintains the optimal response because the switching of the auxiliary phase always occurs after the new i_{out} has been reached, as illustrated in Fig. 4. Operating the auxiliary phase in digital peak current-mode [15] also limits the auxiliary phase current to a finite number of values, which does not provide the fastest transient response for all possible load steps.

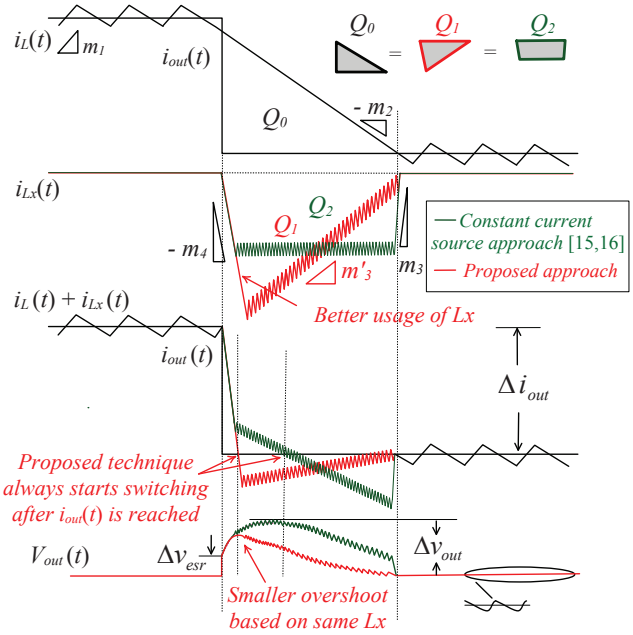


Fig. 4. Comparison between the constant current source approach [15], [16] and the proposed approach.

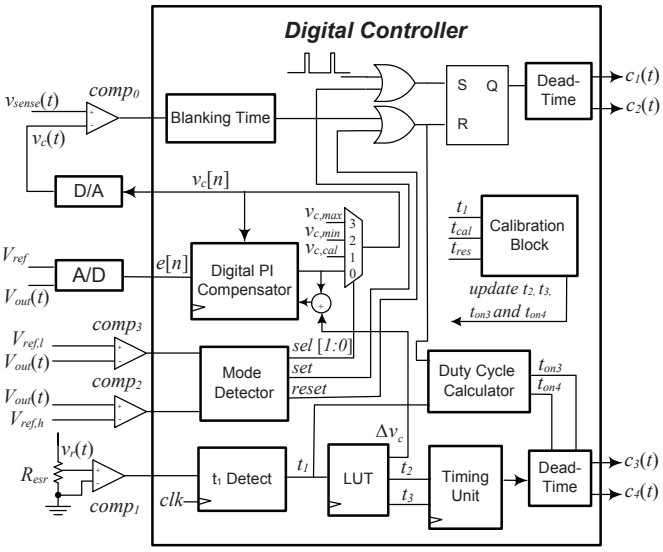


Fig. 5. Architecture of the digital controller.

III. IMPLEMENTATION

The high-level system architecture is shown in Fig. 1, and the ideal switching waveforms are shown in Fig. 3. Load step detection is achieved by monitoring the zero-crossing of the capacitor current $i_c(t)$ using $comp1$ [14]. Compared to the valley detection of $V_{out}(t)$ [1], this method does not require a

high resolution oversampling ADC and is also independent of the ESR of the output capacitor, R_{esr}. A portion of the PCB trace in the ground path of the output capacitor can be used to sense the zero-crossing of $i_c(t)$, and in future high-frequency applications where on-chip capacitors are used, the inherent resistance of the capacitor interconnect could potentially be used. Transient events are detected by $comp2$ and $comp3$. The thresholds $V_{ref,h}$ and $V_{ref,l}$ are set to 50 mV above and below V_{out} such that the initial voltage droop due to ESR of C_{out} is sufficient to trigger $comp2$ and $comp3$. A system clock of 50 MHz is used to provide the time base. The simplified architecture of the digital controller is shown in Fig. 5. For a positive load step, the controller operates as follows:

1) The load-step is detected by *comp3*. The linear PI controller is put on hold and the digital current-command $v_c[n]$ is set to the maximum value of $v_{c,max}$, which maintains peak current protection. M_h and M_{hx} are turned on to ramp up the currents in both L and L_x immediately.
2) The zero-crossing of $i_C(t)$ is detected by *comp1* at the end of t_1, which is recorded by the t_1-detection block. The measured t_1 is fed into a lookup table (LUT) to obtain t_2, t_3 and Δv_c.
3) The auxiliary phase starts to switch at a fixed duty cycle after t_2 and is turned off at the end of t_3. t_{on3} and t_{on4} are calculated to yield an effective slope of m'_4, which ensures that charge balance is achieved when i_L reaches the new i_{out}. The digital current-command $v_c[n]$ of the linear PI compensator is incremented by Δv_c according to the value stored in the LUT before re-activating the linear PI controller.

TABLE III

TIMING PARAMETERS FOR THE PROPOSED CONTROL SCHEME

Load Step	t_2	t_3	Δv_c
Positive	$\frac{L_x}{L}\cdot t_1$	$(\frac{L}{L_x}-\frac{L_x}{L})\cdot t_1$	$(m_1+m_3)\cdot t_1$
Negative	$\frac{L_x}{L}\cdot t_1$	$(\frac{L}{L_x}-\frac{L_x}{L})\cdot t_1$	$(m_2+m_4)\cdot t_1$

For a negative load-step, the controller operation is similar. The parameters t_2, t_3, Δv_c are given in Table III. To obtain an accurate Δv_c, the steady-state current ripple in i_L is tracked with the 50 MHz system clock which is synchronized with the 500 kHz switching clock. A correction term is then added to Δv_c based on when load transient occurs during a switching period. For low V_{out}, $t_{on3} << t_{on4}$, therefore t_{on3} is selected to have the minimum pulse-width allowed by the gate-driver. Therefore t_{on4} and the auxiliary phase switching frequency, f_{sx}, vary as a function of L_x to achieve different m'_3 and m'_4.

IV. CALIBRATION

The proposed control scheme requires the knowledge of the values of L and L_x for the LUT. The actual values of L and L_x can be obtained by calibration. The ratio of t_{on3}/t_{on4} and timing parameters t_2 and t_3 only depend on L/L_x, which can be obtained from t_{res}/t_1, as shown in Fig. 6, through the following relation:

$$\frac{t_{res}}{t_1}=\frac{m_1+m_3}{m_1}=\frac{L}{L_x}+1 \tag{2}$$

The accuracy of the digital current-command $v_c[n]$ setting the load current after a transient event also impacts the response time. According to Table III, $\Delta v_c[n]$ is function of the inductor current slopes, m_{1-4}. To calibrate it, the values of L and L_x need to be obtained. L_x/L can be found from (2), and L can be measured by incrementing the current-command by a known Δv_{cal} during a transient event, and the time it takes for i_L to reach this $v_{C,cal}$, t_{cal}, is proportional to the value of L.

$$t_{cal}=\frac{\Delta v_{cal}}{m_1}=\frac{\Delta v_{cal}}{V_g-V_{out}}\cdot L \tag{3}$$

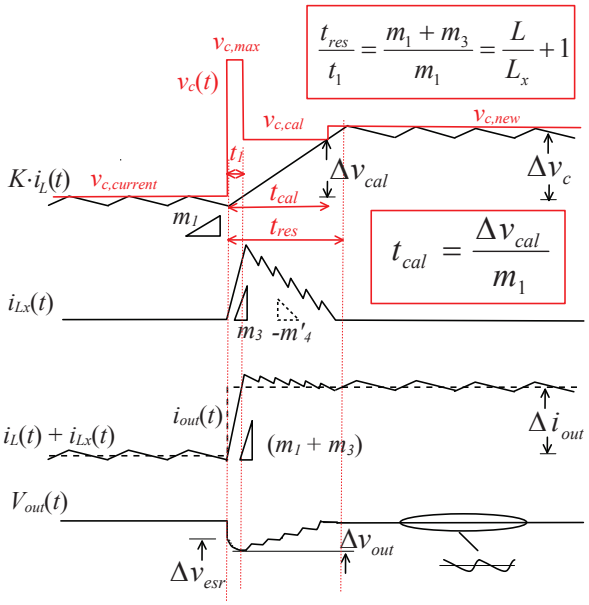


Fig. 6. Proposed calibration for the adaptive slope control.

Initially the controller is pre-loaded with a LUT that is based on the best knowledge of L and L_x. During a large load step, the calibration block re-writes the LUT, and it operates as follows (see Fig. 6):

1) After a load-step is detected by *comp3*, the value of the previous current-command $v_{c,current}$ is saved internally, and the current-command $v_c[n]$ is set to the maximum value of $v_{c,max}$ to ramp up i_L. M_{hx} is turned on to ramp up i_{Lx}.
2) The zero-crossing of $i_C(t)$ is detected by *comp1* at the end of t_1 to indicate load current has been reached. Then the current-command $v_c[n]$ is incremented by Δv_{cal} to $v_{C,cal}$, and *comp0* is masked to prevent reset to the PWM SR-latch. The time i_L reaches $v_{C,cal}$, t_{cal}, is recorded. The auxiliary phase operates normally following the timing parameters in the original LUT.
3) After t_{cal} is obtained, the digital current-command $v_c[n]$ is incremented by Δv_c to $v_{C,new}$, and the time it takes

i_L to reach $v_{C,new}$ is recorded as t_{res}. Then the linear PI controller is re-activated.

4) With the values of t_1, t_{cal} and t_{res}, the calibration block calculates a new set of parameters according to (2) and 3, Table II and III, and updates the LUT. The new table is used for the upcoming load transients.

The proposed on-line calibration takes place during converter operation, which compensates for the inductor's temperature coefficient.

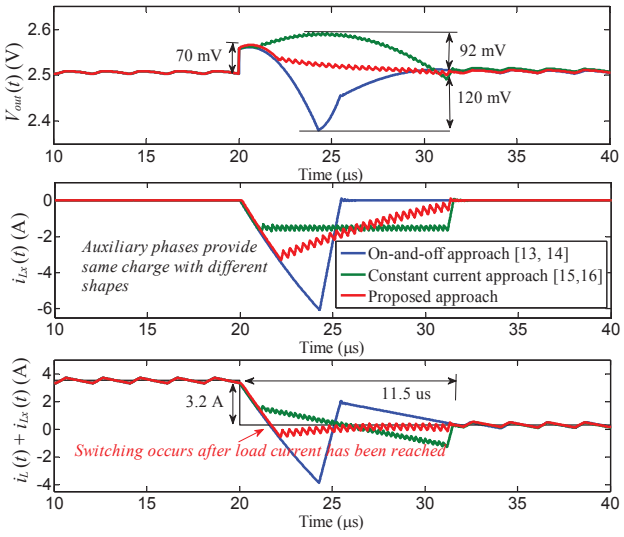


Fig. 7. Cadence AMS simulation of the three discussed techniques for a 3.2 A negative load step.

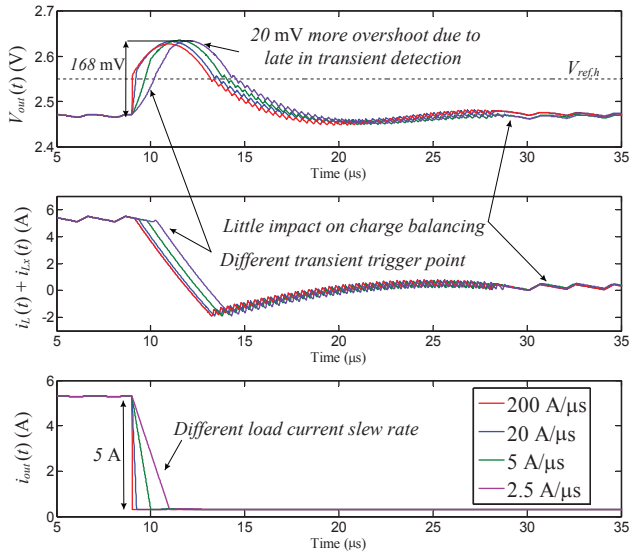
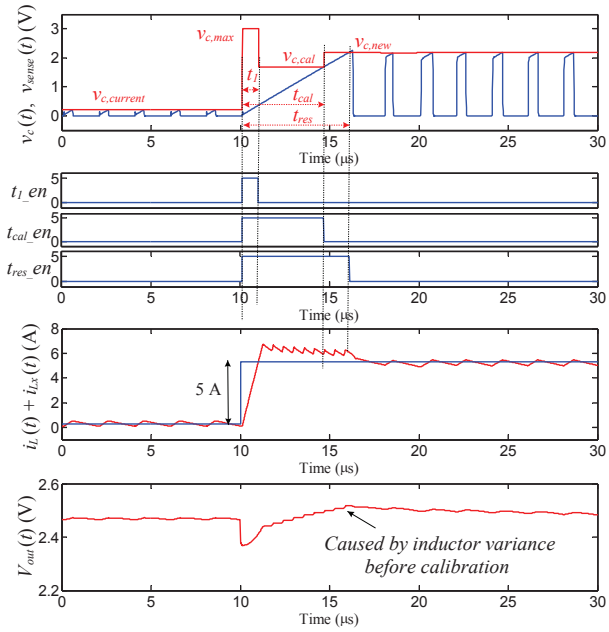


Fig. 8. Cadence AMS simulation of the proposed scheme response at four different load current slew rates for a 5 A negative load step.

V. Simulation

An accurate mixed-signal simulation of the full closed-loop system was performed using Cadence AMS Designer. The simulated response for a 3.2 A negative load step is shown in Fig. 7. The existing approaches [13], [15], [16] were also simulated using the same converter parameters (listed in Table IV) and are super-imposed. The proposed approach maintains the optimal response, which are 70 mV in Δv_{out} and 11.5 μs in t_{res}. Approach [13] produces an undesired undershoot of 120 mV, and approach [15], [16] yields a sub-optimal response of 92 mV.



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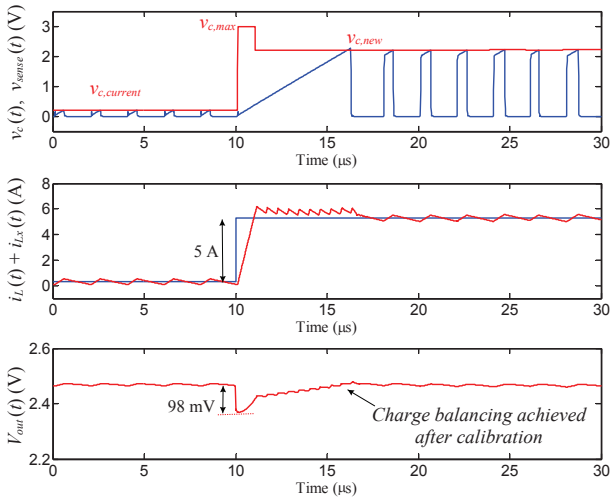


(b)

Fig. 9. (a) AMS simulation of the proposed calibration scheme) (b) AMS simulation of the response after calibration.

The proposed control scheme performs charge balancing based on load steps with infinite slope, and it does not require sampling the output voltage. Therefore if the load current slew rate is not much larger compared to the slope of (i_L + i_{Lx}), excess charge will be provided or removed by the auxiliary phase. Interestingly, a slower load current slew-rate also causes a longer delay in the transient detection circuit,

TABLE IV

PROTOTYPE SPECIFICATIONS

Specification	Value	Units
Input Voltage, V_g	10	V
Output Voltage, V_{out}	2.5	V
Rated Load, I_{load}	7	A
R_{on} for $M_{h,l}$ (SO-8)	20	mΩ
R_{on} for $M_{hx,lx}$ (SOT-23)	57	mΩ
Output Capacitor C_{out}	50	μF
Total Capacitor ESR R_c	$\approx$ 30	mΩ
Filter, L, L_x	10, 1.5	μH
Switching Freq., f_s	500	kHz
Aux. Phase Switching Freq., f_{sx}	$\leq$ 3	MHz

which actually compensates for the finite slew-rate. A mixed-signal simulation was performed to illustrate this effect for a negative 5 A load step with four different current slew-rates, as shown in Fig. 8. Although the excess charge needs to be removed is smaller as the load current slew-rate reduces from 500 A/μs to 2.5 A/μs, the delay in transient detection circuit becomes larger, which corrects the charge balancing. The net effect is a 20 mV higher voltage droop, and impact on charge balancing is small.

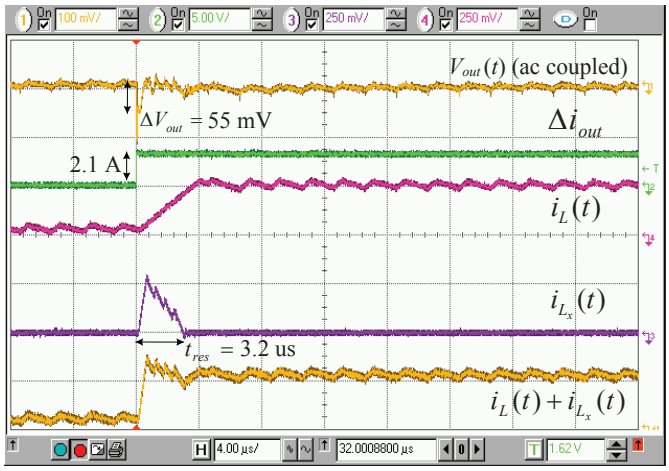
A simulation result was performed to illustrate the calibration process, as shown in Fig. 9. The LUT was pre-loaded for L= 10 μH, and the simulation was performed on a system with L = 8.2 μH. The enable signals of the counters for t_1, t_{cal} and t_{res} are shown. During the calibration, since the old LUT was used, an error in charge balancing is clearly visible. After the calibration is completed, the LUT is updated and charge balancing is achieved for this system with L = 8.2 μH.

VI. EXPERIMENTAL RESULTS

An experimental 500 kHz, 10 V to 2.5 V buck converter prototype was built to demonstrate the control scheme. The digital controller is implemented on a Xilinx FPGA. The system parameters are listed in Table IV. An undershoot of 55 mV, which is dominated by the ESR drop and an overshoot of 80 mV are achieved for a load step of 2.1 A, as shown in Fig. 10. In Fig. 11, the response for a load step of 3.2 A is shown and the operation of the main phase is illustrated. As shown in Fig. 12, the proper operations of the auxiliary phases as well as the load detection circuit are demonstrated. An undershoot of 100 mV (ESR drop dominated) and an overshoot of 120 mV are achieved for a load step of 3.2 A. The deviation from the ideal achievable overshoot, which is 70 mV, as shown in the simulation result in Fig. 7, is due to the delays in transient detection circuit, digital controller and MOSFET gate-drivers.

VII. CONCLUSION

The digital adaptive slope control scheme is verified to actively adjust the charge balancing rate such that the undesired voltage deviations are eliminated, and the optimal response is maintained for both positive and negative load steps with different current slew rates. Neither the control scheme nor the load detection circuit require oversampling



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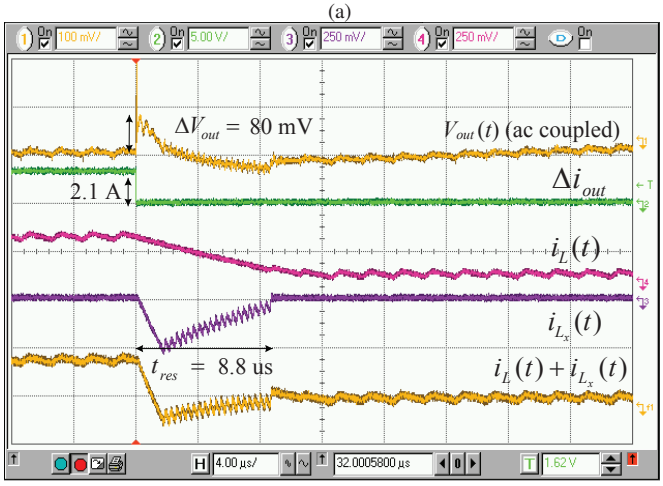

(b)

Fig. 10. Dynamic response for (a) positive Δi_{out} of 2.1 A (4 μs/div, 2.5 A/div) (b) negative Δi_{out} of 2.1 A (4 μs/div, 2.5 A/div).

of $V_{out}(t)$. A calibration scheme is also presented to calibrate the controller against variance in main and auxiliary phase inductance. The ideal transient improvement on ΔV_{out}, in this case, is $K = (1 + L/L_x) = 7.7\times$, compared to a single-phase system with the same L and C_{out}.

ACKNOWLEDGMENT

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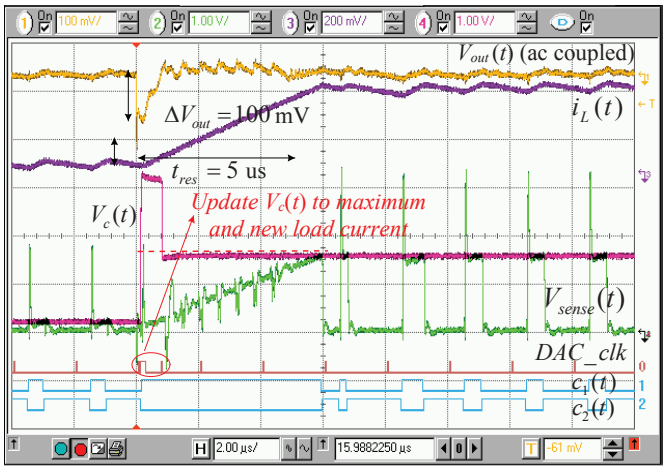

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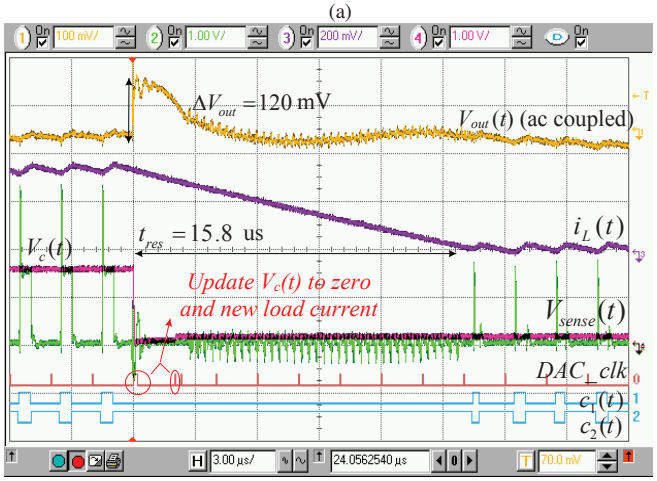
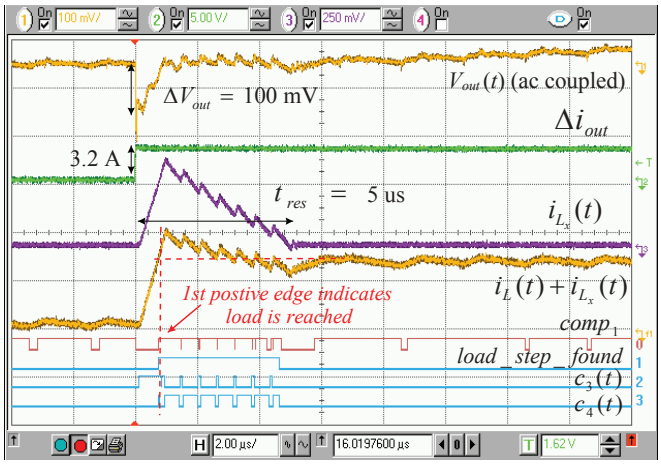


(b)

Fig. 11. Main phase operation for (a) positive Δi_{out} of 3.2 A (2 μs/div, 2 A/div) (b) negative Δi_{out} of 3.2 A (3 μs/div, 2 A/div).



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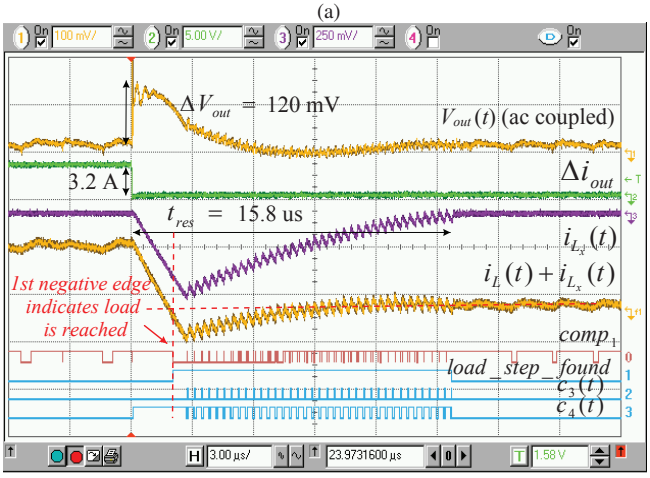

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Fig. 12. Auxiliary phase and load detection circuit operations for (a) positive Δi_{out} of 3.2 A (2 μs/div, 2.5 A/div) (b) negative Δi_{out} of 3.2 A (3 μs/div, 2.5 A/div).

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