Versatile Capabilities of Digitally Controlled Integrated DC-DC Converters

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Abstract— **The increasing need to incorporate complex control features in switched mode power supplies (SMPS) in a CMOS compatible environment has spurred the study of digitally controlled integrated dc-dc converters. Designers continuously examine various design considerations for the implementation of these power converters, including topology choices, digital vs. analog control scheme, power conversion efficiency optimization, advanced passive component technologies, and power transistors. This paper highlights some of our recent work on integrated dc-dc converters with a particular focus on outlining the novel features that are only possible with digital controllers. More specifically, recent advances such as segmented output stage, segmented gate driver, dead-time control, and transient suppression are reviewed.**

I. INTRODUCTION

Low-power digitally controlled dc-dc converters have shown steady improvement since the first counter based digital pulse-width modulator (DPWM) design [1]. The introduction of the delay-line based DPWMs [2] made digital controllers a viable option in low power portable environment. Traditional digital controller designs are intended to mimic the functionality of conventional analog compensators. Therefore, most digital controllers can only have similar performance as their analog counterparts, typically at a higher implementation cost. The true capability of low-power digital control becomes apparent with the introduction of more flexible designs, such as the use of segmented output stage to dynamically adjust the size of the output transistors according to load conditions, in order to maintain high power conversion efficiency [3]-[5], and one-step dead-time correction scheme to continuously optimize the dead-times for the power transistors [6]. Digital controllers also have the ability to switch seamlessly between linear and nonlinear operating modes and achieve near-optimal transient performance [7].

This paper is a brief highlight of our recent developments in integrated dc-dc converters, with a particular focus on outlining the novel features that are made possible with the use of digital control and integrated SMPS. This is by no means a complete survey, as there are many high level research activities in this area available in the literature.

II. EFFICIENCY OPTIMIZATION

The conversion efficiency of dc-dc converters is usually the primary concern in power supply design. While SMPS are known to be much more efficient than linear voltage regulators, power conversion efficiency is a function of load current and falls off rapidly at light load. The peak efficiency is determined by the choice of switching frequency, inductor size, on-resistance of the power MOSFETs and parasitic elements. To accommodate the wide range of load current required by today's point-of-Load (POL) converters, many techniques have been proposed to dynamically adjust the modes of operation to maximize the overall efficiency.

In [3]-[5], digitally controlled converters with segmented layout of the power MOSFETs in their output stages were implemented. The load current is monitored continuously and the digital controller determines the best size of power MOSFET to be used [3]. This allows an optimal trade-off between gate drive loss (minimized with small effective transistor size) and conduction loss (minimized with large effective transistor size) for a given load current. An improvement in power conversion efficiency of up to 7.5% at light-load was reported for a 4.2V-to-1.8V, 4MHz integrated converter as shown in Fig. 1 [3]. The measured efficiency improvement for the second generation of the converter is as plotted in Fig. 2. To further demonstrate the effectiveness of this automatic transistor size selection feature, a load-prediction technique was proposed in [5]. In this example, a digital class-D audio amplifier, often found in portable MP3 players, is used as the load. The required output current is predicted based on the digital audio data stream, which is readily available in class-D audio amplifier systems. With load prediction, the power MOSFET sizing and the expected load current requirement can be synchronized, and the converter can always operate at optimum efficiency. This digital control method also eliminates the need for precise analog circuitry for current sensing, making the system suitable for integration with advanced digital CMOS

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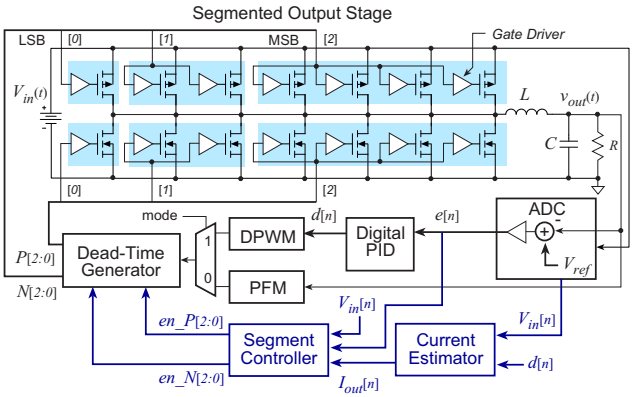

Figure 1. Architecture of a dc-dc converter with segmented output stage. A current estimator is used to determine the number of segments (power transistor size) to be used in real-time.

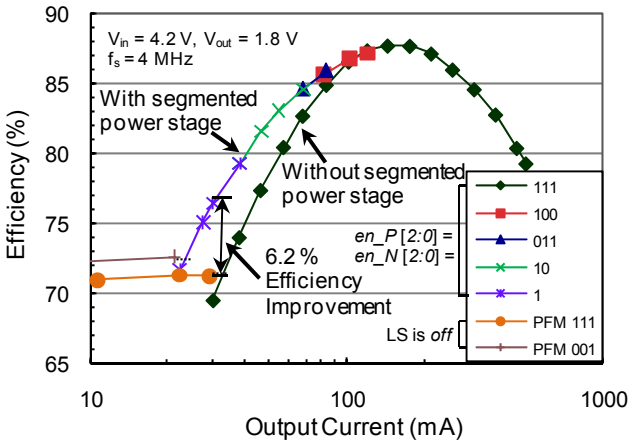

Figure 2. Measured improvement in power conversion efficiency for the same dc-dc converter with and without segmented power stage.

technologies. The use of digital control also allows the incorporation of traditional PWM-PFM mode-hopping method to achieve dynamic efficiency optimization over a wide range of operating conditions [3]-[4].

For integrated dc-dc converters running in the multi-MHz range, fast gate drivers are necessary to minimize the turn-on and off times of the power MOSFETs, in order to reduce the switching losses. However, these high current drivers are usually accompanied by a significant amount of gate drive loss [8]. Under light load conditions, the gate drivers' power consumption can easily become comparable or even greater than the switching loss as shown in Fig. 3. To further improve light load efficiency, a segmented gate driver with adjustable driving capability was proposed as in Fig. 4 [8]. Eight identical gate driver segments are connected in parallel. The effective drive strength can be adjusted through a 3-bit digital bus, turning on one or more segments at a time. The measured converter efficiency using a segmented gate driver is as shown in Fig. 5. With lower gate driving capability at light load, as much as 7% efficiency improvement can be obtained.

In synchronous dc-dc converters, non-overlapping dead-time is required to eliminate the conduction loss induced by

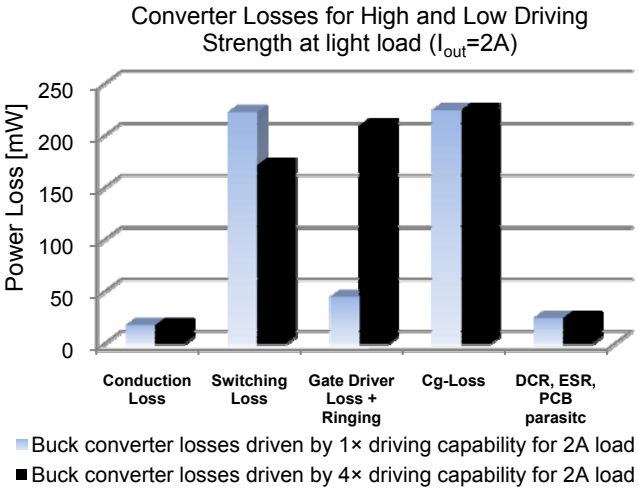

Figure 3. Loss analysis of a dc-dc converter at light load where gate drive loss is a significant component.

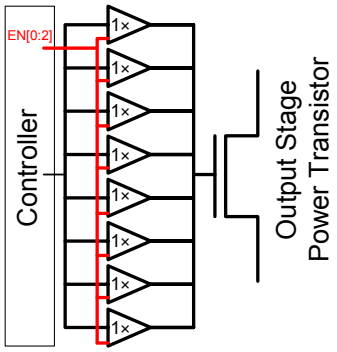

Figure 4. Segmented gate driver circuit with adjustable driving strength.

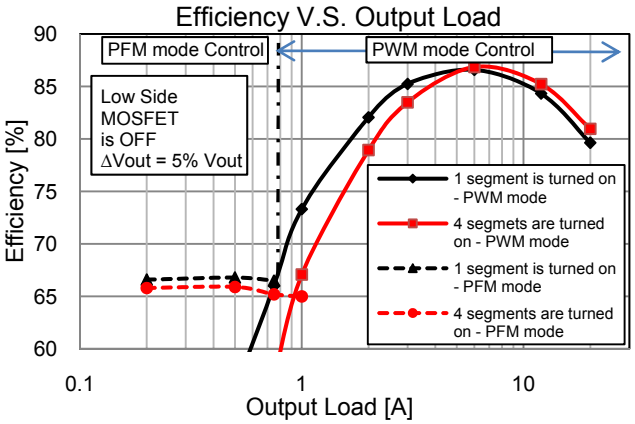

Figure 5. Efficiency versus the output load for gate drivers with 1× and 4× driving strength.

simultaneous cross conduction through the high-side (HS) and low-side (LS) switches, as well as body-diode conduction and reverse recovery loss in the synchronous MOSFET. However, optimum dead-time varies with circuit parameters, operation conditions and temperature, making adaptive dead-time control necessary. Analogue dead-time control schemes require either a current starving charge pump [4], [9] or a complex delay-locked loop [10]. Digital dead-time searching algorithms were proposed with simpler implementation yet

limited reaction speed [11]. A fast-response, one-step dead-time correction method incorporated into an integrated digital dc-dc converter was reported in [6]. The undesirable body-diode conduction in the power MOSFETs is detected by a two-input NOR gate, as shown in Fig. 6. The duration of body-diode conduction is then measured by a delay-line. The measured timing error is then digitally subtracted from the dead-time in the next switching cycle. The plot in Fig. 7 compares the efficiency for cases with fixed dead-time and with continuously adjusted dead-time. It can be seen that, the efficiency is optimized across a wide range of output current. Up to 9.5% improvement in efficiency is achieved.

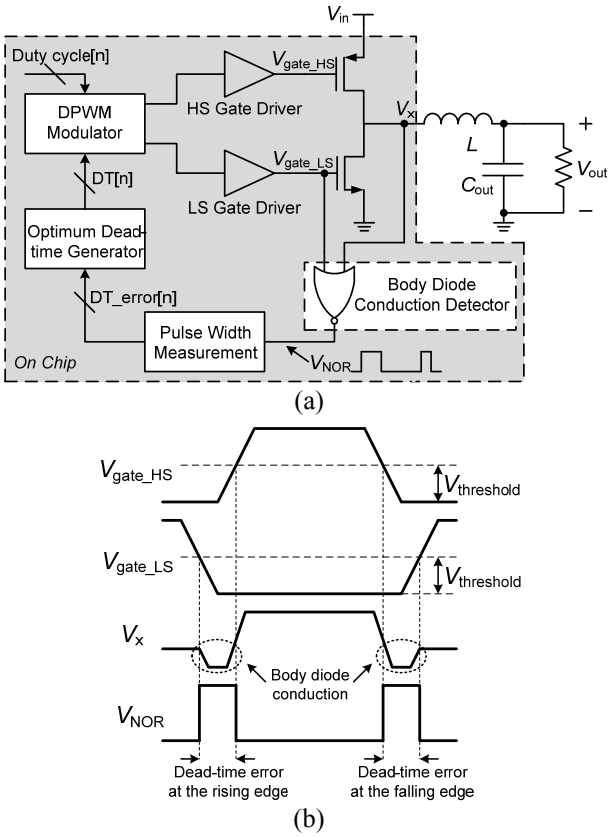

Figure 6. System diagram (a) and theorecital waveform (b) for detecting body-diode conduction with a NOR gate.

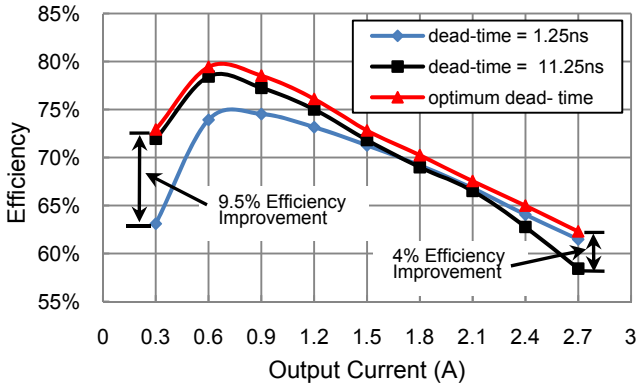

Figure 7. Overall power conversion efficiency is optimized via dynamically adjusted dead-time compared with fixed dead-times cases.

III. Nonlinear Control For Transient Suppression

Dc-dc converters require fast dynamic response to maintain precise voltage regulation in the presence of rapid load steps. Nonlinear control techniques are gaining increasing popularity as it allows the converter to break the limitations of the linear control loop bandwidth. As a result, faster transient response when compared to conventional linear control methods can be obtained [12]. Digital control technologies facilitate the implementation of complex nonlinear transient-suppression algorithms and novel converter topologies that are generally not possible using analog approaches. It also facilitates seamless transition between linear mode for steady state operation and non-linear mode for transient suppression.

Capacitor charge-balance based algorithms have been studied for years [13]-[14]. After a transient event is detected, the digital controller calculates the turn-on and turn-off times of the power switches required to restore the output voltage as well as the inductor current within one switching action. The algorithm provides fast transient response with shortest recovery time.

Transient deviation of dc-dc converters is inherently limited by the current slew-rate of the inductor. To overcome this physical limitation, a Buck converter with a steered inductor was introduced in [15]. After a heavy-to-light load step occurs, the inductor current is steered away from the output capacitor and back to the power source via two extra switches. During this time period, the inductor voltage is increased to the level of input voltage. The slew-rate for the inductor current is greatly increased, thus suppressing the voltage overshoot. An alternate approach to increase this slew-rate without introducing additional power switches in the output path was proved to be effective in [7], [16]-[17]. As shown in Fig. 8, a main converter output stage is connected in parallel with an auxiliary output stage that has a much smaller inductor. The main converter is responsible for steady-state operation. The auxiliary stage is only activated for transient recovery and provides high current slew-rate to suppress voltage deviation. Analog implementation of the dual-stage converter was discussed in [16]. The controller is based on a pair of high-speed hysteresis comparators. It requires multiple switching actions and a series of voltage ringing was observed before returning to steady state. A fully integrated voltage-mode dc-dc converter that utilizes digitally controlled dual output stages was presented in [7]. The micrograph of the IC is shown in Fig. 9. During transient recovery, the switching commands for both the main and the auxiliary output stages are determined based on the capacitor charge-balance principle, aiming at bringing the output voltage back to steady state with one set of on/off switching actions. The non-linear digital controller also predicts the new duty ratio and passes it to the steady-state linear controller, thus achieved a seamless transition. Experimental result in Fig. 10 and 11 shows that the auxiliary stage achieves over 50% reduction in transient overshoot and 80% reduction in recovery time compare to a conventional converter. A current-mode implementation of

the digital dual-stage converter was discussed in [17], where timing of the switching commands during transients is easily obtained using a digital look-up table.

CONCLUSION

Low-power digital controllers offer the flexibility to implement efficiency optimization schemes and novel control techniques that are not readily supported by analog circuit techniques. The continued cost-scaling of CMOS technologies and the growing need for on-chip power management will continue to fuel the popularity of digitally controlled integrated dc-dc converters.

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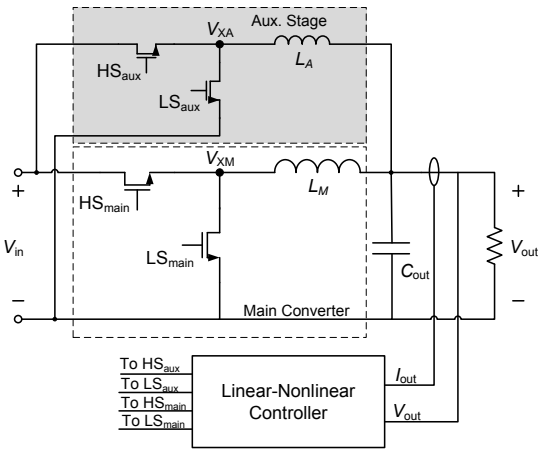

Figure 8. A dc-dc converter with an auxiliary output stage for fast load transient recovery.

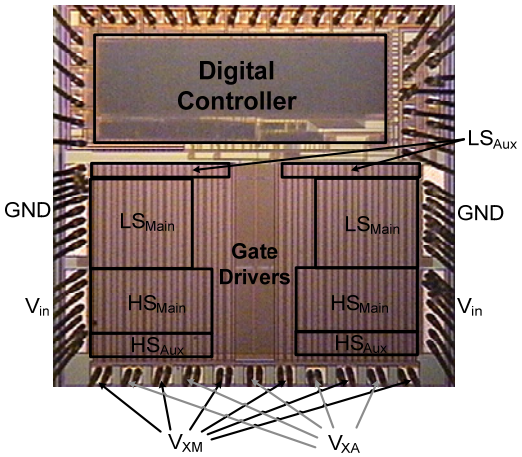

Figure 9. Micrograph of the integrated dc-dc converter implemented in 0.25µm HV-CMOS technology. Die size is 2.35mm×2.35mm.

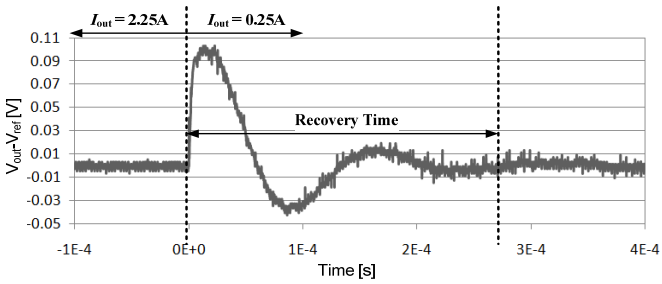

Figure 10. Dynamic response under a 2.25A-to-0.25A load transient using conventional single-stage PID controller.

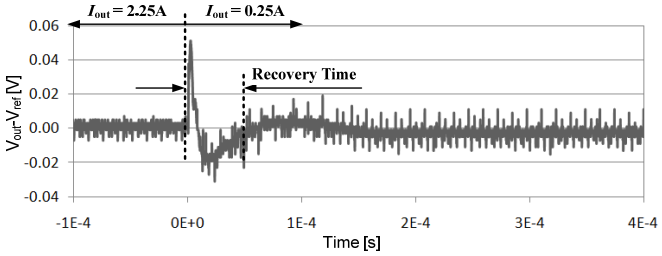

Figure 11. Dynamic response under a 2.25A-to-0.25A load transient using digitally controlled dual output stages.