A Survey of Light-Load Efficiency Improvement Techniques for Low-Power DC-DC Converters

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***Abstract*—Maintaining high efficiency at light-load conditions is extremely important in most modern power management applications, where the predominantly digital loads spend the majority of their time in idle mode. The objective of this paper is to review circuit and system-level techniques used to leverage the existing process technologies in order to achieve high efficiency over a wide load range. The main focus is on low-power dc-dc converters operating above several MHz. Existing fixed and variable frequency schemes are contrasted in this work, namely pulse-frequency modulation with fixed and adaptive on-time, burst-mode control, adaptive gate swing, segmented power-stage, resonant gate drivers and capacitive charge recovery.**

I. Introduction

Dc-dc converters are traditionally designed to achieve a desired efficiency specification at the rated output power. In high power-density applications, the thermal constraints are the primary consideration. In integrated power management ICs for battery powered devices, the system must be optimized to achieve the highest possible battery life, while the statistical distribution of the load current is not well known a priori. The sources of power loss for a synchronous buck converter are shown in Fig. 1, and the approximate equations for the losses are listed in Table I. In most dc-dc converters operating at heavy load, the conduction and switching losses dominate.

Beyond the peak efficiency point, the MOSFET and inductor conduction losses dominate, as shown in Fig. 2(a). Therefore, low R_{on} MOSFETs and a low DCR inductor are needed to meet efficiency specifications. However under light-load conditions, MOSFET switching and gate-drive losses become significant, especially for integrated converters operating beyond several MHz. As a result, the efficiency degrades as the load current decreases, as shown in Fig. 2(b). Light-load efficiency is a major concern in applications where the digital load ICs spend the majority of their time in idle mode.

Extensive research has been conducted in recent years at the device, circuit and system level to improve light-load efficiency. On the device side, recent advances in the $R_{on} \times Q_{gate}$ product of low voltage power MOSFET, integrated schottky diodes, new magnetic materials to implement low DCR inductor as well as high-density, low-ESR capacitor designs all contribute to the overall efficiency improvement. The objective of this paper is to review circuit and system-level techniques used to leverage the existing process technologies in order to achieve the best efficiency over a wide load range.

This paper is organized as follows. Existing fixed and variable-frequency techniques are discussed in Section II and III, respectively, including selected simulation and experimental results. Finally, the schemes are compared in Section IV and a basic selection guidelines are proposed.

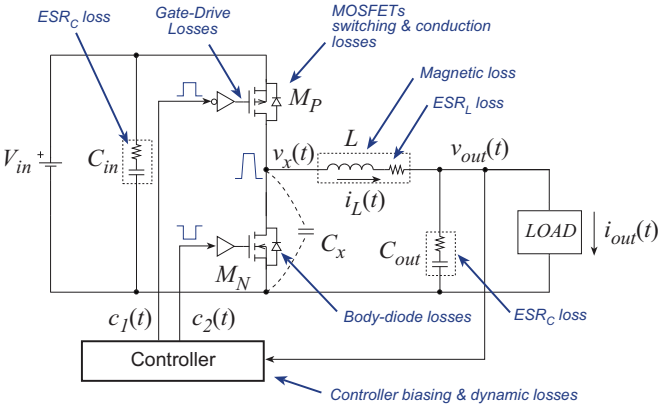


Fig. 1. Sources of power loss in a synchronous buck converter.

TABLE I
Approximate Converter Loss Equations

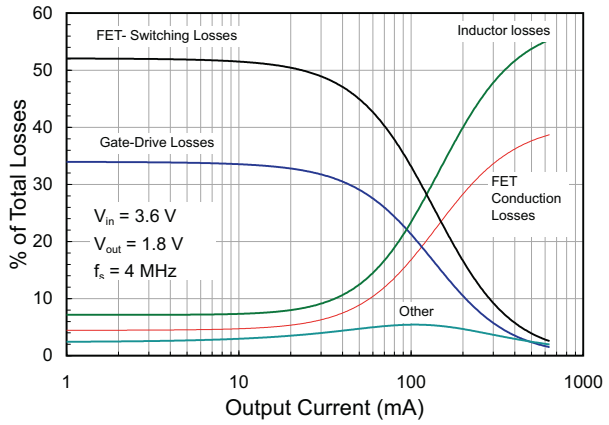
Loss Component	Equation
MOSFET conduction loss, P_{cond}	$I^2_{ds(rms)} R_{on}$
MOSFET switching loss, P_{sw}	$(2C_x V^2_{in} + V_{in} I_{out} t_f) f_s$
Dead-time loss, P_{dt}	$V_d I_{out} t_{dt} f_s$
Body diode reverse recovery loss, P_{rr}	$V_{in} Q_{rr} f_s$
Inductor DCR loss, P_L	$I^2_{L(rms)} R_L$
Capacitor ESR loss, P_{esr}	$I^2_{ac} R_{esr}$
Gate-drive loss, P_{gate}	$Q_g V_{dr} f_s$
Controller loss, P_{ctrl}	$V_{dd}(I_q + I_{dyna} + I_{stat})$

II. Variable Frequency Techniques

Existing variable frequency control techniques that mitigate P_{gate}, such as pulse frequency modulation (PFM) [1]–[12], pulse-skip [13], and burst-mode control [14] are frequently employed in integrated controllers, despite the fact that they generally lead to poor output voltage regulation and electromagnetic interference (EMI) concerns due to the load dependence of f_s.

A. Pulse Frequency Modulation

Reducing the switching frequency at light loads, widely known as pulse-frequency-modulation (PFM) [1]–[12], [15]–[17], is used to reduce the switching and gate drive-losses. In



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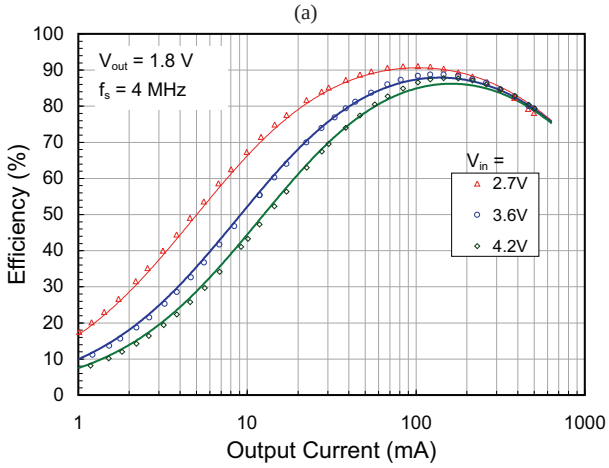


(b)

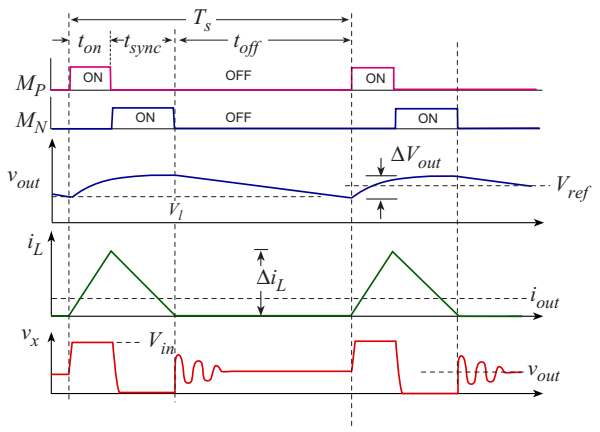
Fig. 2. (a) Calculated percentage of different losses. (b) Calculated (solid line) and measured (symbols) efficiency at different V_{in}.

fact, most low-power commercially available dc-dc converter ICs are capable of switching into PFM at light loads, either automatically through internal sensing mechanisms, or using an external mode selection pin.

The waveforms for PFM with diode emulation, also known as synchronous PFM are shown in Fig. 3. Regulation of $v_{out}(t)$ is usually achieved using a fixed on-time, t_{on}, and automatically controlling the off-time, t_{off}, such that $v_{out}(t)$ reaches a preset threshold V_l at the end of T_s. The ringing at $v_X(t)$ following the turn-off of M_N is due to the LC_x circuit formed by L and the parasitic capacitance at v_X, C_x. This ringing leads to high-frequency noise that can be attenuated with an additional switch across L.

Using a hysteretic approach, the PFM controller can be designed using only a single low-power analog comparator and has been demonstrated with a current consumption as low as 4 μA [7]. Alternatively, t_{on} and t_{off} can be generated using power-efficient delay-lines [8]. Implementing ultra low-power digital controllers for PFM remains a major challenge. Assuming a low ripple-voltage $\Delta v_{out}(t)$, the switching frequency f_s is given by

$$f_s = \frac{I_{out}}{t_{on}^2} \cdot \frac{2V_{out}L}{V_{in}(V_{in} - V_{out})}. \quad (1)$$



(a)

Fig. 3. Ideal waveforms for synchronous PFM.

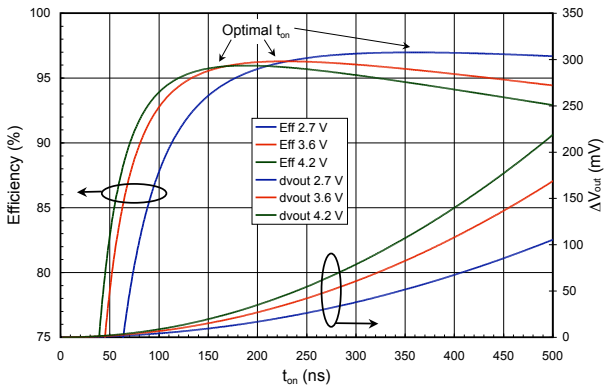


Fig. 4. Theoretical efficiency and output voltage ripple in synchronous PFM mode.

With a fixed t_{on}, f_s changes linearly versus I_{load} to maintain a constant V_{out}. In fact f_s can be used to indirectly sense the output current and trigger a transition back from PFM to PWM mode. By varying t_{on} with both V_{in} and I_{out}, the efficiency can be further optimized [2], [6], [8], [9], [11], [12], as discussed below.

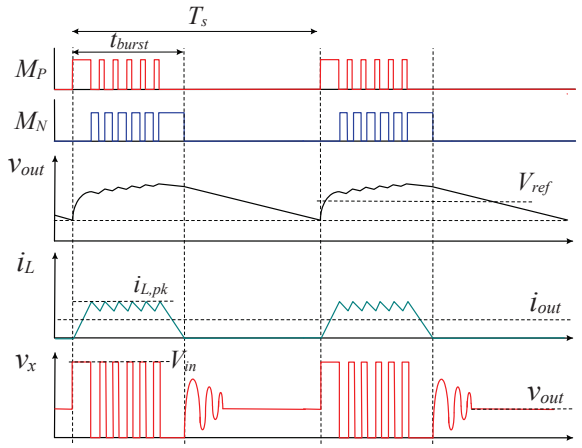
In general, t_{on} cannot be chosen arbitrarily large to maximize the efficiency, since this potentially leads to unacceptably large voltage ripple $\Delta V_{out} \propto t_{on}^2$, as shown in Fig. 4. The optimal PFM on-time $t_{on,opt}$ that maximizes the efficiency is given by

$$t_{on,opt} = \frac{(6V_{in}Q_TL^2)^{\frac{1}{3}}}{(V_{in} - V_{out})^{\frac{2}{3}}} \left(R_{on,P} + R_{on,N} \cdot \frac{V_{in} - V_{out}}{V_{out}} \right)^{-\frac{1}{3}}. \quad (2)$$

The on-time, t_{on}, should therefore be adjusted to maximize the efficiency, given a specific constraint on the maximum ΔV_{out}. One scheme for achieving adaptive t_{on} PFM control (PFM-AOT) is presented in [18]. The measured efficiency in both PFM and PWM mode for an integrated prototype is shown in Fig. 8.

B. Pulse-Skip and Burst-Mode Control

Several variations of PFM have been successfully commercialized, including Burst-Mode (BM) and Pulse-Skip mode. In Burst-Mode, a burst of pulse is periodically used to charge the output capacitor [14]. BM can be operated either with a fixed duty-cycle pulse during the burst, or with current programmed mode control (CPM), as shown in Fig. 5. For the same I_{out} and f_s, Burst Mode results in a lower peak inductor current. The burst-time t_{burst}, can be adjusted to optimize efficiency.



(a)

Fig. 5. Converter waveforms under CPM burst-mode control.

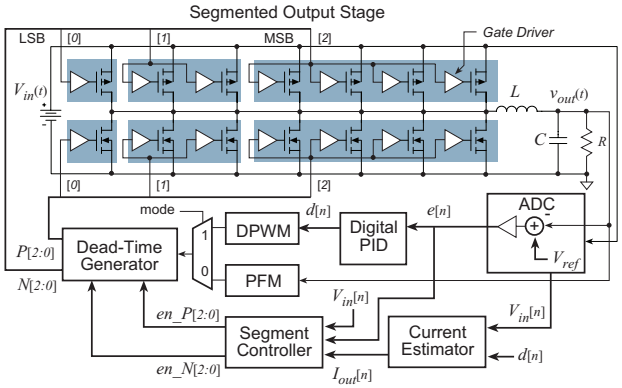
III. Fixed-Frequency Techniques

In numerous applications such as automotive electronic control units (ECUs), operating a dc-dc converter over an unpredictable range of f_s in PFM or BM is usually forbidden due to strict electromagnetic compatibility (EMC) requirements. Several fixed frequency techniques have been proposed to mitigate the gate-drive losses.

A. Segmented Power Stage

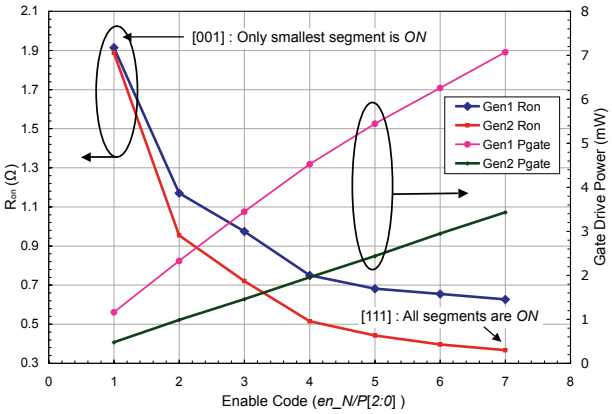
In the first approach [19]–[23], portions of a segmented power stage (SPS) can be turned off at light-load conditions to optimize the trade-off between the effective gate capacitance and R_{on}. The so-called switched-width concept was first proposed by [19] and then subsequently developed by [20]–[23] for practical use and with fine-grained, dynamic segment control.

SPS has a modest overhead compared to a lumped power stage, since the segmentation is easily achieved by separating the gate of power MOSFET cells in the layout, while the drain and source metalization remains unchanged. The measured trade-off between R_{on} and P_{gate} is shown in Fig. 7 for an integrated SPS IC with seven segments connected in a binary weighted fashion. The trade-off between R_{on} and P_{gate} is clearly apparent from Fig. 7. The measured efficiency is shown in Fig. 8. Dynamic control of a SPS was demonstrated on a buck converter using steady-state duty-cycle feedback in voltage-mode control [21], [22], as shown in Fig. 6. Real-time SPS control was also demonstrated by using the digital current-command in CPM [24], [25]. In [23], the SPS concept is used for an integrated boost converter. SPS has even been used within the gate-driver itself. In [26], [27], the effective size and drive-strength of a gate-driver was adjusted for a fixed size power MOSFET. This provides modest efficiency benefits and is more suitable for applications with non-segmented discrete power transistors.



(a)

Fig. 6. Digitally controlled SPS IC with automatic segment selector [21].

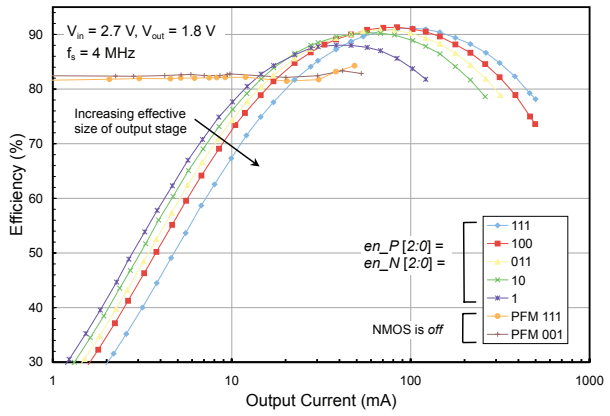


(a)

Fig. 7. Measured trade-off between on-resistance and gate-drive power consumption for on-chip power MOSFETs in two ICs. (Gen1 from [21] and Gen2 from [18]).

B. Adaptive Gate Swing

An alternative approach to SPS is known as adaptive gate swing control (AGS). Unlike SPS, where the gate charge, Q_g, is reduced by leaving portions of the transistor *off* at light-load conditions, AGS modulates the charge by only partially charging the power transistor. Similar to SPS, AGS is used to dynamically exploit the Q_{gate} versus R_{on} trade-off, without needing to segment the power transistor. This is achieved by reducing the drive voltage, V_{dr}, at light loads while increasing the R_{on} as shown in Fig. 9(a) and (b), respectively. In low-voltage CMOS power stages a full-swing driver is usually



(a)

Fig. 8. Measured efficiency for a segmented power stage IC [18].

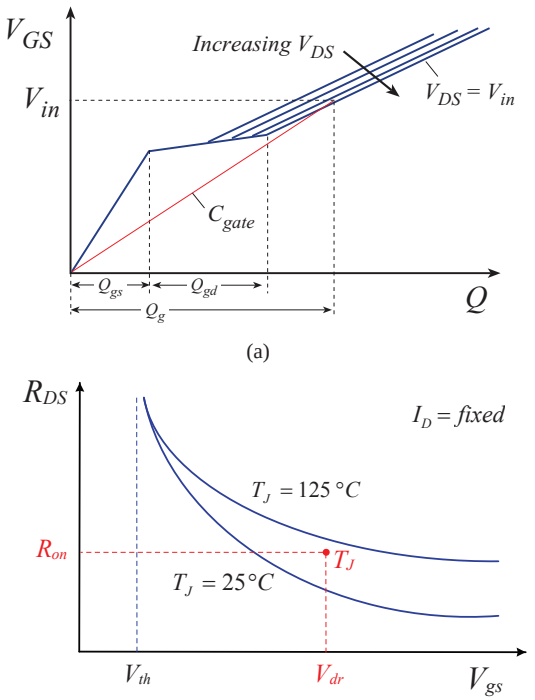
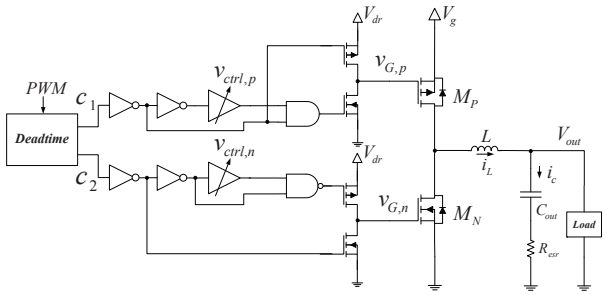


Fig. 9. (a) Typical V_{GS} versus Q_g plot.(b) Typical R_{on} versus V_{GS} plot.



(a)

Fig. 10. AGS implemented with pre-mature termination of the turn-on stage using variable delay blocks [28].

used, where $V_{dr} = V_{in}$. Providing a separate regulated voltage V_{dr} for SPS is not practical due to the large current spikes drawn from the drivers. One practical implementation of APS is shown in Fig. 10 [28], where a programmable timing circuit is used to prematurely terminate the turn-on process. This allows the Q_{gate} of M_P and M_N to be independently controlled using $v_{ctrl,p}$ and $v_{ctrl,n}$, respectively. Unfortunately, this simple and elegant solution raises important reliability concerns, since the gate voltages $v_{G,p}$ and $v_{G,n}$ are left floating after turn-on. In high-reliability applications the power MOSFET gates must be driven by low-impedance paths at all times.

In [29], AGS is demonstrated on an isolated half-bridge converter, and the gate-drive voltage is controlled digitally based on load current sensing. In [30], the self-scaling gate-drive voltage is also based on the load condition. AGS has been implemented in combination with the SPS technique in [24], [25], where the gate-drive supply is generated using a switched-capacitor circuit with discrete voltages. AGS control requires prior knowledge of the MOSFET R_{on} and Q_g characteristics to determine the optimal gate-drive voltage under various load conditions, unless calibration is introduced.

C. Resonant Gate Driver

A third method for reducing P_{gate} involves the use of a resonant circuit in the gate-driver. A conventional CMOS gate driver is shown in Fig. 11(a). Numerous resonant gate drivers (RGD) have been demonstrated, including LC-based RGD, as shown in Fig. 11(b) and (c) [31]–[34], and current source RGD [35]–[38]. The basic waveforms for the RGD approach of Fig. 11(c) is shown in Fig. 12. The current $i_r(t)$ circulates in the resonant inductor and is used to charge and discharge the gate capacitance when both S_1 and S_2 are *off*. The gate charge is therefore returned to the storage capacitance after each switching cycle.

In [39]–[42] the circuit architectures of Fig. 11 are used with coupled inductors to implement gate drivers for both M_P and M_N. These techniques inevitably require a dedicated inductor or a transformer for energy storage.

The RGD concept has been demonstrated to achieve more than 5 % in overall efficiency improvement over a wide load range [34], [36], [39], however most of the existing prototypes are implemented using discrete components and with open-loop control on converters at $f_s < 4$ MHz. Given the low cost of SPS and AGC, using RGD with relatively large off-chip passive components below 10 MHz seems unjustified. In [43], [44], an integrated RGD is designed to operate at 200 MHz, and the gate timing is designed based on the simulated converter parasitics. A reduction of 20 to 30 % in gate-drive loss is observed. Without some form of feedback or calibration, maintaining these benefits over a wide range of process and temperature variations is questionable.

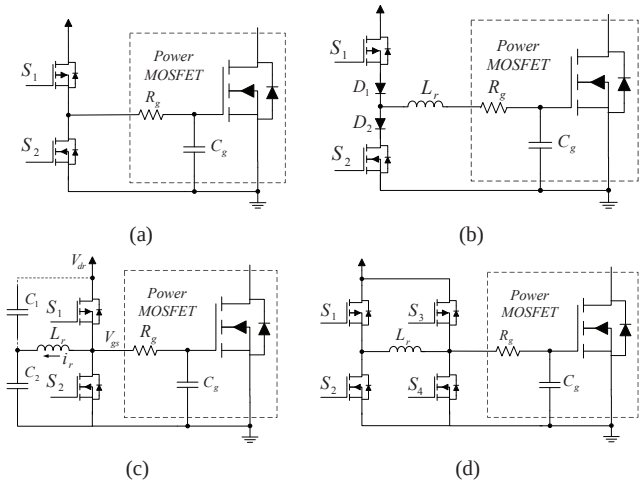


Fig. 11. (a) Conventional CMOS gate driver (b) and (c) LC resonant gate drivers (d) current source resonant gate driver.

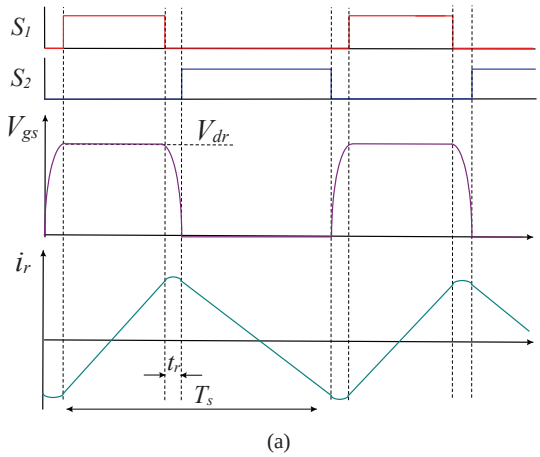


Fig. 12. Switching waveforms of the resonant gate driver in Fig. 11(c) [31].

D. Charge Recycling to Reduce Gate-Drive Losses

Capacitor-based charge recycling (CCR) has been used for power reduction in various digital circuits and energy harvesting systems [45]–[47]. CCR uses the superior energy density of capacitors and does not rely on additional inductors. CCR is therefore more cost-effective then RGD. In one CCR scheme, the gate drivers are stacked such that the charge can directly be transferred from the high-side gate to the low-side gate [7], [48]–[50]. The mid-rail node is either regulated to power other circuit blocks, or connected to the switching node through a diode-connected transistor. Alternatively, a linear regulator can be used to provide a mid-rail voltage as the charge storage node. The implementation of an on-chip, high-bandwidth linear regulator to provide the mid-rail voltage is relatively expensive, since the gate drivers require very high peak currents, as demonstrated in [51]. In [28], a combined gate charge modulation and recycling technique (GCMR) is implemented with a on chip LC tank for a 3 MHz converter with 5 % efficiency improvement at light-load conditions.

CCR involves storing a portion of Q_{gate} in a capacitor during the gate discharge phase, then re-using it during charging phase. The charge from the driver supply is therefore partially recycled. CCR requires an additional capacitor that is at least one order of magnitude larger than the effective gate capacitance of the power MOSFET. A large storage capacitance ensures that the storage tank maintains a constant voltage throughout the charge-sharing phase. Unlike SPS and AGS, CCR reduces P_{gate} without compromising R_{on}, similar to RGD.

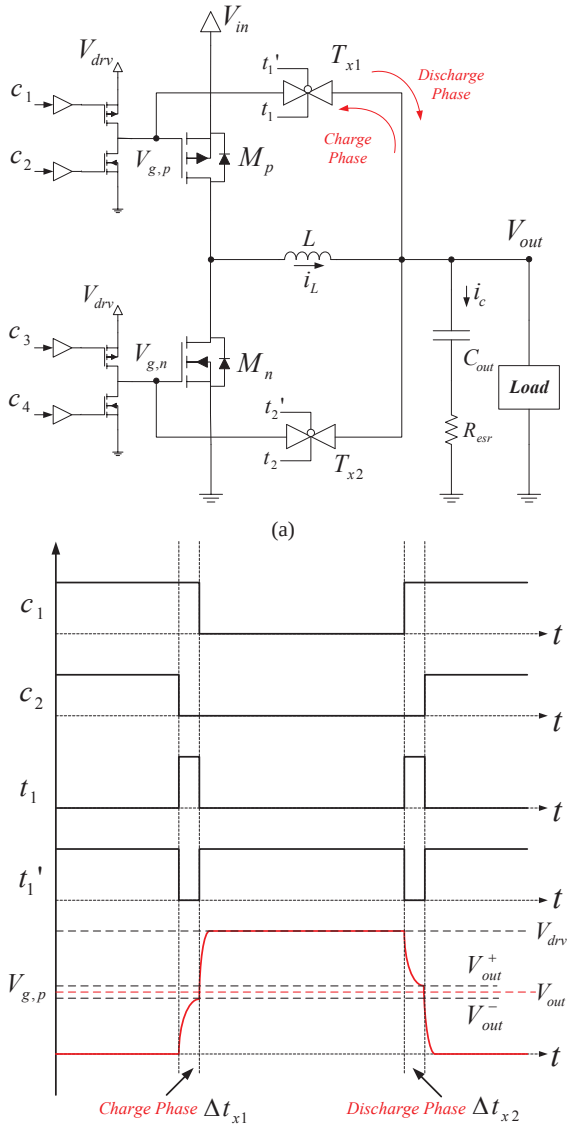


Fig. 13. (a) Simplified CCR architecture and (b) Ideal switching waveforms for the high-side switch [52].

In order to alleviate the need for an additional large on-chip capacitor, [52] proposes to use the existing output capacitor, C_{out}, since V_{out} is precisely regulated. The ideal CCR architecture and ideal gating waveforms are shown in Fig. 13(a) and (b), respectively. The gates of the power MOSFETs M_p and M_n are connected to C_{out} through transmission gates T_{x1} and T_{x2} during charge recycling. The last stage of the gate

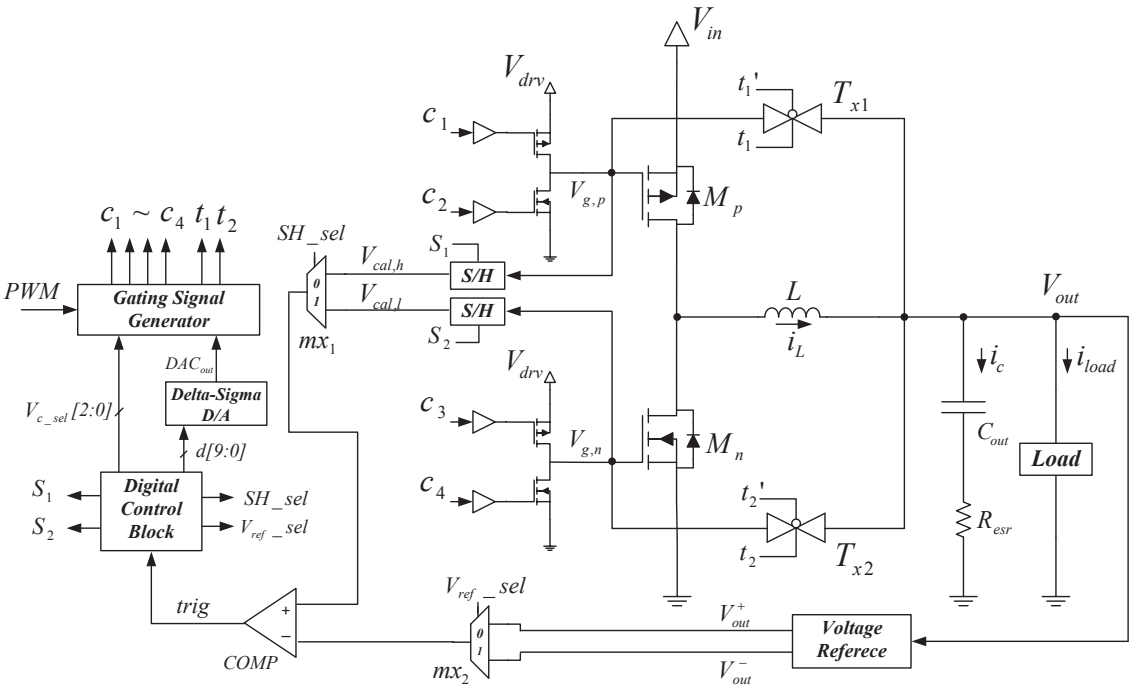


Fig. 14. System architecture of the closed-loop gate-charge recycling timing control [52].

drivers has four separated gating signals, c_1 to c_4, in order to allow the gate to be driven by the transmission gates while it is being charged or discharged through C_{out}. Ideal switching waveforms for M_p and T_{x1} are shown in Fig. 13(b). During the charging phase, $V_{g,p}$ is first charged to V_{out} through T_{x1}, while the driver is left in a high impedance state. Ideally, T_{x1} is turned off precisely when $V_{g,p}$ reaches V_{out}, after which the driver charges $V_{g,p}$ to V_{dr}. A similar procedure applies for the discharging phase. The ideal power savings is 50 % when V_{out} = V_{in}/2, when perfect charge recycling occurs.

Achieving the maximum reduction in P_{gate} requires precise closed-loop control of the timing in the charge recycling circuit of Fig. 13(a) due to process, voltage and temperature (PVT) variations. A closed-loop delay-locking control scheme that is insensitive to the aforementioned delays is proposed in [52], as shown in Fig. 14. As in most calibration schemes, the process only is performed periodically to conserve power. A 20 MHz synchronous buck converter is designed and simulated with voltage mode control at fixed input voltage of 2.5 V, and the converter efficiency is plotted for output voltages at 0.8, 1.2 and 1.6V from 15 mA to 180 mA, as shown Fig. 15. The charge recycling technique exhibits from 3 to 5 % efficiency improvements up to 100 mA. In Fig. 16, the power savings at every output voltage is separated into driver and input power savings. A savings of 25 % in P_{gate} is observed across all loads.

IV. Comparison and Discussion

The seven light-load efficiency optimization techniques covered in this work are contrasted in Table II. It is certainly possible to combine two or more techniques in a single IC.

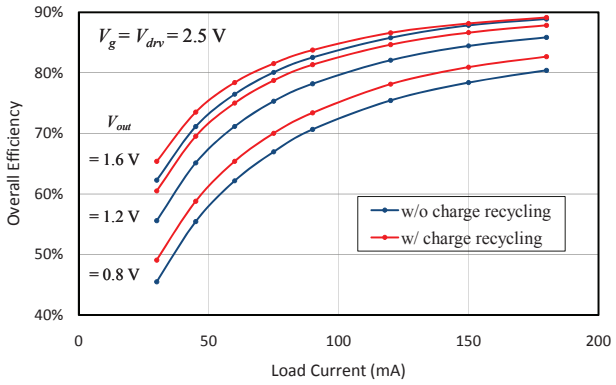
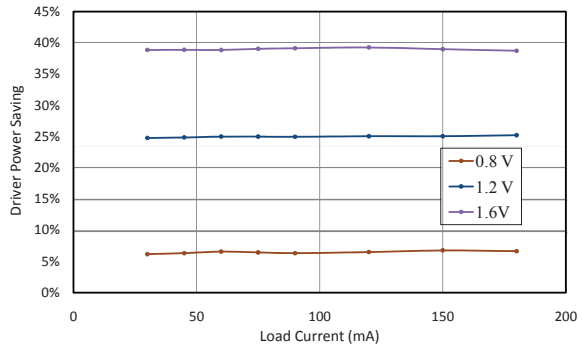


Fig. 15. Simulated efficiency improvements at V_{out} = 0.8, 1.2 and 1.6 V [52].

SPS and AGS can be combined by using the technique shown in Fig. 10 with a segmented power stage. On the other hand, certain combinations are inherently incompatible, such as CCR and RGD, while others are simply variants such as PFM, PFM-AOT and BM. Deciding which technique to implement is non-trivial, since it depends on the EMI requirements, the device performance, space and cost constraints. The literature contains a vast array of experimental work on these techniques, covering a wide range of frequency and power levels. Variable frequency techniques such as PFM, PFM-AOT and BM provide the largest efficiency benefit, however they are not suitable at full load and therefore automatic mode-switching is required. In general, PFM and SPS are the simplest to implement with low-power controllers and they provide a good cost/benefit trade-off. CCR is also attractive but requires



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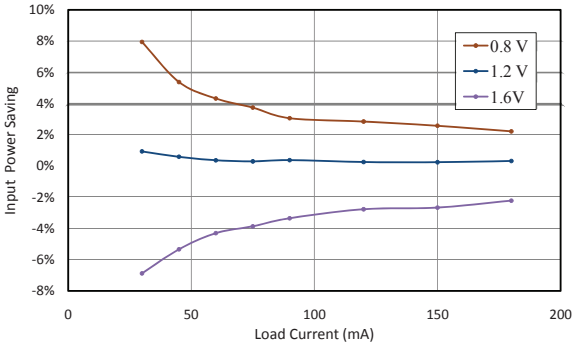

(b)

Fig. 16. (a) Simulated driver power saving and (b) input power saving, comparison at different V_{out} [52].

calibration. RGD is more suitable either at very high frequency where an on-chip resonant inductor can be used, or at high power levels with large discrete power transistors.

TABLE II
EFFICIENCY OPTIMIZATION TECHNIQUES COMPARISON

	PFM	PFM AOT	BM	AGS	SPS	RGD	CCR
Section	II-A	II-A	II-B	III-A	III-B	III-C	III-D
Requires Additional L	N	N	N	N	N	Y	N
Requires Additional C	N	N	N	N	N	Y/N	Y/N
Suitable for Discrete Power-stage	Y	Y	Y	Y	N	Y	Y
Trade-off Between $Q_{gate}R_{on}$	N	N	N	Y	Y	N	N
Gate Charge Recovered	N	N	N	N	N	Y	Y
Variable Frequency EMI Issues	Y	Y	Y	N	N	N	N
Used Over Full Load Range	N	N	N	Y	Y	Y	Y

V. CONCLUSION

Maintaining high efficiency at light-load conditions is extremely important in most modern power management applications. The most popular light-load efficiency optimization techniques are outlined in this work, namely pulse-frequency modulation, burst-mode control, adaptive gate swing, segmented power-stage, resonant gate drivers and capacitive charge recovery. These techniques offer varying levels of efficiency improvements and the cost/benefit trade-offs must be carefully weighed for each application.

ACKNOWLEDGMENT

The authors are grateful for the support of the Canadian Microelectronics Corporation (CMC), the Natural Sciences and Engineering Research Council of Canada (NSERC), the Canadian Foundation for Innovation (CFI) and the Ontario Research Fund (ORF).

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