Precision Gate Drive Timing in a Zero-Voltage-Switching DC-DC Converter

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***Abstract*— This paper presents the design and implementation of an integrated low-voltage power conversion controller capable of delivering MOSFET gate-drive signals to on-chip power transistors with precision timing. Analog Dead-Time-Locked-Loops (DTLL) are used to realize an accurate analog dead-time controller with fast error rejection in a fixed frequency Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) buck converter.**

I. Introduction

The next-generation VLSI chips will require point-of-load DC-DC switch-mode converter modules capable of providing tightly regulated sub-1V supply voltages, high currents up to several hundred amps under extreme load transients (di/dt of thousands of A/µs). The most popular solution for such applications is the multi-phase interleaved buck converter.

Stringent future demands on transient response and power density will push the switching frequency, f_s, beyond several MHz. A higher f_s allows wider control bandwidth, shorter modulation delay and reduced output inductance L, yielding higher current slew rate during load transients. The interconnect parasitics between the Voltage Regulation Module (VRM) and VLSI package are significant contributors to supply voltage fluctuations. It will eventually be necessary to integrate power management chips, passive components and the target VLSI circuit within a single package. Promising hybrid-packages are emerging, including the Multi Dimensional Die-Integration System Chip (MDSC) architecture of Fig. 1. Clearly, pushing f_s beyond several MHz for passive component miniaturization is a prerequisite for these future packaging solutions.

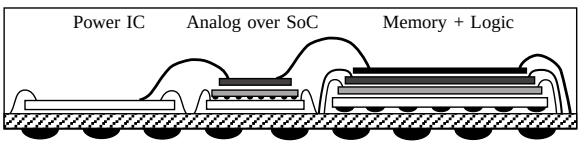

Fig. 1. Representation of Multi Dimensional Die-Integration System Chip [1].

Unfortunately, increasing f_s will incur higher losses, such as the gate-drive loss and, in particular, the switching losses in conventional hard-switched synchronous Buck converters [2]:

$$P_{sw} = P_{turn-on} + P_{turn-off} \approx 2(C_p(V_{in}^2 + V_{in}I_{out}t_r)f_s \quad (1)$$

where $P_{turn-on}$ is due to the charging of the parasitic capacitance C_p at the junction of the power switches during turn-on (see Fig. 2), and $P_{turn-off}$ is due to the overlapping of the V and I waveforms during turn-off.

Maintaining high efficiency at such high f_s is a major challenge. Soft-switching techniques can minimize noise and switching losses. Zero-Voltage-Switching (ZVS) is ideal for low-voltage MOSFET based converters, since capacitive loss can be virtually elliminated.

II. Zero-Voltage-Switching Quasi-Square-Wave Converter

A. Topology

Consider the MOSFET-based synchronous buck topology, as shown in Fig. 2. If L is reduced below L_{crit} given by Eq. (2), the inductor current will flow in both forward and reverse direction, thus discontinuous-conduction mode is avoided. The reversed inductor current following low-side turn-off charges up the parasitic capacitance at node X in lossless resonance, thus $P_{turn-on}$ in Eq. (1) is eliminated [3]. Similarly, a lossless discharge occurs during the dead-time, T_2 due to the positive inductor current. The dead-times, T_1 and T_2 must be controlled in real-time in order to achieve the ideal zero-voltage-switching transitions of Fig. 2(b). A true ZVS-QSW converter minimizes switching and body diode losses and lowers the EMI due to the reduced dV_x/dt, without increasing the power stage complexity. Further details concerning the ZVS-QSW topology are given in [4] [5].

$$L_{crit} = (1 - \frac{V_o}{V_{i(min)}}) \cdot \frac{R_{(min)}}{2f_s} \quad (2)$$

B. Dead-Time Control Strategies and Requirements

The ideal dead time delays T_1 and T_2 in Fig. 2 are determined by the resonant switching durations due to the charging and discharging of C_p by the valley and peak inductor

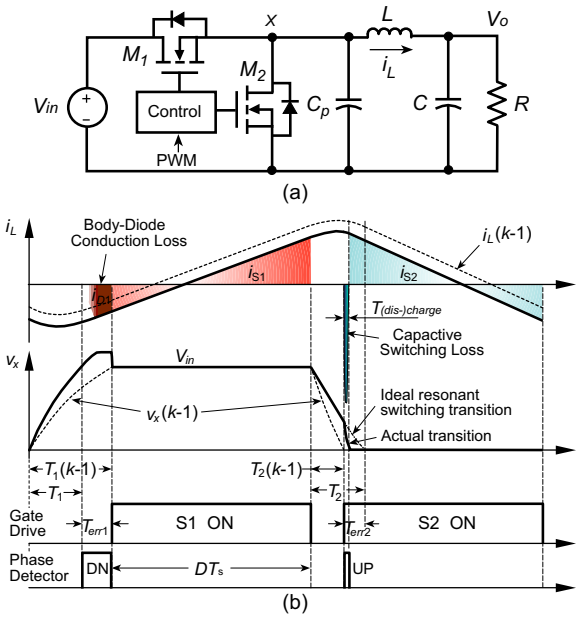

Fig. 2. (a) ZVS-QSW buck converter. (b) Load transient leads to dead-time errors and switching loss. The period *k-1* has ideal dead-times.

currents, respectively. In turn, T_1 and T_2 are directly affected by the RMS output current. The ideal dead-times alternate between their respective maximum and minimum durations over the full range of load conditions..

A converter designed with fixed delays inevitably suffers from body-diode conduction losses when the delay is longer than ideal, or capacitive losses when the delay is shorter than ideal. These losses, which occur every switching cycle, are unavoidable since fixed dead-times cannot be optimized for all load conditions.

The simplest solution is an adaptive scheme in which the gate-drive is asserted after detecting the zero-voltage crossing [6]. This is not suitable in high-frequency applications where comparator and gate-drive delays ($\leq$20ns) lead to severe positive dead-time errors.

An alternative approach proposed by [7] uses an opamp assisted V/I converter for the adaptive delay generator. The design assumes that the V_x transition is linear, therefore the $V_{in}/2$ crossing occurs at the middle of the ideal dead-time. This is used to assert the gate drive before the actual zero-voltage crossing. The main drawback is that the transition is not exactly linear and therefore external trimming is required to eliminate timing errors.

A "predictive" scheme based on a digital Delay-Locked-Loop (DLL) was proposed using a D-flip-flop phase detector and a digital delay line to track the ideal dead-time [8]. This robust scheme has relatively poor transient performance, requiring numerous switching cycles to reach steady state. Moreover, even at steady state, the dead-time swings sub-harmonically around the ideal value due to the nature of it's nonlinear ("bang-bang") phase detector and the fixed delay step. There is an inherent tradeoff between the steady-state dead-time accuracy and the settling speed of the DLL since the delay can only be incremented by one step per switching cycle. Therefore, the incremental digital delay cannot be reduced arbitrarily since the losses incurred with a slow DLL settling time can be prohibitive. This drawback renders this scheme unsuitable for applications with frequent load variations such as microprocessors.

This paper proposes a design that employs analog Delay-Time-Locked-Loops (DTTL) to allow quick and accurate adjustments of the dead-times [7]. Comparators that sense the power MOSFETS' v_{DS} zero-voltage crossing (Comp_{VDS}) and v_{GS} threshold-voltage crossing (Comp_{VGS}) are followed by a phase detector as shown in Fig. 3. The phase detector provides up and down pulses for the charge pump. The charge pump outputs the delay control voltage V_{ctrl} that linearly determines the dead-time delay, which completes the negative feedback loop.

To maintain high-efficiency during load variations, it is desirable for the DTLLs to reach steady-state within at most several switching cycles. The gain of the DTLL can be expressed as:

$$|G| = \frac{I_{CP}}{I_{DL}} \cdot \frac{C_{DL}}{C_{CP}} < 1 \tag{3}$$

$|G|$ must be chosen to be sufficiently large to obtain fast tracking without leading to instability in this discrete-time DTLL system with a fixed one-cycle delay. In the linear delay generator as shown in Fig. 3(a), the PWM signal rapidly discharges C_{dl}, which is then linearly charged by I_{dl} until it reaches the buffered V_{ctrl}. The PWM signal is therefore delayed by $t_d = V_{ctrl} \cdot C_{dl}/I_{dl}$.

For negative dead-time errors the resonant transition is not completed and C_p is charged/discharged almost instantaneoulsy, resulting in an UP pulse generated by the phase detector (approximately $T_{(dis)charge}$), which is much shorter than the actual error T_{err}. This leads to poor tracking since the short UP pulse does not sufficiently correct the dead-time. The problem is solved by inserting a One-Shot block, which linearly extends the UP pulses that exceed a minimum threshold length (Fig. 4). Pulses narrower than the threshold are fed to the charge-pump, unaffected by the one-shot block. The value of this threshold can be digitally adjusted.

The references for the Comp_{VGS} in the high and low-side DTLLs are the threshold voltages of the *p* and *n*-channel MOSFETs, respectively. They are generated internally using dedicated circuits. The inputs of the comparator Comp_{VDS} are connected across the power transistors. To account for the small forward voltage drop of the power devices, a digitally trimmed offset is introduced to each comparator.

The offset introduced into the comparator, Comp_{VDS} in Fig. 3(a) causes the phase detector DN pulse to be slightly extended by t_{offset} beyond the ideal dead-time error (T_{err1} in Fig. 2(b) with respect to the ideal dead time T_1). If such DN pulses were fed directly into the charge pump, the DTLL's loop gain would be increased for small dead-time errors, possibly resulting in instability. A Down Pulse One-Shot block similar

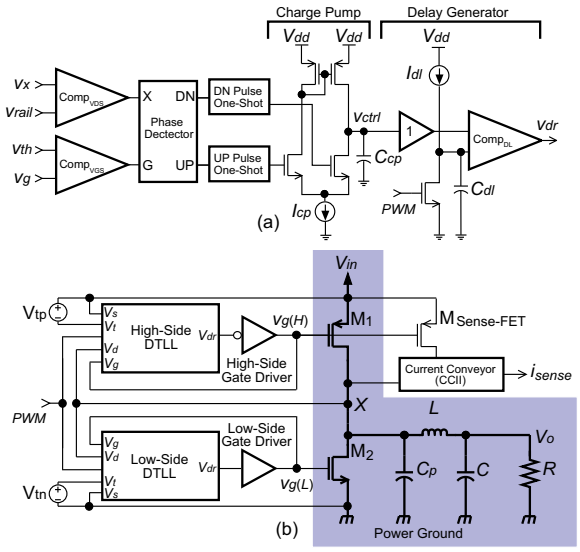

Fig. 3. (a) ZVS-QSW buck converter with Dead-Time-Locked-Loops. (b) Circuits inside one of the DTLL blocks.

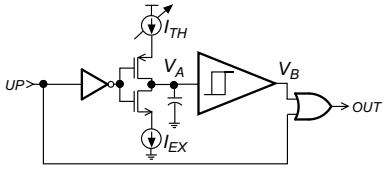

Fig. 4. Up One-Shot Block.

to the Up Pulse One-Shot block is inserted to shorten the DN pulses, creating a desirable control dead-zone. This dead-zone ensures that the DTLL loop gain is effectively reduced for small dead-time errors, yet largely unaffected for large errors.

The design also includes a senseFET based current sensing structure as shown in Fig. 3(b). The i_{sense} current is fed into an external resistor. The resulting voltage can be used as a current feedback in a high-bandwidth PWM controller.

III. Simulation Results

The HSpice transient simulation result for the current-mode controlled ZVS-QSW buck converter system under a dynamic load with large transient variations is shown in Fig. 5. The adjustment of V_{ctrl} in both DTLLs follows the inductor current rapidly. Therefore, the dead-time errors are essentially eliminated in two switching cycles. After several cycles, the dead-times reach steady state and the V_x waveform exhibits ideal ZVS resonant transitions similar to Fig. 2(b). The simulated loss distributions for the DTLL design compared to fixed 10ns dead-times are as shown in Fig. 6. Results are presented for rated (10A), light (1.5A) and dynamic loads (10kHz repetition). The DTLL circuitry clearly eliminates switching losses under constant and dynamic loads, maintaining high efficiency. The DTLL advantage is even more promising as f_s scales to 4MHz, where $\eta = 93\%$.

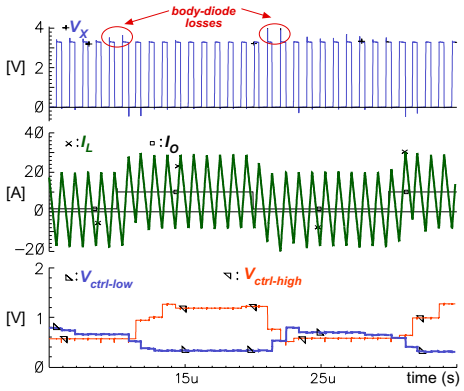

Fig. 5. Transent waveforms of ZVS-QSW buck converter with DTLLs under a dynamic load (1.5A-10A).

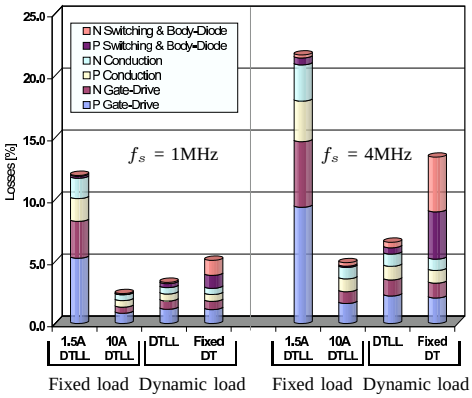

Fig. 6. On-Chip losses with DTLL/fixed dead time. V_o=1.3V, devices optimized @10A, for 1 and 4MHz.

IV. Silicon Implementation

A ZVS-QSW controller chip was implemented in TSMC's 0.18µm CMOS process (Fig. 8) to demonstrate the DTLL concept. The block diagram of this controller chip is as shown in Fig. 7. In addition to realizing the circuit blocks depicted in Fig. 3(b), this chip also includes an 8-bit digital delay line for comparison purposes and a digital RAM file containing calibration data. Various DTLL parameters such as the Comp_{VDS} offsets and the one-shot thresholds can be digitally trimmed. Both DTLL blocks can generate delays up to 50ns. The scaled-down power stage has a nominal output of 0.2A with $V_{in} = 2$V and 0.5V$< V_o <$1.4V. Using the digital delay line to generate longer than ideal dead-times, body-diode conduction is evident,as shown in Fig. 9. Fig. 10 shows properly regulated dead-times for f_s=5MHz. The benefit of the dead-time error rejection and true soft-switching is verified by the measured efficiency of the ZVS-QSW converter with different inductor sizes (see Fig. 11). A peak efficiency of 82% is achieved at 5MHz. The efficiency of above 75% is maintained until the conduction losses of the MOSFET switches start to dominate. The efficiency would be greatly improved with optimized power MOSFETs, which are unavailable in the low voltage process.

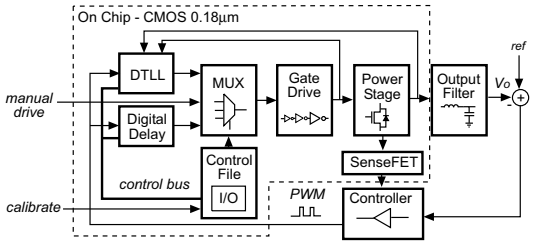

Fig. 7. Block diagram of the ZVS-QSW buck converter with integrated DTLLs.

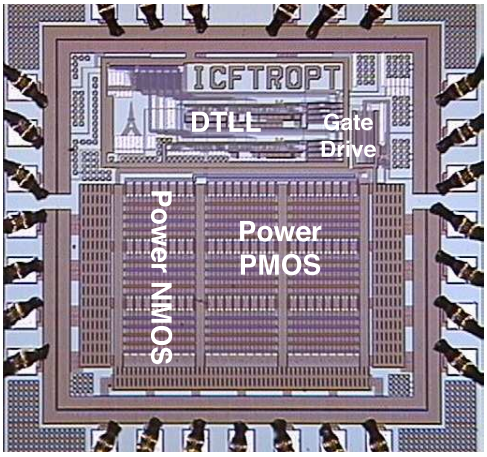

Fig. 8. A micrograph of the 0.18um CMOS 1.56mm^2 integrated ZVS-QSW DC-DC convreter chip.

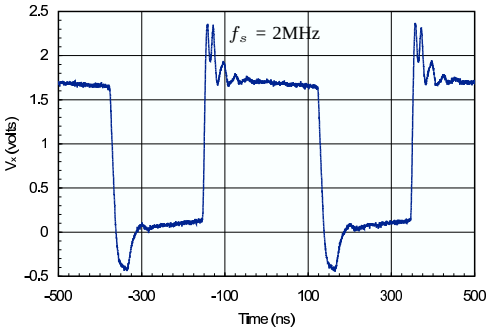

Fig. 9. Measured voltage waveform at node X of the ZVS-QSW converter. Body-diode losses occur due to the shorter than ideal dead-time.

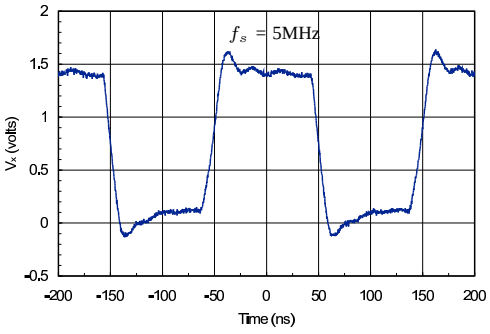

Fig. 10. Measured voltage waveform at node X of the ZVS-QSW converter. Proper gate-drive timing eliminates body-diode conduction after resonant transitions.

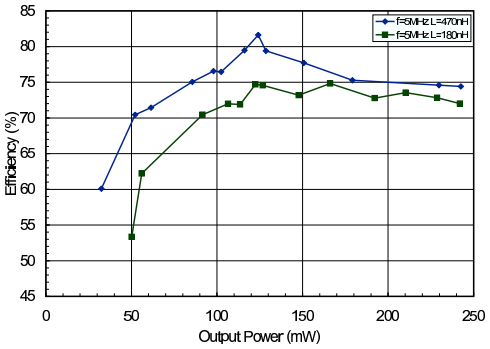

Fig. 11. Measured efficiency of the ZVS-QSW converter for V_{in}=2V, V_o=1.4V.

TABLE I

ZVS-QSW CHIP SPECIFICATIONS

Technology	0.18µm Mixed-Signal CMOS
Supply voltage	2V
Nominal output voltage	1V
Maximum dead-time	50ns
High-Side R_{ds-on}	0.4 Ω
Low-Side R_{ds-on}	0.4 Ω
Die area	1.56mm^2
DTLL power consumption	4.5mW

V. CONCLUSIONS

Conventional DC-DC topologies used to power modern VLSI circuits cannot satisfy future demands for shrinking voltages, rising frequencies, tighter regulation and high efficiency. Zero-Voltage-Switching can be applied to the Quasi-Square-Wave buck converter to eliminate switching losses, as long as the dead-times are adjusted in real-time to track load changes. This work demonstrates the feasibility of analog Dead-Time-Locked-Loops in a low voltage application for achieving fast dead-time error rejection and low steady-state switching losses.

VI. ACKNOWLDEGEMENTS

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