A Quasi-Resonant Bi-directional Tri-Mode DC-DC Converter with Limited Valley Current

Mazhar Moshirvaziri, Chuanwei Li, Olivier Trescases
University of Toronto, Department of Electrical and Computer Engineering
10 King's College Road, Toronto, ON, M5S 3G4, Canada

***Abstract*— This work targets non-isolated, bi-directional dc-dc converters for hybrid energy-storage systems in light electric vehicles. Three operating modes are used to achieve high-efficiency over the full load range based on the inductor current constraints. The highest switching frequency is used near the rated current in order to limit the peak inductor current and avoid saturation. Soft-switching ZVS turn-on is achieved on both transistors in the mid-load range, where the frequency is automatically controlled to maintain a fixed dead-time and near-constant negative inductor valley-current. Pulse-frequency-modulation is used at light-load conditions for improved efficiency. A 2 kW two-phase bi-directional dc-dc converter prototype was implemented to demonstrate the tri-mode operation. The converter operates with an input voltage of 50 V and an output voltage of 100 V. Using the proposed tri-mode control scheme, a peak efficiency of 97.5% is achieved while a minimum efficiency of 88% is maintained over the full load range.**

I. Introduction

The main focus of this work is efficiency optimization in high-frequency dc-dc converters. The target application is Hybrid Energy-Storage Systems (HESS) for Light Electric Vehicles (LEVs), as shown in Fig. 1(a). As Lithium-Ion (Li-Ion) batteries become more affordable, there is a growing number of LEV applications, including electric bicycles, scooters, motorcycles, small utility vehicles and personal mobility devices. The HESS contains both a Li-Ion battery pack for high-energy density and an ultracapacitor (u-cap) module for high power-density [1]. The two energy sources are interfaced to the bus voltage, V_{bus}, using two bi-directional, non-isolated dc-dc converters. A current-command, $I_{bt}*$, is periodically generated by the system power optimizer with an update rate of 1-10 Hz in the targeted LEV application, based on the convergence time of the optimization algorithm [2]. The current-command, $I_{bt}*$, is calculated based on the dynamic load requirements, and the battery/u-cap state-of-charge (SOC). The u-cap converter directly regulates V_{bus} using a standard voltage control loop. The system-level power optimizer is used to off-load the large load-transients from the battery to the u-cap, which has a lower Equivalent Series Resistance (ESR) and a higher cycle-life. The detailed operation of the power optimizer [1]–[4] is beyond the scope of this paper, which deals exclusively with the bi-directional dc-dc converter that interfaces the battery to V_{bus}, as shown in Fig. 1(b). The converter operates with digital average current-mode control. The capacitance C_x represents the lumped parasitic capacitance at v_x. While several isolated and non-isolated topologies have been proposed for high-power EV applications [5], [6], the boost topology was chosen due to its low cost and high efficiency, especially when operated with soft-switching.

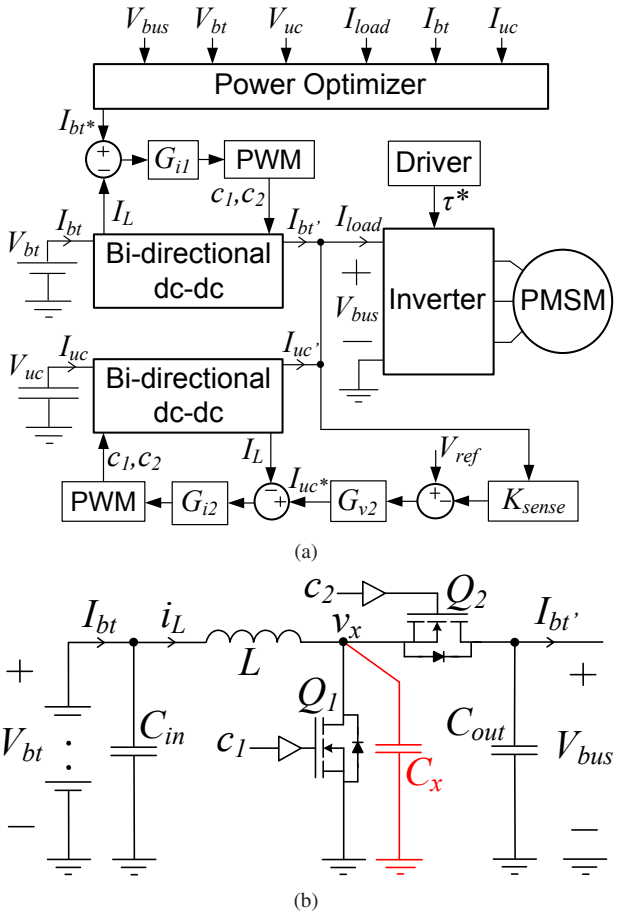


Fig. 1. (a) Architecture of a hybrid energy-storage system. (b) Synchronous boost converter used for interfacing the storage devices to V_{bus}.

Operating the converter in Fig. 1(b) with a negative inductor valley-current, I_v, allows zero-voltage-switching (ZVS) turn-on to be achieved in both switches due to the resonant transitions of $v_x(t)$ during the dead-times t_{d1} and t_{d2}, as shown in Fig. 2(a). Optimizing the dead-times, and hence eliminating the turn-on losses, for a range of load currents and battery voltages is essential for achieving higher efficiency. The main challenge in dead-time optimization is the precise timing of gate-drive signals to achieve ZVS in the presence of load changes, uncertainty in the parasitic components and gate-driver delays [7]. Dead-time optimization in high-frequency,

non-isolated converters has been extensively studied, with various analog and digital on-line calibration schemes for fixed-frequency operation. Analog dead-time calibration based on a delay-locked-loop (DLL) has been carried out in [8] while [9], [10] have utilized a current starved charge pump. A digital sensorless dead-time optimization has been introduced in [11] which has a simple implementation but suffers from a limited reaction speed during load transients. Another digital adaptive dead-time optimization based on efficiency is introduced in [12]. A digital single-step dead-time correction has been reported in [13] and an observer based method has been done in [14]. Digital dead-time optimization for a multi-phase dc-dc converter based on the current sharing of the phases has been introduced in [15]. All these works demonstrate dead-time calibration based on a fixed-frequency operation.

In this work, a novel approach to multi-mode quasi-resonant operation is demonstrated for the targeted LEV application. Consider the constraints on $i_L(t)$ shown in Fig. 2(b). The second quadrant operation, where $i_L(t) < 0$, is not shown for clarity. The converter must maintain the constraint given by

$$i_L(t) < I_{L,sat} - \Delta I_m \tag{1}$$

under all conditions, where $I_{L,sat}$ is the inductor saturation current and ΔI_m is the safety margin required for dynamic excursions and sensing errors. In this HESS application, ΔI_m can be minimized since the battery current-command, $I_{bt}*$, is tightly controlled and is only periodically updated by the system power optimizer. Moreover, large dynamic load currents are off-loaded to the u-cap converter. This also helps to alleviate the potential electromagnetic interference (EMI) issues associated with operating the battery-connected dc-dc converter at variable frequency.

II. Mode Description and Control Strategy

Operating with $I_v < 0$ is required to achieve ZVS turn-on in both switches, which is referred to as dual-ZVS. Achieving dual-ZVS turn-on is unpractical at the full-load condition due to the large peak current, I_p, which requires an inductor with a very high saturation current, leading to prohibitive cost. Operating with a large inductor current ripple, ΔI_L, in the full-load condition increases the conduction losses, P_{cond}, given by

$$P_{cond} = \left(I_L^2 + \frac{\Delta I_L^2}{3}\right)(R_L + R_{on}) + I_L^2 R_{bt} + \frac{\Delta I_L^2}{3} R_{C_{in}} + \left(\left((I_L - I_{Load})^2 + \frac{\Delta I_L^2}{3}\right) D' + D I_{Load}^2\right) R_{C_{out}} \tag{2}$$

assuming $R_{C_{in}} << R_{bt}$, where D is the steady-state duty-cycle and R_{bt}, R_L, $R_{C_{in}}$, $R_{C_{out}}$ are the equivalent series resistance (ESR) of the battery, inductor, input capacitor and output capacitor, respectively. I_L and I_{Load} are the average inductor and load current while $\Delta I_L = I_L - I_v$. Assuming a switching-frequency of f_s and $t_{d1,2} << T_s$, the converter can operate in dual-ZVS mode for I_L given by (3), where I_v is given by (4).

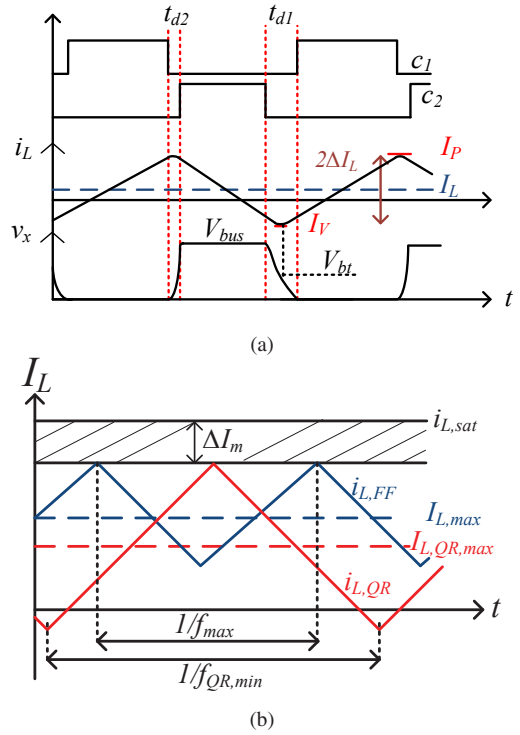


Fig. 2. (a) Ideal waveforms for ZVS operation. The optimal t_{d1} and t_{d2} depend on I_V and I_P respectively. (b) Inductor current constraints.

$$I_L < I_{crit} = \frac{I_{L,sat} - \Delta I_m + I_v}{2} \tag{3}$$

$$I_v \approx -\frac{C_x V_{bus}}{t_{d2}} \tag{4}$$

In this work, a tri-mode control scheme with variable switching frequency in the mid-load range is proposed for achieving a high efficiency over the full load range, while meeting the constraints of Fig. 2(b) and limiting the peak-to-peak inductor current. The chosen switching frequency and dead-time control strategy is illustrated in Fig. 3.

A. Mode Description

The three operating modes are described in order of decreasing I_L:

1. **Fixed-frequency Mode (FF)**:
   In this mode $I_{L,QR,max} < |I_L| < I_{L,max}$. The converter operates at the maximum frequency, $f_s = f_{max}$, which is the minimum operating frequency such that $|i_L(t)| < I_{sat} - \Delta I_m$. In this mode, t_{d2} is controlled to achieve ZVS turn-on in Q_2. The transistor Q_1 experiences hard-switching since $I_v > 0$ and t_{d1} is minimized to avoid cross-conduction. Operating with a fixed f_s at heavy-load conditions reduces the potential for EMI problems. At this switching frequency, core losses as well as the eddy current losses become quite significant in the inductor.

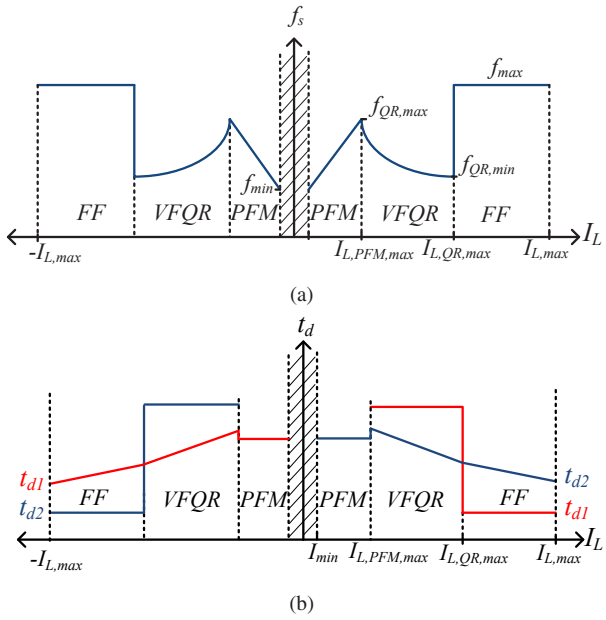


Fig. 3. (a) Switching frequency variation and (b) dead-time control strategy for different operating modes.

2. **Variable Frequency Quasi-Resonant Mode (VFQR)**: In this mode $I_{PFM,max} < |I_L| < I_{QR,max}$. At $I_{QR,max}$, the frequency is reduced from f_{max} to $f_{QR,min}$ such that $I_p = I_{sat} - \Delta I_m$ and the valley current, $I_v = I_{vr}$, provides sufficient charge to discharge v_x from V_{bus} to 0, in order to achieve ZVS turn-on in Q_1. The waveform of $i_L(t)$ at the edge of VFQR mode is shown in Fig. 2(b). In VFQR mode, f_s is controlled such that a fixed dead-time t_{d1} and a near-constant I_{vr} are maintained as the battery current changes. The dead-time t_{d2} is also adjusted such that dual-ZVS turn-on is achieved. Increasing f_s while reducing I_L is non-conventional, however in the absence of turn-on losses, it helps to maintain a near constant I_v that has several important advantages in this operating mode. 1) At light-loads, for the same I_L, higher f_s reduces the valley current and therefore prevents large negative currents into C_{in}, 2) it reduces ΔI_L and P_{cond} at light-loads and 3) the constant dead-time is much easier to control in order to achieve ZVS over a wide current range. In this mode, since $I_L(R_{bt} + R_L + R_{on}) << V_{bt}$, $f_s \propto 1/I_L$ as given by (5), where D is given by (6).

$$f_s = \frac{V_{bt} D}{2L(I_L - I_v)} \quad (5)$$

$$D \approx 1 - \frac{V_{bt} - I_L(R_{bt} + R_L + R_{on})}{V_{bus}}. \quad (6)$$

3. **Pulse-Frequency Modulation (PFM)**: In this mode $I_{min} < |I_L| < I_{PFM,max}$. The converter operates in a fixed on-time PFM mode, as in [16]–[18]. Constant on-time is applied to Q_1 while Q_2 is controlled to avoid body-diode conduction as $i_L(t)$ decays to 0. Operating in PFM results in higher efficiency below $I_{PFM,max}$, where the gate-drive losses, P_{dr}, and controller losses, P_{cont}, become significant. It can be shown that $f_s \propto I_L$ in PFM mode [17], [18]. The region $|I_L| < I_{min}$ is avoided by the system power optimizer. The limit I_{min} is selected such that $f_{min} > 20$ kHz lies outside of the audible band. Further efficiency improvements can be achieved using adaptive on-time PFM or burst-mode.

The above mode descriptions apply only to the first quadrant, where $I_L > 0$. In the second quadrant, the control strategy is identical, while Q_1, Q_2, t_{d1} and t_{d2} have opposite roles, as demonstrated in Section III. In the second quadrant the following changes should be made: 1) In FF mode, t_{d1} will be controlled to achieve ZVS turn-on in Q_1, while Q_2 experiences hard-switching. 2) In VFQR mode, t_{d2} is constant, while t_{d1} and f_s are adjusted to achieve dual-ZVS turn-on, resulting in a near-constant I_p. 3) In PFM mode, the fixed on-time is applied to Q_2 and diode emulation is achieved using Q_1.

B. Closed-Loop Control

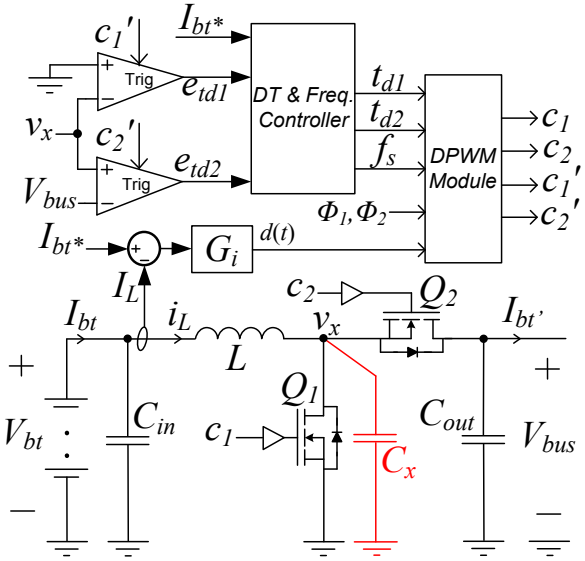
As outlined in Section I, $I_{bt}*$ is periodically calculated in the system power optimizer. Once a current command has been received by the dc-dc converter, the mode is selected based on the pre-defined mode limits, as defined Fig. 3(a).

The digital controller architecture is shown in Fig. 4(a). Two auxiliary PWM signals, c_1' and c_2', are generated by the controller and delayed from the main PWM signals, c_1 and c_2, by ϕ_1 and ϕ_2, respectively. The auxiliary PWM signals are used to trigger the high-speed latched comparators that are sampled to detect the ZVS condition on both transistors. The delays ϕ_1 and ϕ_2 are programmed such that c_1' and c_2' are in phase with the actual V_{gs} crossing of V_{th} for Q_1 and Q_2, as shown in Fig. 4(b). For improved accuracy, ϕ_1 and ϕ_2 can even be programmed to vary with $I_{bt}*$ in order to account for the current dependency of the gate-driver delays. The output of the comparators can thus be monitored to automatically control t_{d2} in first quadrant, t_{d1} in second quadrant operation, as well as f_s for ZVS operation.

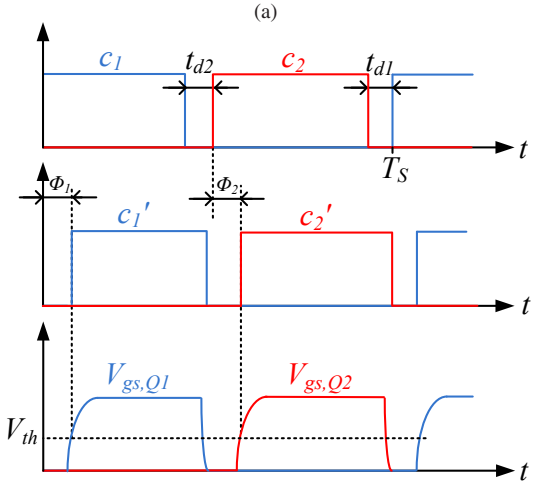
The pre-calculated frequency and the dead-times are fed forward to the controller as the current command is updated. These approximate values may not be optimal for achieving dual ZVS turn-on due to the parameter variations and uncertainties. Automatic adjustment is therefore necessary to achieve the optimal efficiency under a wide range of conditions. In order to avoid the dead-time and frequency adjustments interfering with the current-loop, the fine-tuning of the dead-time and switching frequency is initiated when the current-loop has reached steady-state, based on the internal digital error signal in the current-loop, $e[n]$. Automatic calibration of the dead-time and switching frequency is done using a binary search algorithm around the calculated feed-forward values, based on the comparators outputs.

III. Experimental Results

A 2 kW prototype of the tri-mode bi-directional dc-dc converter was fabricated to demonstrate closed-loop operation, as shown in Fig. 5. While the fabricated boost converter has



(a)



(b)

Fig. 4. (a) Simplified architecture of the VFQR controller. (b) Signal timing in VFQR mode.

two symmetric phases, the experimental results are reported for a single-phase operation for simplicity. The frequency and dead-time control strategy can easily be extended to multi-phase operation. The nominal converter parameters are listed in Table. I.

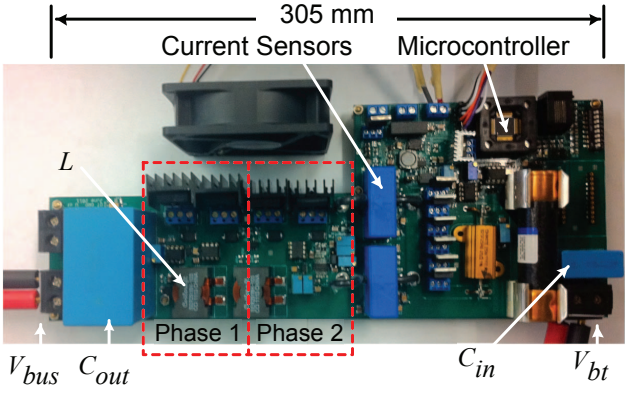


Fig. 5. Fabricated 2 kW quasi-resonant tri-mode converter prototype.

A 16-bit microcontroller (dsPIC33FJ64GS606) is used to implement the digital average current-mode control (ACMC) scheme. This specialized microcontroller has a 1.04 ns resolution for adjusting the switching period, duty-cycle and dead-time.

TABLE I
EXPERIMENTAL SYSTEM PARAMETERS

System Parameter	Value	Unit
Bus Voltage, V_{bus}	100	V
Battery Voltage, V_{bt}	50	V
Max. Switching Frequency, f_{max}	400	kHz
Converter Parameter (Each Phase)		
Max. Power, P_{max}	1	kW
Saturation Current, $I_{L,sat}$	29	A
Current Margin, ΔI_m	5	A
Max. Current, $I_{L,max}$	20	A
Min. Current, $I_{L,min}$	0.4	A
Inductors, L	10	μH
Inductor ESR, R_L	2.7	mΩ
MOSFET on-resistance, R_{on}	5.9	mΩ
Estimated Parasitic Capacitance, C_x	2.6	nF

The measured waveforms of the converter operating in VFQR mode are shown in Fig. 6. The inductor current has a peak value of 11 A while the valley current reaches -2 A. The inductor average current is 4.5 A and the switching frequency is 192 kHz. Fig. 7 provides the measured waveform of the converter operating in the PFM mode. The inductor average current is 0.4 A and the converter is operating with the lowest switching frequency, $f_{min} = 68$ kHz.

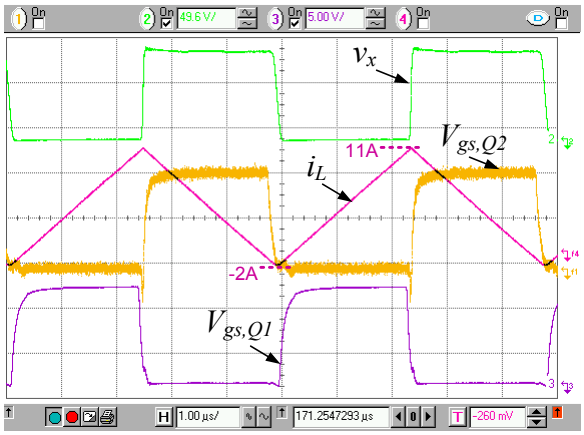


Fig. 6. Measured steady state waveforms of the converter operating in VFQR mode. f-1: $V_{gs,Q2}$, 5 V/div; ch-2: v_x, 49.6 V/div; ch-3: $V_{gs,Q1}$, 5 V/div; f-4: i_L, 5 A/div.

The measured efficiency is shown in Fig. 8(a) for the different operating modes. For this particular design, despite the higher conduction losses, VFQR mode provides a higher efficiency even at high load currents, however operating in this mode for $I_L > I_{L,QR,max}$ violates the inductor constraints of Fig. 2(b). PFM offers a very high efficiency at light-load

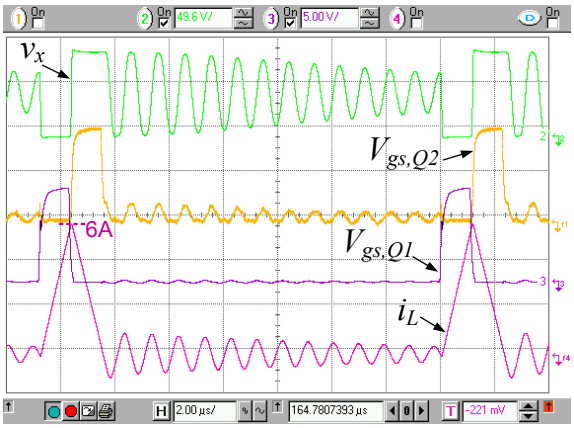


Fig. 7. Measured steady state waveforms of the converter operating in PFM mode. f-1: $V_{gs,Q2}$, 5 V/div; ch-2: v_x, 49.6 V/div; ch-3: $V_{gs,Q1}$, 5 V/div; f-4: i_L, 2 A/div.

conditions, as shown in Fig. 8(a). The efficiency of the tri-mode boost converter with optimal mode-switching based on $I_{bt}*$ is shown Fig. 8(b). Peak efficiencies of 97.5% and 97% are achieved in the first and second quadrant, respectively. A minimum efficiency of 88% is maintained over the full load range and an efficiency improvement of 2.6% is achieved using VFQR mode over the FF mode at the boundary. Given that the high-side and low-side switches are identical, the efficiency curve in first and second quadrant should be identical, however the slight difference in the measurements can be attributed to variations in parasitic elements of Q_1 and Q_2, as well as the finite accuracy of the ZVS control scheme.

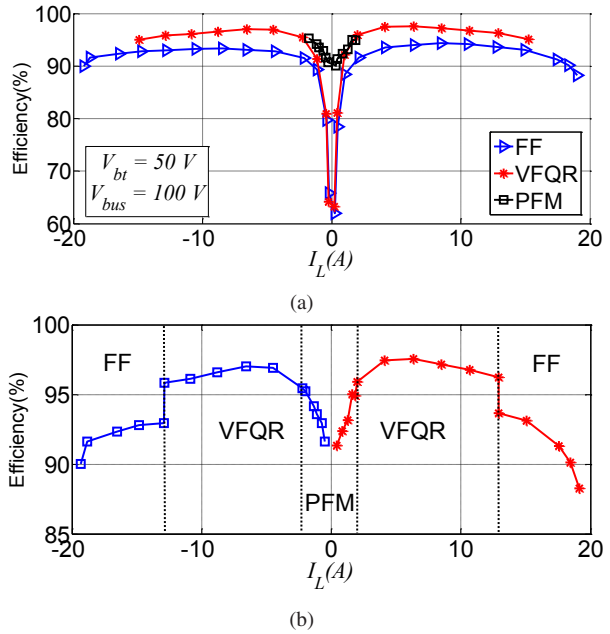


Fig. 8. Measured efficiency in (a) different modes of operation and with (b) Tri-mode converter.

The measured t_{d1} and t_{d2} for FF and VFQR modes in both quadrants are shown in 9(a). The measured f_s of the tri-mode boost converter is shown in Fig. 9(b). The minimum switching frequency at $I_{L,min}$ is 68 kHz, which lies safely outside of the audible band. The frequency drops from 400 kHz to 90 kHz at the border of VFQR mode. In this application the system power optimizer that periodically updates $I_{bt}*$ can be designed to avoid operating right at the boundary of FF and VFQR mode to to avoid frequent mode-switching and the associated EMI issues.

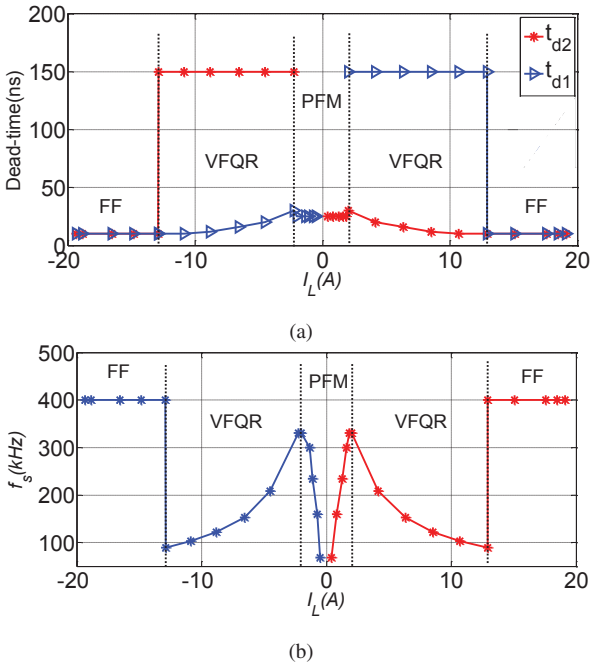
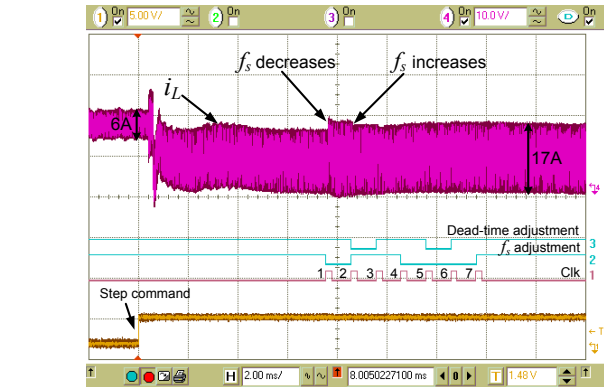


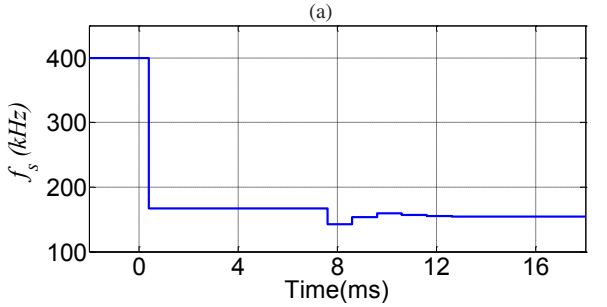
Fig. 9. Measured (a) dead-time and (b) switching frequency in the tri-mode bi-directional converter.

The transient response of the converter due to a step in $I_{bt}*$ from 15 A to 6.5 A is shown in Fig. 10. The converter first operates in FF mode at 15 A and automatically switches to VFQR mode following the command-step. The measured converter waveforms are shown in Fig. 10(a). The switching frequency is shown in Fig. 10(b) during the automatic adjustment process in VFQR mode. The frequency f_s is first updated based on a feed-forward and then fine-tuned using a binary search algorithm, as described in Section II. The dead-time and frequency fine-tuning begin 7 ms after the command-step, when steady-state is detected. The frequency and dead-time adjustment are done in less than 15 ms which is an order of magnitude faster than the update rate of $I_{bt}*$. Operating in FF mode, the switching frequency at 15 A is 400 kHz and the optimized switching frequency in VFQR mode at 6.5 A is 154 kHz while the valley current $I_v \approx$ -2 A.

The converter's transient response due to a change in $I_{bt}*$ from 3 A to 9 A is shown in Fig. 11. The converter operates in VFQR mode for both values of $I_{bt}*$. The measured converter waveforms are shown in Fig. 10(a). The switching frequency of the converter, which is calculated using the method described in Section II, is shown in Fig. 11(b). The optimized switching frequency at 3 A and 9 A is 227 kHz and 110 kHz respectively, while the converter maintains a nearly constant valley current of $I_v \approx$ -2 A.

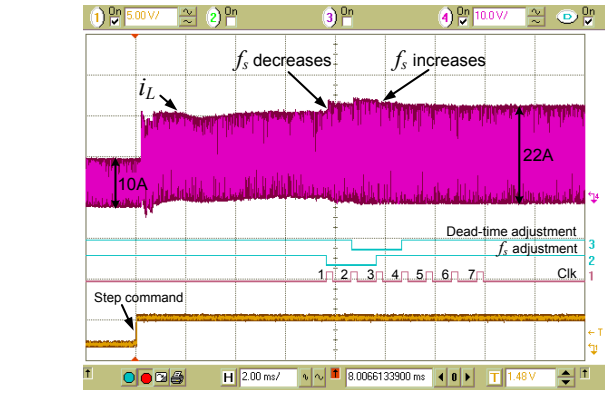


(a)

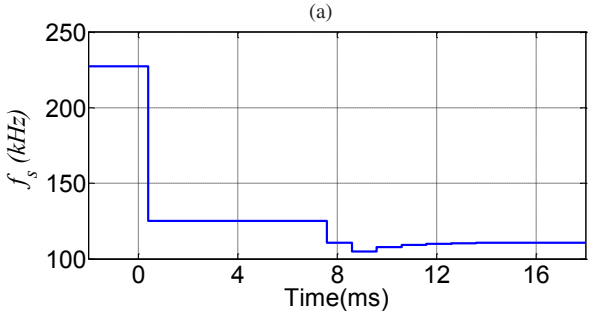


(b)

Fig. 10. Measured transient response of the converter due to a step in $I_{bt}*$ from 15 A to 6.5 A. (a) Inductor current and internal digital adjustment signals. ch-4: i_L, 10 A/div. f_s adjustment = 0 indicates that the frequency is decreasing. Dead-time adjustment = 0 indicates that the dead-time is increasing. (b) Switching frequency during calibration process.



(a)



(b)

Fig. 11. Measured transient response of the converter due to a step in $I_{bt}*$ from 3 A to 9 A. (a) Inductor current and internal digital adjustment signals. ch-4: i_L, 10 A/div. f_s adjustment = 0 indicates that the frequency is decreasing. Dead-time adjustment = 0 indicates that the dead-time is increasing. (b) Switching frequency during calibration process.

IV. Conclusions

In this work we have demonstrated the concept of variable-frequency quasi-resonant operation for maintaining a constant dead-time and a near constant inductor valley current in the mid-load range. Fixed frequency and PFM modes are combined with the VFQR operation to obtain a tri-mode bi-directional converter that can operate with a high efficiency over the full load range. Steady-state and dynamic experimental results for the 2 kW prototype boost converter show the effectiveness of the approach.

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