Current-Mode Bi-directional Single-Inductor Three-Port DC-DC Converter for Portable Systems with PV Power Harvesting

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KEYWORDS

<<DC power supply>>, <<Photovoltaic>>, <<Battery charger>> and <<Renewable energy systems>>.

ABSTRACT

This work targets low-power portable electronic applications with PV power harvesting. A bi-directional dc-dc converter is required to interface the battery with the load and PV module. A new current-mode scheme is applied to the single-inductor three-port converter, where the peak and valley inductor current are controlled by two separate digital regulation loops. The controller is shown to regulate both the PV voltage and the load voltage in the presence of load and irradiance steps. In solar deficit mode, energy is transferred from the battery to the load indirectly through the PV node, eliminating the two input switches used in conventional dual-input, dual-output converters. The scheme is demonstrated on a digitally controlled 1 W harvester prototype.

I. INTRODUCTION

Energy harvesting from photovoltaic (PV) cells is widely used in self-sustaining Wireless Sensor Nodes (WSNs) [1]. Built-in solar charging capability is also appealing in smart phones and other low-power portable devices [2] in order to extend the battery life.

The typical power management architecture for portable devices with PV power harvesting is shown in Fig. 1(a), where two cascaded dc-dc converters are used. The first dc-dc converter performs Maximum Power Point Tracking (MPPT), while the second regulates the load voltage, V_{load}. This conventional architecture has uni-directional dc power flow and is straightforward to control. In cases where the load requires high-power bursts, ultracapacitors can be used to complement the battery [3], as has also been shown for hybrid vehicles electric vehicles [4].

In low-power high-density portable applications, the component count is of critical importance. The number of inductors can be halved by using a Single-Inductor (SI) Dual-Input Dual-Output (DIDO) converter, as shown in Fig. 1(b) [5]–[8]. At this power level, the power-stage and controller can be monolithically integrated, while the inductor(s) are off-chip [7]–[9]. In order to use standard control schemes that assume uni-directional power flow in multi-port single-inductor converters, the battery is connected both at the output and input ports using an additional switch, as shown in Fig. 1(b). In [5], DCM operation with time-scheduling is used to regulate V_{load}, as well as manage the power flow during heavy/light loads and under varying irradiance conditions. While this topology eliminates one inductor compared to Fig. 1(a), the use of two additional switches to connect V_{bat} to a separate input port increases the system cost unnecessarily. The main objective of this work is to demonstrate a single-inductor three-port converter that directly supports bi-directional power flow from the battery,

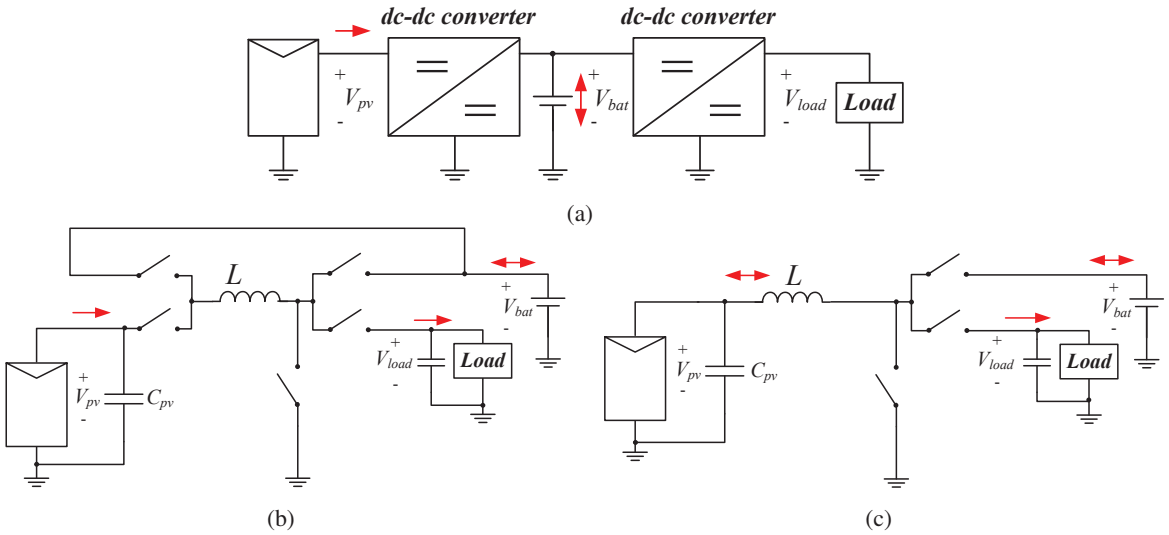


Fig. 1. Power management architectures with PV power harvesting. (a) Two cascaded dc-dc converters. (b) Single-inductor DIDO converter with uni-directional power flow. (c) Bi-directional three-port converter used in this work. The V_{pv} node is used to buffer energy transfer from the battery to the load during solar deficit conditions.

without requiring additional switches, as shown in Fig. 1(c). The control of this converter under the various power scenarios is the major challenge addressed in this work.

The paper is organized as follows. Section II outlines the current-mode control scheme for the bi-directional single-inductor converter. Section III describes the practical implementation and simulation results. Experimental results for the prototype are reported in Section IV.

II. Proposed Converter Architecture and Control Scheme

The topology and mixed-signal controller proposed in this work are shown in Fig. 2(a) and (b), respectively. The converter is a synchronous boost SIDO, and the controller is specifically designed to handle both positive and negative inductor current, $i_L(t)$. In this project, $V_{load} < V_{bat}$, therefore M_2 is implemented using back-to-back transistors for reverse blocking capability. The control scheme is based on current-programmed mode control (CPM) for both peak and valley inductor currents.

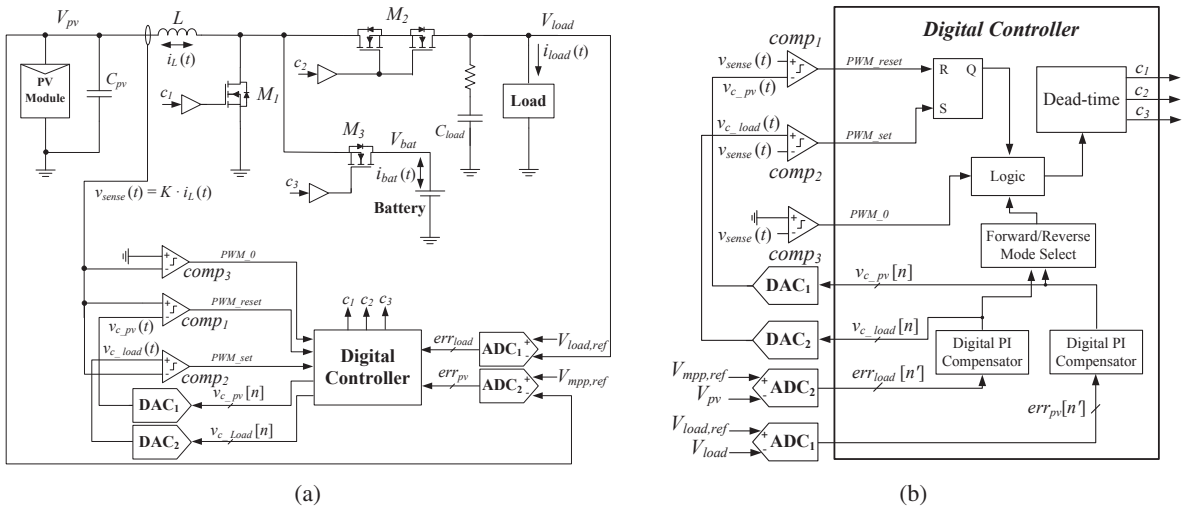


Fig. 2. (a) Bi-directional SI three-port dc-dc converter architecture and (b) digital controller.

The peak, valley and zero-crossing of the inductor current, $i_L(t)$, are detected by the three comparators, $comp_1$, $comp_2$ and $comp_3$, respectively. There are two separate voltage regulation loops in the system. The first loop regulates V_{load} to $V_{load,ref}$, while the second loop regulates the PV voltage,

V_{pv}, to the reference set by the outer MPPT loop, $V_{mppt,ref}$. Using an inner voltage loop in MPPT systems is well known to increase the control system robustness to variations in irradiance [10].

The operating modes are characterized by the relative steady-state values of the dissipated load power, P_{load}, and the generated PV power at MPP, P_{MPP}.

1) **Solar Deficit: Discharge**: $P_{MPP} < P_{load}$. The battery is discharged to meet the load demand, $P_{batt} = P_{MPP} - P_{load}$, until the battery is fully discharged.
2) **Solar Deficit: Lockout**: $P_{MPP} < P_{load}$. If the battery becomes fully discharged, the system enters under-voltage lockout and shuts down.
3) **Solar Excess: Charging**: $P_{MPP} > P_{load}$. The harvested power exceeds the load and the battery is charged with the excess power, $P_{batt} = P_{MPP} - P_{load}$, until the battery is fully charged.
4) **Solar Excess: Power Tracking**: $P_{MPP} > P_{load}$. If the battery is fully charged, the MPPT must be disabled and PV voltage loop reference is set simply to provide load-power tracking. Power tracking mode is discussed in the literature [11] and not treated here.

The ideal waveforms of each mode are shown in Fig. 3. The three inductor current slopes m_1 to m_3, correspond to the gating signals c_1 to c_3, respectively, and are given by

$$[m_1 \quad m_2 \quad m_3] = [\tfrac{V_{pv}}{L} \quad \tfrac{V_{load}-V_{pv}}{L} \quad \tfrac{V_{bat}-V_{pv}}{L}]. \tag{1}$$

The additional operating conditions, such as when P_{load} =0 are not discussed here, since the control reduces to a conventional SISO boost charging scheme. The main focus of this paper is the Solar Deficit (Discharge) and Solar Excess (Charge) modes, where the converter operates with three active ports. In particular, the Solar Deficit mode requires that i_L crosses zero during each cycle.

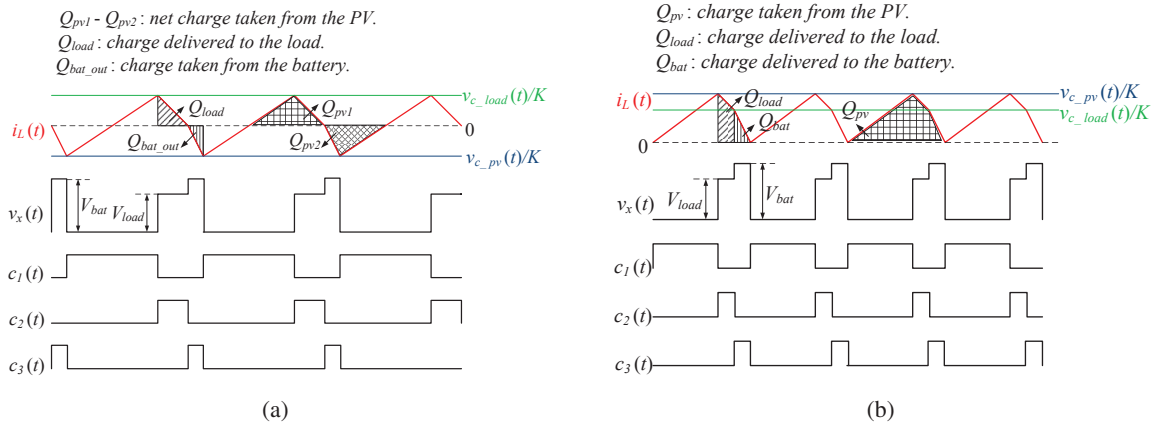


Fig. 3. Ideal steady-state waveforms for (a) Solar Deficit and (b) Solar Excess mode.

A. *Solar Deficit: Battery Discharging*

In Solar Deficit mode, the converter first charges the inductor in the reverse direction from the battery, then the charge is released to the input capacitor, C_{pv}, as shown in Fig. 3(a). The switch M_2 is then turned *on* to release the charge to the load. The peak inductor current, I_{c_load}, is set by v_{c_load}, which is controlled to regulate V_{load}, while the valley current, I_{c_pv} is set by v_{c_pv} to regulate V_{pv} for MPPT. Note that I_{c_pv} refers to the absolute value of the valley current, which is negative in this mode.

The converter uses the V_{pv} node to indirectly transfer energy from the V_{bat} to V_{load}. The ratio between the steady-state peak and valley inductor current is given by

$$\frac{I_{c\_load}}{I_{c\_pv}} = \sqrt{\frac{P_{load}}{P_{bat}} \cdot \frac{V_{load} - V_{pv}}{V_{bat} - V_{pv}} \cdot \frac{V_{bat}}{V_{load}}} = K_c. \tag{2}$$

Based on the energy balance analysis, the peak current is given by

$$I_{c\_load} = 2I_{load}\left(1 + \frac{1 + 1/K_c}{m_1/m_2} + \frac{m_2}{m_3 K_c}\right), \tag{3}$$

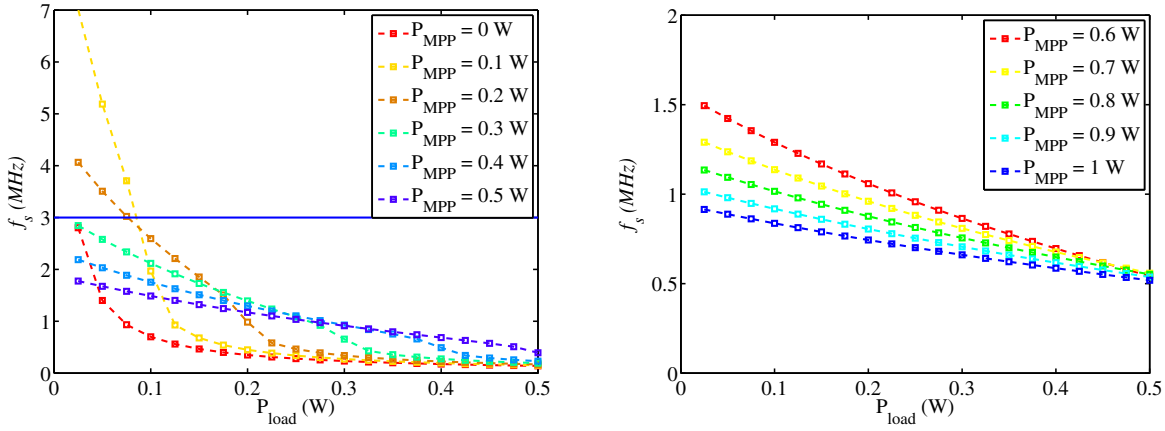
and the switching frequency can be shown to be

$$f_s = \frac{2I_{load}m_2}{I_{c\_load}^2}, \tag{4}$$

which is plotted in Fig. 4(a) for the prototype specifications listed in Table I. In this work, the maximum frequency is limited to 3 MHz under light load conditions. Note that the minimum load can be further reduced by switching to Pulse Frequency Modulation (PFM), which adds to the control complexity. The MPPT efficiency, η_{mppt}, is adversely affected by the ripple at V_{pv},

$$\Delta V_{pv} = \frac{Q_{pv1}}{C_{pv}}. \tag{5}$$

The relationship between ΔV_{pv} and η_{mppt} is well covered in [12] and can be used to size the input capacitance under worst case conditions.



(a) (b)

Fig. 4. Variation of the switching frequency with load power when (a) $P_{MMP} \leq 0.5$ W and (b) $P_{MMP} > 0.5$ W.

During night-time operation, when the PV module is not irradiated, the MPPT loop can be disabled and V_{pv} becomes an independent variable. A high value of V_{pv} is desirable to reduce the peak current I_{c_load}. At the same time, V_{pv} should not significantly exceed the open-circuit voltage, V_{oc}, otherwise the non-irradiated PV module operates in the fourth quadrant and dissipates some power. The V_{oc} is given by

$$V_{oc} = \alpha\frac{kT}{q}\ln\left[\frac{I_p}{I_s} + 1\right], \tag{6}$$

where α is the diode ideality constant, kT/q is the thermal voltage, I_s is the diode saturation current and I_p is the photocurrent, which is empirically given by

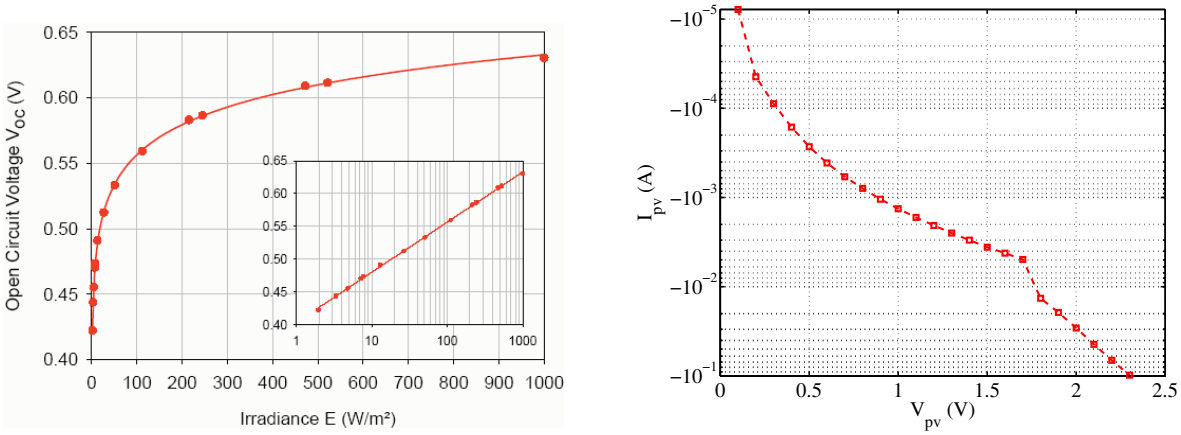
$$I_p = (I_{p0} + K_I\Delta T)\frac{G}{G_0}, \tag{7}$$

where I_{p0} is the nominal photocurrent at room temperature, G_0 = 1000 W/m^2, ΔT is the deviation from room temperature, G is the irradiance and K_I is the temperature coefficient of the short-circuit current, I_{sc}. The measured variation of V_{oc} with irradiance, G, for a commercial PV cell is shown in Fig. 5(a) [13]. In total darkness (G = 0), which never occurs in practical environments, V_{oc} = 0; the

topology has the limitation that sending power from the battery to the load incurs a power loss of

$$P_{loss} = I_s V_{pv} \left[\exp\left(\frac{qV_{pv}}{\alpha kT} \right) - 1 \right]. \tag{8}$$

The cell current versus voltage was measured for the PV array under practical night-time conditions, as shown in Fig. 5(b). The PV array consists of 18 parallel-connected mono-crystalline silicon panels, each of which has four cells in series. In this case, operating with V_{pv} = 1 V and 1.5 V results in P_{loss} = 1.5 mW, and 6 mW, respectively. Ideally, V_{pv} should be dynamically controlled versus load power in dark conditions to optimize the system efficiency.



(a) (b)

Fig. 5. (a) Open-circuit voltage variation with irradiance [13]. (b) Measured I-V curve under dark condition.

B. Solar Excess: Battering Charging

In Solar Excess mode, the converter operates in critical conduction mode as shown in Fig. 3(b). After charging i_L, M_2 is turned *on* to release the charge to the load. The on-time of M_2 is controlled by the current command, v_{c_load}, which is generated by the load voltage regulation loop. The remainder of the charge, Q_{bat} is released to the battery by turning M_3 *on*, until $i_L(t)$ reaches 0. The peak inductor current is set by v_{c_pv}, which is set by the PV voltage regulation loop. Using this simple dual current-loop, variable frequency scheme avoids the need for slope compensation. Pseudo-CCM mode [14] can alternatively be used to operate at fixed frequency while reducing the current ripple, at the expense of an additional free-wheeling switch across the inductor.

The ratio between the steady-state PV current and load current commands is given by

$$\frac{I_{c\_pv}}{I_{c\_load}} = \sqrt{\frac{P_{load} + P_{bat}}{P_{bat}}} = K_c'. \tag{9}$$

Based on the energy balance analysis, the peak current is given by

$$I_{c\_pv} = 2I_{load} \left(\frac{1 + \frac{m_2}{m_1} - \frac{1}{K_c'} + \frac{m_2}{m_3 K_c'}}{1 - \frac{1}{K_c'^2}} \right), \tag{10}$$

and the switching frequency can be shown to be

$$f_s = \frac{2I_{load} m_2}{I_{c\_pv}^2 (1 - \frac{1}{K_c'^2})}, \tag{11}$$

which is plotted in Fig. 4(b) for the prototype specifications listed in Table I.

C. MPPT Algorithm

A fast analog MPPT technique for low-power PV harvesting applications based on a tuned load-line is described in [15]. The fractional open-circuit voltage (FVOC) MPPT method is most commonly

used at power level of a few watts [16], due to reasonable accuracy and low cost. In FVOC, the MPPT reference voltage, $V_{MPP,ref}$, is set to $K_{oc}V_{oc}$, where 0.7< K_{oc} <0.8, depending on the specific panel. To measure V_{oc}, a switch can be connected in series with the PV panel to temporarily open-circuit the panel. Alternatively, a small auxiliary panel left open-circuited can be used to sample V_{oc}. Both of these approaches increase the system cost.

In this work, since the inductor current information is available in the digital controller due to chosen current control scheme, V_{oc} can be measured by explicitly setting the average inductor current, $\langle i_L \rangle$, to zero. The proposed fractional V_{oc} operation is described in Fig. 6. When MPPT is initiated, the converter is forced to operate temporarily in Solar Deficit mode. I_{c_pv} is first set to I_{c_load}, and then adjusted until $\langle i_L \rangle$ = 0, which occurs when

$$\frac{I_{c\_load}}{I_{c\_pv}} = \sqrt{\frac{1 + \frac{V_{pv}}{V_{bat} - V_{pv}}}{1 + \frac{V_{pv}}{V_{load} - V_{pv}}}}, \tag{12}$$

where $V_{pv} = V_{oc}$. In order to maintain load regulation, I_{c_load} is adjusted at each iteration of I_{c_pv}. Once (12) is satisfied, V_{pv} is sampled and $V_{MPP,ref}$ updated.

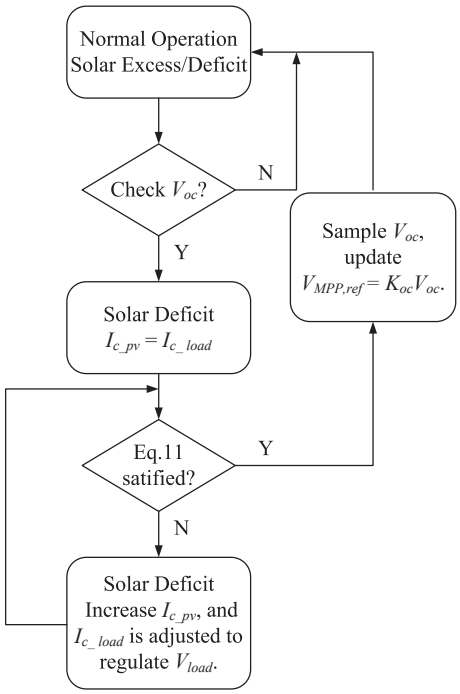
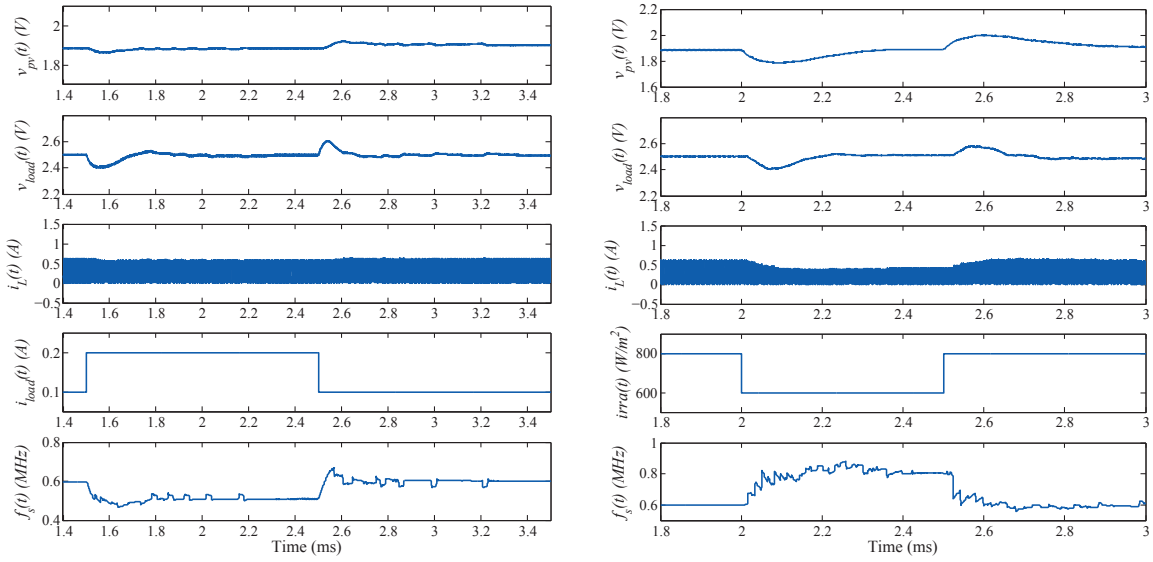


Fig. 6. Fractional V_{oc} operation to determine $V_{MPP,ref}$.

III. Simulation

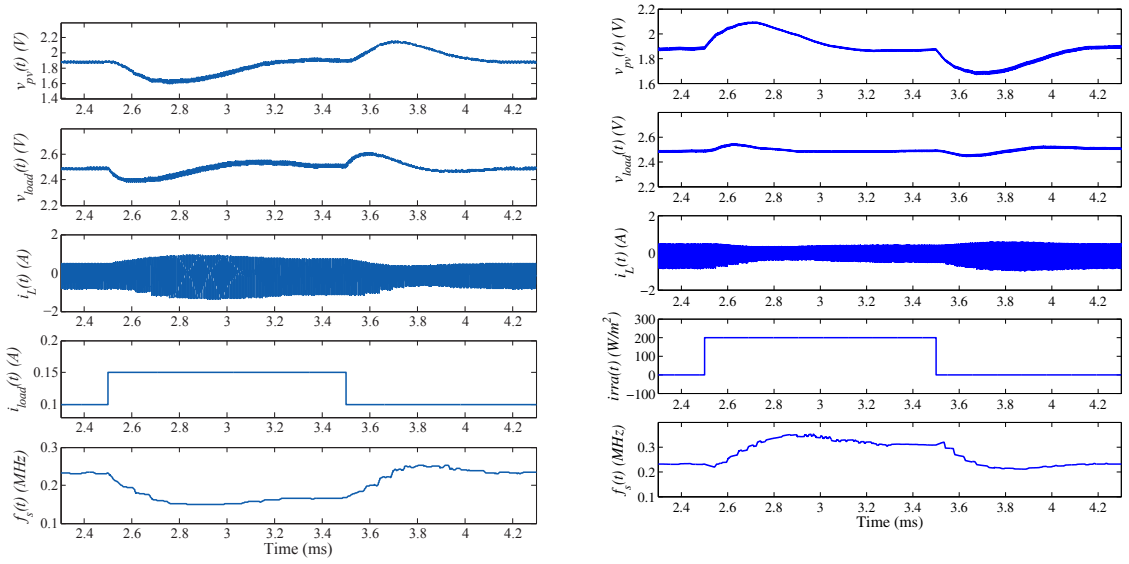
An accurate mixed-signal simulation of the full closed-loop system was performed using Cadence AMS Designer, in order to include all the quantization effects of the mixed-signal control scheme. The outer MPPT loop is not included in the simulation and $V_{MPP,ref}$ is therefore constant. A load-step response in Solar Excess mode is shown in Fig. 7(a). It can be seen that, as the load current changes, the MPPT voltage loop is well damped. Under a 100 mA load step, V_{load} stays within 100 mV of $V_{load,ref}$ and the loop settles within 200 μs. In Fig. 7(b), an irradiance step is applied in the Solar Excess mode to emulate rapid shading. As the PV voltage loop regulates, less than 100 mV of disturbance is observed at V_{load}. The good cross-regulation is expected, due to the well-known line regulation advantages of current mode control. A 50 mA load-step in Solar Deficit mode is shown in Fig. 8(a). V_{load} is regulated within 100 mV of $V_{load,ref}$, and V_{pv} is regulated within 200 mV of $V_{MPP,ref}$. A step in irradiance is applied in the Solar Deficit mode, as shown in Fig. 8(b). As the PV

voltage loop regulates, less than 50 mV of disturbance is observed at V_{load}. The variation in switching frequency, f_s, is also shown in the different modes.



(a) (b)

Fig. 7. (a) Load step response and (b) irradiance step response in Solar Excess mode.



(a) (b)

Fig. 8. (a) Load step response and (b) irradiance step response in Solar Deficit mode.

IV. Experimental Results

An experimental SI three-port converter prototype was built to demonstrate the bi-directional control scheme, as shown in Fig. 9. The digital controller is implemented on a Xilinx FPGA. A system clock of 50 MHz is used. The system parameters are listed in Table I. The PV array has a rated power of 1 W. The steady-state waveforms during Solar Deficit and Excess modes are shown in Fig. 10(a) and (b), respectively. The load current is 100 mA.

A 50 mA load step is applied in Solar Deficit mode, as shown in Fig. 11(a). V_{load} and V_{pv} are regulated within 120 mV and 240 mV, respectively. A 100 mA load step is applied in Solar Excess mode, as shown in Fig. 11(b). V_{load} is regulated within 120 mV, and little disturbance is presented on V_{pv}. Zoomed captures of Fig. 11(b) are shown in Fig. 12(a) and (b), for positive and negative load steps,

respectively. In Fig. 13(a), as V_{pv} responds to a step change in $V_{MPP,ref}$, V_{load} experiences a 200 mV overshoot, and the recovery time is 140 μs. The measured system efficiency is shown in Fig. 13(b). In Solar Excess mode, the efficiency increases with load power, due to the lower switching frequency at higher load. In Solar Deficit mode, the efficiency is lower, at 82.5%, due to higher conduction losses. While the prototype is sufficient for demonstrating the control scheme, the efficiency could be significantly improved with smaller on-chip power MOSFETs and optimized drivers.

TABLE I
PROTOTYPE SPECIFICATIONS

Specification	Value	Units
PV MPP Voltage, $V_{mpp,ref}$	1.9	V
Load Voltage, V_{load}	2.5	V
Battery Voltage, V_{bat}	4	V
Rated Load, $I_{load,rated}$	200	mA
Load Capacitor C_{load}	20	μF
PV Capacitor C_{pv}	40	μF
Filter, L	2.2	μH
R_{on}, M_1	31	mΩ
R_{on}, M_2	62	mΩ
R_{on}, M_3	57	mΩ
ADC Resolution (7 bits), Δv_{adc}	32	mV
DAC Resolution (12 bits), Δi_{dac}	2.5	mA

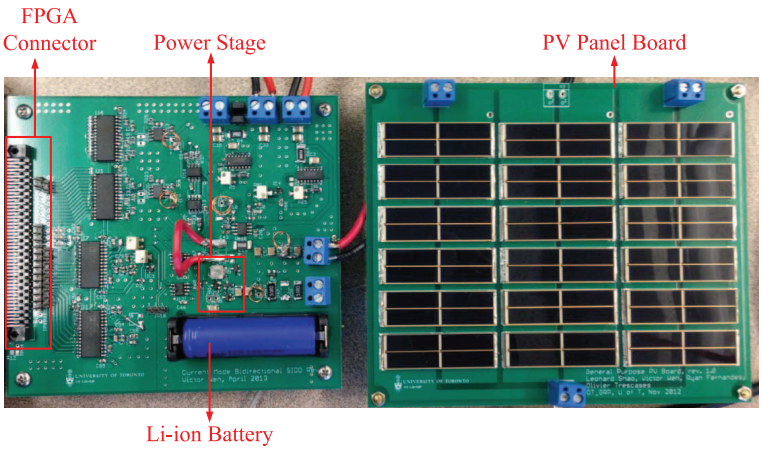
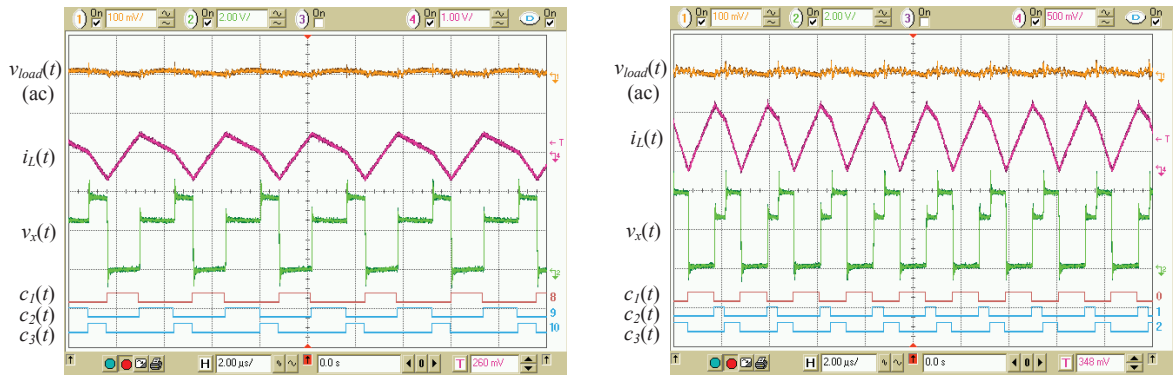
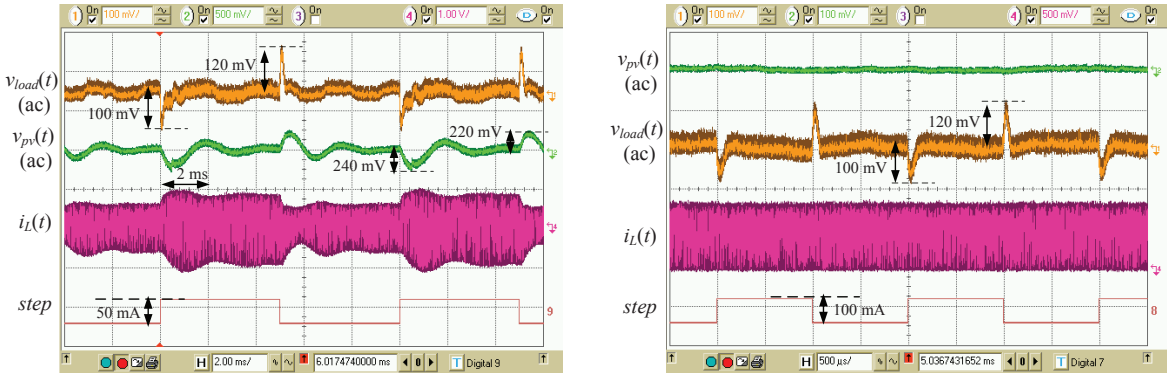


Fig. 9. Experimental prototype.



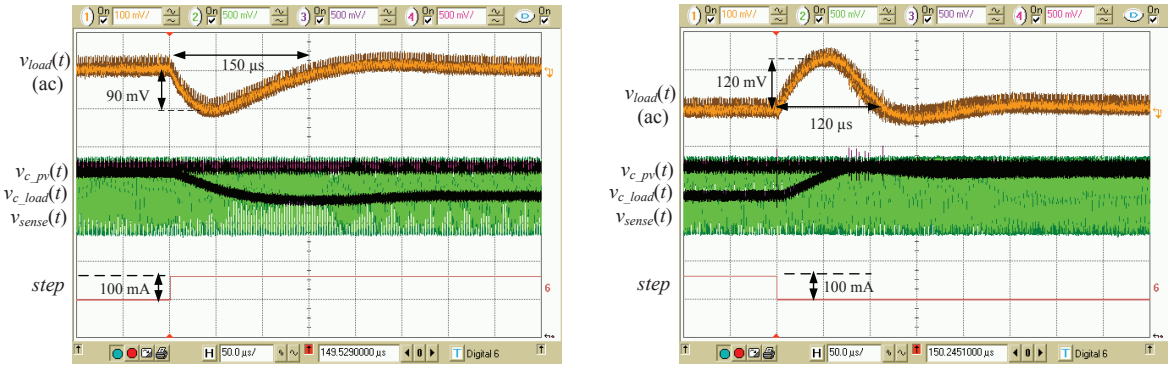
(a) (b)

Fig. 10. (a) Measured steady-state waveforms in Solar Deficit mode and (b) Solar Excess mode, at I_{load} = 100 mA.



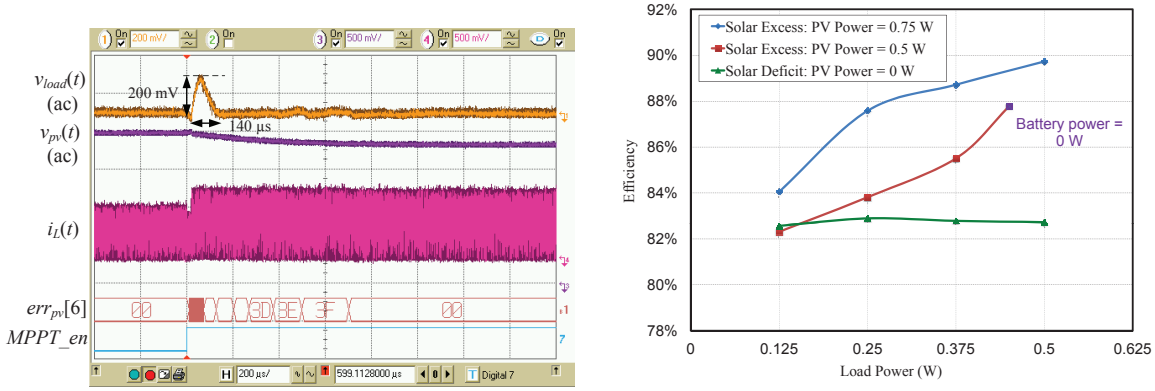
(a) (b)

Fig. 11. Measured transient waveforms in (a) Solar Deficit mode and (b) Solar Excess mode.



(a) (b)

Fig. 12. Zoomed transient waveforms in Solar Excess mode for (a) positive and (b) negative load step.



(a) (b)

Fig. 13. (a) Transient waveforms showing good cross-regulation between the MPPT voltage loop and the load regulation loop. (b) Measured system efficiency.

V. Conclusions

The proposed dual loop current-mode scheme, where both the inductor valley and peak currents are controlled separately, was shown to effectively regulate both the load voltage and the PV voltage. The converter maintains regulation in Solar Excess and Solar Deficit modes, while using the PV node to transfer energy from the battery to the load with minimal loss, even in practical dark conditions. The simulation and experimental measurements confirm both the steady-state and dynamic operation of the converter. Overall the converter provides reasonable dynamic response and efficiency for low-power PV applications, while reducing the system cost compared to using multiple SISO converters.

REFERENCES

[1] K. K. Win, X. Wu, S. Dasgupta, W. J. Wen, R. Kumar, and S. Panda, "Efficient solar energy harvester for wireless sensor nodes," in *Communication Systems (ICCS), 2010 IEEE International Conference on*, Nov. 2010, pp. 289–294.

[2] Y. Sun, X. Wu, and M. Zhao, "Single-inductor dual-output converter with dynamic power distribution," in *ASIC, 2009. ASICON '09. IEEE 8th International Conference on*, Oct. 2009, pp. 1097–1100.

[3] J. Varley, M. Martino, S. Poshtkouhi, and O. Trescases, "Battery and ultra-capacitor hybrid energy storage system and power management scheme for solar-powered wireless sensor nodes," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 4806–4811.

[4] S. Lukic, S. Wirasingha, F. Rodriguez, J. Cao, and A. Emadi, "Power management of an ultracapacitor/battery hybrid energy storage system in an hev," in *Vehicle Power and Propulsion Conference, 2006. VPPC '06. IEEE*, Sep. 2006, pp. 1–6.

[5] N.-M. Sze, F. Su, Y.-H. Lam, W.-H. Ki, and C.-Y. Tsui, "Integrated single-inductor dual-input dual-output boost converter for energy harvesting applications," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, May 2008, pp. 2218–2221.

[6] Y.-H. Lam, W.-H. Ki, C.-F. Tsui, and P. Mok, "Single-inductor dual-input dual-output switching converter for integrated battery charging and power regulation," in *Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on*, vol. 3, May 2003, pp. 447–450.

[7] M. Du and H. Lee, "A single-inductor dual-input dual-output buck regulator with enhanced power-delivery capability for portable battery management system," in *Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on*, Aug. 2010, pp. 1141–1144.

[8] H. Shao, C.-Y. Tsui, and W.-H. Ki, "A single inductor dido dc-dc converter for solar energy harvesting applications using band-band control," in *VLSI System on Chip Conference (VLSI-SoC), 2010 18th IEEE/IFIP*, Sep. 2010, pp. 167–172.

[9] Y. Nakase, S. Hirose, H. Onoda, Y. Ido, Y. Shimizu, T. Oishi, T. Kumamoto, and T. Shimizu, "A 0.5v start-up 87single-inductor dual-output (sido) boost dc-dc converter for battery and solar cell operation sensor network micro-computer integration," in *Custom Integrated Circuits Conference (CICC), 2012 IEEE*, Sep. 2012, pp. 1–4.

[10] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *Power Electronics, IEEE Transactions on*, vol. 20, no. 4, pp. 963–973, 2005.

[11] Q. Zhiyuan, W. Shengtie, L. Guangchen, and T. Guizhen, "Integrated control of energy management for stand-alone pv system," in *Asia-Pacific Power and Energy Engineering Conference, 2009.*, 2009, pp. 1–4.

[12] S. Kjaer, "Design and control of an inverter for photovoltaic applications," Ph.D. Thesis, 2005, aalborg University.

[13] "Ixolartm high efficiency solarmd." IXYS Datasheet, available at http://ixapps.ixys.com/DataSheet/20110107-SLMD121H04-DATA-SHEET.pdf.

[14] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-ccm/dcm simo switching converter with freewheel switching," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.

[15] W.-C. Liu, Y.-H. Wang, and T.-H. Kuo, "An adaptive load-line tuning ic for photovoltaic module integrated mobile device with 470us transient time, over 99*Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, 2013, pp. 70–71.

[16] T. Esram and P. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *Energy Conversion, IEEE Transactions on*, vol. 22, no. 2, pp. 439–449, 2007.