Power Management for Modern VLSI Loads using Dynamic Voltage Scaling

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Abstract — Modern deep sub-micron MOS devices suffer from a significant amount of DC leakage power dissipation due to the tunneling current across the ultra-thin gate oxide and off-state drain to source leakage, etc. In this paper, a dynamic voltage scaling (DVS) technique is demonstrated experimentally to provide an automated real-time control of the supply voltage according to the required VLSI core clock frequency. The DVS scheme is made practical with the use of a high efficiency soft-switching DC-DC converter and an on-chip frequency-to-voltage control loop. Using a 0.18µm CMOS CPLD chip to serve as a typical VLSI load, a power saving of greater than 50% at 0.6 times the maximum clock frequency was observed. This DVS architecture is suitable for managing the power consumption of modern VLSI chips where the demand on processing rate varies constantly.

I. Leakage Current Components in CMOS Devices

With the aggressive scaling of the gate length in deep sub-micron devices, many VLSI technologies are already utilizing ultra-thin gate oxide (t_{ox} < 2nm). According to the ITRS Roadmap [1], listed in Table 1, the requirement for even thinner t_{ox} will lead to even worst gate leakage current due to quantum mechanical effects [2]. The well-known gate leakage components are as illustrated in Fig. 1(a). These include Edge Direct Tunneling (EDT) and Gate-to-Channel Tunneling. Off-State drain leakage components due to extreme short channel effects [3] are as shown in Fig. 1(b). These include *pn*-junction diode leakage (I_1), weak inversion current (I_2), Drain-Induced Barrier Lowering (I_3), Gate-Induced Drain Leakage (I_4), Punch-through (I_5) and Narrow width effect (I_6). While significant effort at the device level has been made to reduce these leakage components (e.g. using high-*k* gate dielectrics), The ITRS Roadmap shows that these problems are only going to get worse as we move toward future generation technologies.

Table 1. ITRS Leakage Roadmap

Year	2001	2002	2003	2004	2005	2006	2007
Drawn L [nm]	90	75	65	53	45	40	35
Physical L [nm]	65	53	45	37	32	28	25
Equivalent t_{ox} [nm]	2.3	2.1	2	2	1.9	1.9	1.4
Nominal $I_{subthreshold}$ @ 25°C [µA/µm]	0.01	0.03	0.07	0.1	0.3	0.7	0.1
Nominal V_{DD}	1.2	1.1	1	1	0.9	0.9	0.7
Static Power, W/L=3 [nW/device]	5.6	6.7	10	11	26	53	53

The leakage components under consideration are voltage dependent. The HSpice simulated I-V characteristics for a 0.13µm MOS device are as shown in Fig. 2. In general, the leakage current can be reduced by either increasing the V_{TH} via body biasing or by reducing the V_{GS} (hence V_{DD}). ITRS predicts a continuing trend to reduce the power supply voltage to below 1V by 2005 (see Fig. 3). At the same time, the supply current per chip will greatly exceed 100A. Therefore, it is a significant challenge in the design of Voltage Regulation Modules (VRMs) to power current and future deep sub-micron VLSI chips.

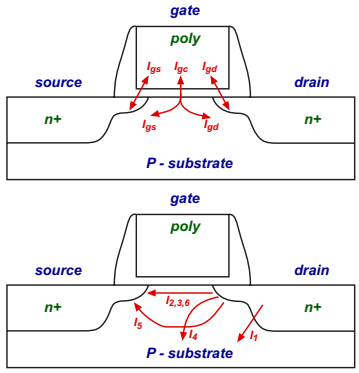

Fig. 1. Gate leakage (a) and off-state drain leakage (b) components in deep sub-micron MOSFETs with ultra-thin oxides.

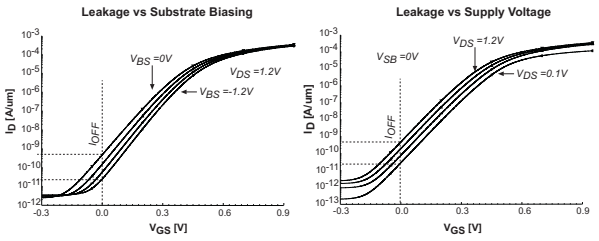

Fig. 2. Simulated drain leakage current in 0.13µm MOSFETs as functions of (a) substrate bias - hence V_{TH}, and (b) supply voltages - V_{GS}.

In addition, it is advantageous to dynamically adjust the power supply voltage level according to the VLSI chip's required processing load [4] in order to further reduce leakage power consumption. This technique, generally referred to as Dynamic Voltage Scaling (DVS), is especially useful to maximize the battery life of portable electronics.

In previous demonstrations of DVS techniques, the focus was placed primarily on the power consumption of the VLSI chip [5]. However, due to the inefficiency of most DC-DC switching power supplies required to provide a

wide range of output voltage levels, the power saving from the DVS scheme is often lost in the power supply circuits. In this work, a high efficiency soft-switching DC-DC converter with fast transient response implemented in 0.18µm CMOS technology [6] is designed to be an integral part of the DVS control loop. The DVS control loop is designed to provide transparent operation without the burden of any extra design overhead for the VLSI circuit designers.

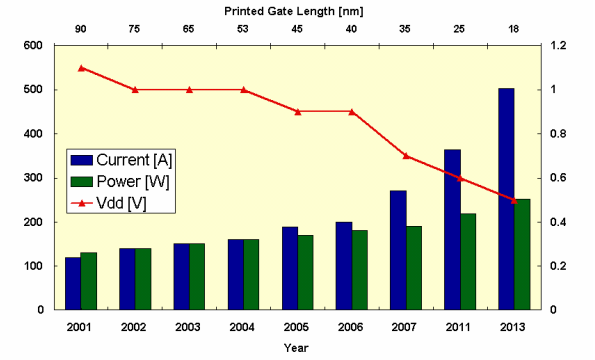

Fig. 3. ITRS Roadmap on supply voltage, current and power requirements.

II. Powering VLSI Chips using VRMs

Traditionally, all the circuit blocks in a VLSI chip are powered by a common V_{DD}-GND grid as shown in Fig. 4(a). However, since different circuit blocks are often required to provide a varying degree of performance at different times, the optimization of an appropriate V_{DD} level for the entire chip using DVS is very difficult. It is much more flexible if different circuit blocks are powered by their own dedicated power grid as shown in Fig. 4(b). Most modern power hungry VLSI chips (e.g. CPUs) are already being shipped in the form of PCB modules with custom designed VRMs around the periphery (see Fig. 5). These VRMs are often DC-DC converters, with off-chip inductors and capacitors, connected in parallel, or in an interleaved switching configuration. In DVS applications, it is possible to have each VRM powering an individual V_{DD}-GND grid. This allows for more efficient optimization of V_{DD} levels.

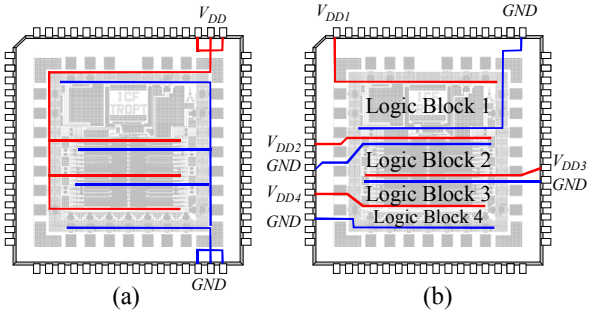

Fig. 4. (a) Conventional power lines inside a VLSI chip. (b) Multiple supply grids powering different circuit blocks in side a VLSI chip.

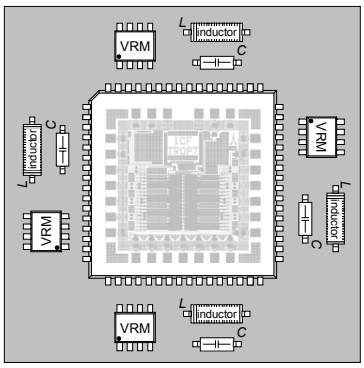

Fig. 5. A VLSI chip module with multiple VRMs to deliver power to the internal circuit blocks.

III. Dynamic Voltage Scaling System

Typically, the VRM is configured in a closed-loop control circuit using a fixed reference voltage, V_{ref} as the target output voltage. A simplified closed-loop DVS system [7] is as shown in Fig. 6. An on-chip VCO generates a clock signal, f_{VCO}, which is proportional to the critical path delay of the VLSI core [8] over process and temperature changes. A clock-scheduling algorithm inside the VLSI chip produces the reference clock f_{ref}. A controller provides a Pulse Width Modulated (PWM) signal to the DC-DC converter to regulate V_{DD} and match f_{VCO} to f_{ref}. This feedback loop ensures that the minimum V_{DD} is used to minimize both the CMOS dynamic power and DC leakage power dissipation over the entire range of f_{ref}.

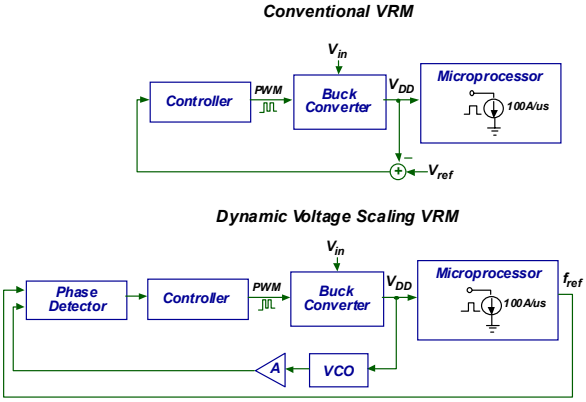

Fig. 6. A comparison between a conventional VRM and Dynamic Voltage Scaling VRM architecture.

The dynamic power can be drastically reduced by using the minimum V_{DD} for a given clock frequency while still maintaining proper circuit operation. The CMOS dynamic power dissipation is given as:

$$P_{dyn} \propto C \cdot V_{DD}^2 \cdot f_{clk} \qquad (1)$$

With constant V_{DD}, the power dissipation of a typical VLSI chip decreases proportionally when the clock frequency is reduced. At reduced frequency, the required supply voltage can also be lowered (limited by the V_{TH} of the MOS devices). An extra power saving can be realized as shown in Fig. 7. The reduction in V_{DD} also reduces both the on-state and off-state leakage power.

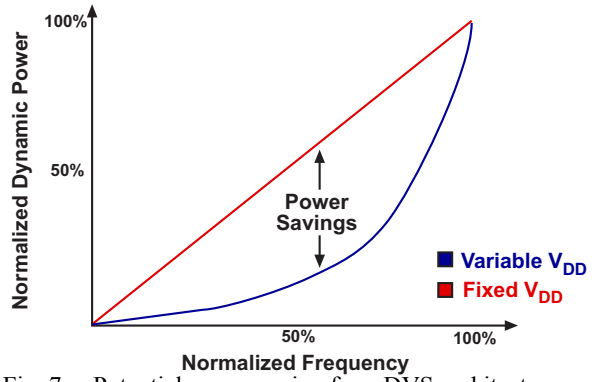

Fig. 7. Potential power saving for a DVS architecture.

IV. High Efficiency Soft-Switching DC/DC Converter

A key requirement of a DVS system is the ability to vary the supply voltage efficiently. Conventional switching power supply circuits are optimized to operate for one particular output voltage and current. Deviation from this rating will result in a degradation of efficiency, reducing the overall benefit of the DVS system. As a result, our proposed DVS architecture is designed with a Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) DC-DC converter as part of the integral system. This circuit serves as the main VRM for the VLSI chip. It is implemented in a 0.18µm mixed signal CMOS technology [6]. A micrograph of this DC-DC converter is as shown in Fig. 8. The corresponding block diagram showing the internal and the required external components are as given in Fig. 9. This chip employs precision gate drive timing circuits for the internal power transistors to provide optimal efficiency under a wide range of loading condition, as can be seen in Fig. 9. The use of ZVS-QSW topology also allows the switching frequency to be in the multi-MHz range, further reducing the component size of the external inductor and capacitor. The measured performance for the ZVS-QSW chip is summarized in Table 2. A peak efficiency of 82% is achieved at 5MHz as shown in Fig. 10. The efficiency of above 75% is maintained until the conduction losses of the MOSFET switches start to dominate. The efficiency would be greatly improved by using optimized power MOSFETs from a dedicated high voltage CMOS process.

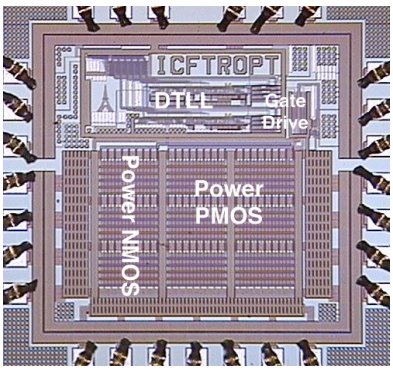

Fig. 8. Micrograph of a ZVS-QSW soft-switching DC-DC converter with precision dead time control. This chip was implemented in 0.18µm CMOS technology. Die size is 1.25×1.25 mm^2.

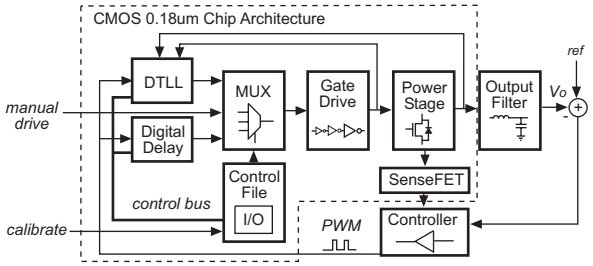

Fig. 9. Block diagram of the ZVS-QSW soft-switching DC-DC converter chip. Circuit blocks outside the dashed-box are off-chip components.

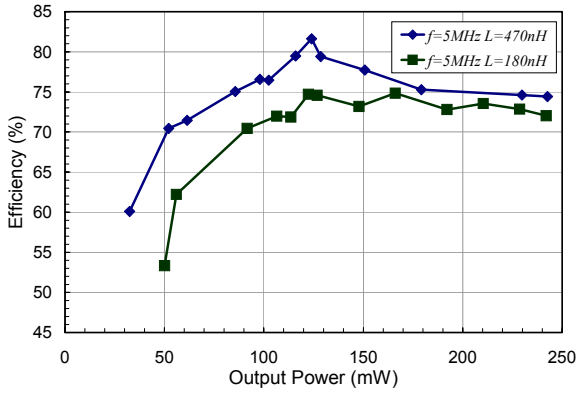

Fig. 10. Measured efficiency of the experimental ZVS-QSW converter for V_{in} = 2V, V_o = 1.4V.

Table 2. ZVS-QSW Chip Specifications

Technology	0.18µm Mixed-Signal CMOS
Input voltage	2V
Nominal output voltage	1V
Maximum dead-time	50ns
Die Area	1.56mm^2
DTLL power consumption	4.5mW
Peak efficiency	82%
Switching frequency	5 MHz
Output inductance	470nH
Output capacitance	6µF

V. DVS System Demonstration

An experimental DVS system was implemented using a state-of-the-art XC2C256 1.8V Complex Programmable Logic Device (CPLD) from Xilinx, as shown in Fig. 11. Eight 8-bit Multiply-Accumulate (MAC) DSP blocks are synthesized, along with a random data generator, to evaluate the power savings of this DVS system.

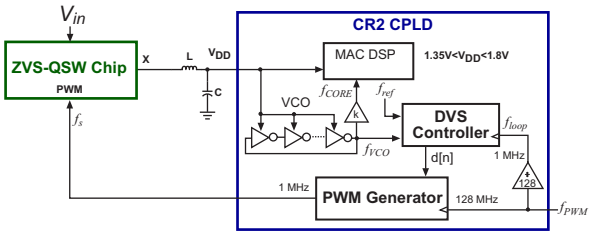

Fig. 11. A dynamic voltage scaling control loop. The unit under test is a Xilinx CoolRunnerII™ CPLD configured to represent a typical DSP load using 8 MAC blocks.

The MAC units can operate from 91 MHz to 141 MHz at V_{DD} = 1.35V and V_{DD} = 1.8V, respectively. The measured power saving for the MAC is as shown in Fig. 12. The DVS loop, as shown in Fig. 11, is implemented using a ring oscillator as a VCO and digital DVS controller that generates the PWM command signal $d[n]$. Both of these circuit blocks are on board the CPLD chip.

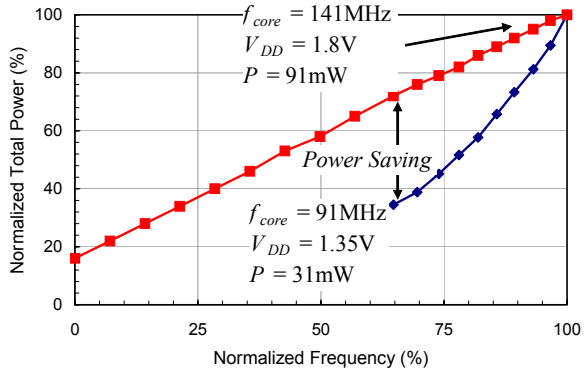

Fig. 12. Measured power savings for the MAC DSP module using the DVS scheme.

The DVS feedback loop consists of a dual mode controller. The operating condition is as illustrated in Fig. 13. A digital Proportional Integral and Derivative (PID) controller is used to achieve a fast transition from one reference clock frequency $f_{ref.}$ to another. Once steady state supply voltage is reached, the controller will revert back to the high efficiency ZVS-QSW mode with accurate gate timing signals. When temporarily operating in the PID DVS mode, the DC-DC converter briefly deviates from ideal soft-switching condition, with a fixed digital (instead of continuous adapted) dead-time to avoid cross-conduction in the power transistors.

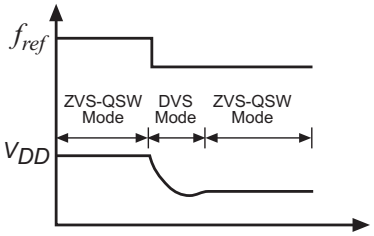

Fig. 13. Representation of a dual mode controller. The DVS loop is only used periodically to update the voltage reference for the ZVS-QSW loop when a new reference frequency is asserted.

The reference frequency, f_{ref} can be toggled externally to evaluate the transient performance of the DVS loop. The transient performance of the experimental DVS system with a PID controller is as shown in Fig. 14. The PID loop achieves a superior settling time of 22µs for the maximum V_{DD} step.

VI. Conclusions

Modern deep-submicron VLSI chips require distributed power supplies with DVS to optimize the dynamic and DC leakage power dissipation. In this paper, a practical DVS architecture is demonstrated using a high efficiency ZVS-QSW DC-DC converter to power a 0.18µm CPLD chip with a dual mode controller. Power saving is in excess of 50% at 0.6 times the maximum operating frequency. The operation of the DVS architecture is almost transparent to the VLSI designer. The only extra circuit design overhead required is a frequency scheduler to generate f_{ref} according to processing performance needs. This DVS architecture also provides the basis for optimum use of multiple VRMs to supply multiple power grids within a single VLSI chip.

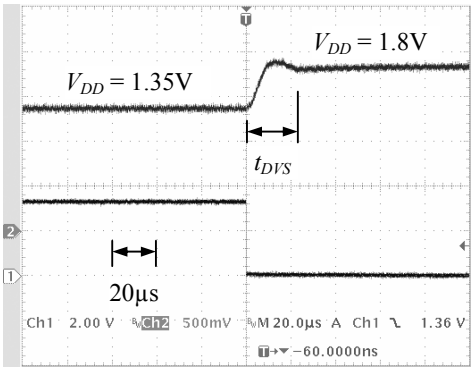

Fig. 14. Measured V_{DD} waveform with the digital PID controller. V_{DD} is scaled between 1.8V and 1.35V in 22µs. The lower waveform represents the step in $f_{ref.}$

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