Variable Output, Soft-Switching DC/DC Converter for VLSI Dynamic Voltage Scaling Power Supply Applications

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***Abstract*— The implementation of a low-voltage Zero-Voltage-Switching Quasi-Square-Wave (ZVS-QSW) buck converter capable of meeting the future challenges of low-voltage VRMs is presented. By eliminating switching losses, high-efficiency operation at switching frequencies beyond 1MHz is achieved. The design uses novel high-speed Dead-Time-Locked-Loops with fast dead-time error rejection to ensure Zero-Voltage-Switching under dynamic loads and variable output conditions. The ZVS-QSW converter, which was implemented in a mixed-signal 0.18 m CMOS process, has a measured efficiency of 82% at 5MHz with a 1.4V output. The ZVS-QSW converter is intended to supply the next generation VLSI chips with a variable supply voltage for Dynamic Voltage Scaling (DVS) applications. DVS refers to the real-time scaling of the supply voltage to the VLSI chip to minimize dynamic power consumption, while satisfying a variable target clock frequency. Several DVS strategies are examined, and it is shown that DVS can be applied to the ZVS-QSW converter using a dual-mode configuration. An experimental DVS test-bench was developed using a state-of-the-art Xilinx CPLD capable of operating from 1.35V to 1.8V. The PID controlled DVS system achieves the maximum V_{DD} transition in 22µs.**

I. INTRODUCTION

Today's high-speed, low-voltage VLSI applications require Voltage Regulation Modules (VRMs) having high dynamic response, high-efficiency and minimal footprint. These stringent demands are pushing the switching frequency, f_s, beyond several MHz. Increasing f_s will incur higher losses, such as the gate-drive loss and, in particular, the switching losses, P_{sw}, in conventional hard-switched synchronous Buck converters [1]:

$$P_{sw} = P_{turn-on} + P_{turn-off} \approx 2C_p(V_{in}^2 + V_{in}I_{out}t_r)f_s \qquad (1)$$

where $P_{turn-on}$ is the power dissipated during the charging of the parasitic capacitance C_p at the junction of the power switches during turn-on (see Fig. 2(a)), $P_{turn-off}$ is due to the overlapping of the V and I waveforms during turn-off, and t_r is the output rise time.

Maintaining high efficiency at high f_s is a major challenge. Soft-switching techniques can minimize noise and switching losses. Zero-Voltage-Switching (ZVS) is well suited to low-voltage MOSFET based converters, since capacitive switching loss can be eliminated through accurate dead-time control, as explained in section II.

The proliferation of handheld devices is underlining the need for aggressive real-time power-management strategies, beyond incremental efficiency improvements in DC/DC converters. Recently, interest is growing in a new class of power controllers capable of delivering variable performance for optimal power consumption. One scheme, known as Dynamic Voltage Scaling (DVS), or V_{DD} hopping, has gained popularity amongst researchers in recent years [2], [3]. In DVS, the supply voltage to a VLSI chip is minimized by the controller to achieve a target operating frequency. The technique relies on the fact that real-time computing tasks (such as frame decoding) often result in predictable workloads, and therefore the power management algorithm can dynamically select a target frequency to meet hardware operating limitations [software DVS]. The dynamic power dissipation in a generic digital circuit is

$$P_{dyn} \propto C \cdot {V_{DD}}^2 f \qquad (2)$$

where C is the lumped switched capacitance and f is the operating frequency. Reducing the frequency allows only proportional power savings since the switched energy per transition is fixed by V_{DD}. The delay in the critical path of a digital circuit in a short-channel CMOS technology can be estimated with a simple α power model, assuming that the transistor stays outside of the sub-threshold region [4]:

$$t_d = k \cdot \frac{V_{DD}}{(V_{DD} - V_{th})^{\alpha}} \propto \frac{1}{f_{MAX}}, V_{DD} > V_{th} \qquad (3)$$

and

$$\frac{\partial t_d}{\partial V_{DD}} = k \cdot \left(\frac{1 - \alpha V_{DD}(V_{DD} - V_{th})^{2\alpha - 1}}{(V_{DD} - V_{th})^{\alpha}} \right) \qquad (4)$$

where V_{th} is the MOFSET threshold voltage, f_{MAX} is the maximum clock frequency and α is the technology dependent velocity saturation coefficient, which varies between one and two. From eq. (4), it can be shown that $\partial t_d / \partial V_{DD} < 0$ and therefore both the maximum operating frequency and the dynamic power decrease as the supply voltage is scaled down. This well-known phenomenon is the basis for DVS. In DVS, V_{DD}, and f are scaled to achieve a quadratic power saving during low demand cycles.

A competing strategy for power reduction, known as Dynamic Threshold Scaling (DVTS), uses external substrate biasing to dynamically control V_{th} and reduce both dynamic

and leakage power consumption [2], [5], [6]. DVTS is more advantageous in nanotechnologies below 0.13µm, where sub-threshold leakage power dominates. The simulated power savings using DVS and DVTS for a ring oscillator in a 0.18µm CMOS process are shown in Fig. 1. DVS is clearly more advantageous in this technology, resulting in a wider operating range and power savings. Using DVS at the minimum supply voltage reduces the power to 4.3% of the maximum power, compared to 46.5% at the same frequency with no voltage scaling.

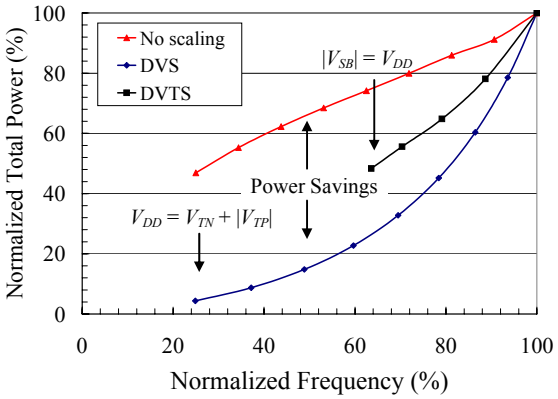

Fig. 1. Normalized simulated power savings for a 0.18µm CMOS ring oscillator using DVS and DVTS.

This paper proposes a dual-mode power converter making use of both DVS and soft-switching to address the future power management needs of VLSI modules. Section II provides background information and simulation results for the soft-switching converter mode. Section III focuses on the DVS mode, while Section IV explains the advantages of a dual mode converter. Implementation details and experimental results are presented in Section V and Section VI respectively.

II. ZERO-VOLTAGE-SWITCHING QUAZI-SQUARE-WAVE CONVERTER

A. Topology

Consider the MOSFET-based synchronous buck topology, as shown in Fig. 2. If L is reduced below L_{crit} given by eq. 5, the inductor current will flow in both forward and reverse direction, thus discontinuous-conduction mode is avoided. The reversed inductor current following low-side turn-off charges up the parasitic capacitance at node X in lossless resonance, thus P_{turn_on} in eq. 1 is eliminated [7]. Similarly, a lossless discharge occurs during the dead-time, T_2 due to the positive inductor current. The dead-times, T_1 and T_2 must be controlled in real-time in order to achieve the ideal zero-voltage-switching transitions of Fig. 2(b). A true ZVS-QSW converter minimizes switching and body diode losses and lowers the EMI due to the reduced dV_x/dt without increasing the power stage complexity. Further details concerning the ZVS-QSW

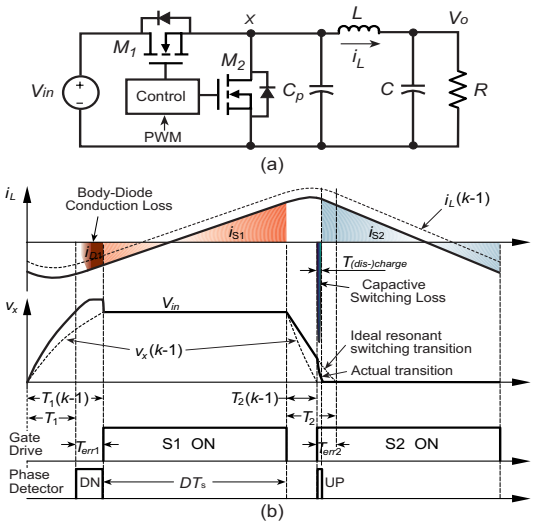

Fig. 2. (a) ZVS-QSW buck converter. (b) Load transient leads to dead-time errors and switching loss. The period k-1 has ideal dead-times.

topology are given by [7], [8].

$$L_{crit} = (1 - \frac{V_o}{V_{i(\min)}}) \cdot \frac{R_{(\min)}}{2 f_s} \qquad (5)$$

B. Dead-Time Control Strategies and Requirements

The ideal dead time delays T_1 and T_2 in Fig. 2(a) are determined by the resonant switching durations due to the charging and discharging of C_p by the valley and peak inductor currents, respectively. In turn, T_1 and T_2 are directly affected by the RMS output current. The ideal dead-times alternate between their respective maximum and minimum durations over the full range of load conditions.

A converter designed with fixed delays inevitably suffers from body-diode conduction losses when the delay is longer than ideal, or capacitive losses when the delay is shorter than ideal. These losses, which occur every switching cycle, are unavoidable since fixed dead-times cannot be optimized for all load conditions.

The simplest solution is an adaptive scheme in which the gate-drive is asserted after detecting the zero-voltage crossing [9]. This is not suitable in high-frequency applications where comparator and gate-drive delays (≈20ns) lead to severe positive dead-time errors.

An alternative approach proposed in [10] uses an opamp assisted V/I converter for the adaptive delay generator. The design assumes that the V_x transition is linear, therefore the $V_{in}/2$ crossing occurs at the middle of the ideal dead-time. This is used to assert the gate drive before the actual zero-voltage crossing. The main drawback is that the transition is not exactly linear and therefore external trimming is required to eliminate timing errors.

A "predictive" scheme based on a digital Delay-Locked-Loop (DLL) was proposed using a D-flip-flop phase detector and a digital delay line to track the ideal dead-time [11]. This robust scheme has relatively poor transient

performance, requiring numerous switching cycles to reach steady state. Moreover, even at steady state, the dead-time swings sub-harmonically around the ideal value due to the nature of the nonlinear ("bang-bang") phase detector and the fixed delay step. There is an inherent tradeoff between the steady-state dead-time accuracy and the settling speed of the DLL since the delay can only be incremented by one step per switching cycle. Therefore, the incremental digital delay cannot be reduced arbitrarily since the losses incurred with a slow DLL settling time can be prohibitive. This drawback renders this scheme unsuitable for applications with frequent load variations such as microprocessors. This paper proposes a design that employs analog Delay-Time-Locked-Loops (DTTL) to allow quick and accurate adjustments of the dead-times [10]. Comparators that sense the power MOSFETS' v_{DS} zero-voltage crossing (Comp_{VDS}) and v_{GS} threshold-voltage crossing (Comp_{VGS}) are followed by a phase detector as shown in Fig. 3. The phase detector provides up and down pulses for the charge pump. The charge pump outputs the delay control voltage V_{ctrl} that linearly determines the dead-time delay, which completes the negative feedback loop.

To maintain high-efficiency during load variations, it is desirable for the DTLLs to reach steady-state within at most several switching cycles. The gain of the DTLL can be expressed as:

$$|G| = \frac{I_{CP}}{I_{DL}} \cdot \frac{C_{DL}}{C_{CP}} < 1 \qquad (6)$$

$|G|$ must be chosen to be sufficiently large to obtain fast tracking without leading to instability in this discrete-time DTLL system with a fixed one-cycle delay. In the linear delay generator, as shown in Fig. 3(b), the PWM signal rapidly discharges C_{dl}, which is then linearly charged by I_{dl} until it reaches the buffered V_{ctrl}. The PWM signal is therefore delayed by

$$t_d = V_{ctrl} \cdot C_{dl} / I_{dl} \qquad (7)$$

For negative dead-time errors the resonant transition is not completed and C_p is charged/discharged almost instantaneously, resulting in an UP pulse generated by the phase detector (approximately $T_{(dis)charge}$), which is much shorter than the actual error T_{err}. This leads to poor tracking since the short UP pulse does not sufficiently correct the dead-time. The problem is solved by inserting a One-Shot block, as shown in Fig. 4, which linearly extends the UP pulses that exceed a minimum threshold length. Pulses narrower than the threshold are fed to the charge-pump, unaffected by the one-shot block. The value of this threshold can be digitally adjusted.

The references for the Comp_{VGS} in the high and low-side DTLLs are the threshold voltages of the *p* and *n*-channel MOSFETs, respectively. They are generated internally using dedicated circuits. The inputs of the comparator Comp_{VDS} are connected across the power transistors. To account for the small forward voltage drop of the power devices, a digitally trimmed offset is introduced to each comparator. If such DN pulses were fed directly into the charge pump, the DTLL's loop gain would be increased for small dead-time errors, possibly resulting in instability. A Down Pulse One-Shot block similar to the Up Pulse One-Shot block is inserted to shorten the DN pulses, creating a desirable control dead-zone. This dead-zone ensures that the DTLL loop gain is effectively reduced for small dead-time errors, yet largely unaffected for large errors.

The design also includes a senseFET-based current sensing structure as shown in Fig. 3(a). This technique was introduced in [12]. The i_{sense} current is fed into an external resistor. The resulting signal can be used as a current feedback in a high-bandwidth current-mode controller. The

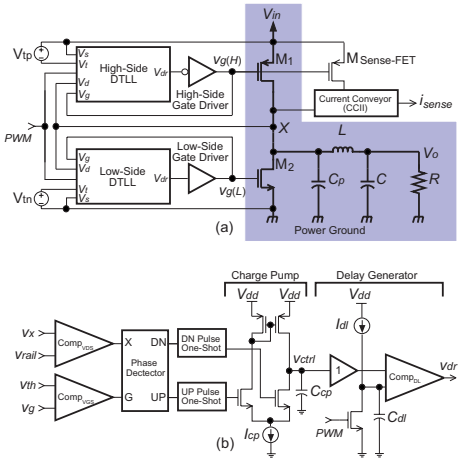

Fig. 3. (a) ZVS-QSW buck converter with Dead-Time-Locked-Loops. (b) Circuits inside one of the DTLL blocks.

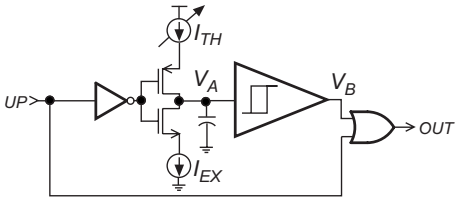

Fig. 4. Up One-Shot Block.

senseFET current sensing solution eliminates the heavy efficiency penalty incurred by traditional current-shunt resistors. More details concerning the current mode controller design are given by [13].

One of the major limitations of the ZVS-QSW converter is that the inductor current, i_L in Fig. 2(b) must be fully reversed before turning off the low-side switch M_2 at the start of T_1 in order to charge C_p. This condition is not met if the output current exceeds the maximum design value. This situation causes V_x to be discharged below ground and become clamped by the body-diode of M_2. Furthermore, the Comp_{VDS} in the High-Side DTLL does not toggle, causing a prolonged *UP* pulse, which charges V_{ctrl} to V_{dd}. The maximum amount of dead-time is then be applied to M_1, given by

$$t_{d(\max)} = V_{dd} \cdot C_{dl} / I_{dl} \quad (8)$$

The converter therefore exits the high-efficiency ZVS-QSW mode and experiences heavy, but tolerable body-diode losses thereby avoiding complete breakdown of the DC/DC converter.

C. Simulation Results

The HSpice transient simulation result for the peak current-mode controlled ZVS-QSW buck converter system under a dynamic load with large transient variations is shown in Fig. 5. The adjustment of V_{ctrl} in both DTLLs follows the inductor current rapidly. Therefore, the dead-time errors are essentially eliminated in two switching cycles. After several cycles, the dead-times reach steady state and the V_x waveform exhibits ideal ZVS resonant transitions similar to Fig. 2(b). The simulated loss distributions for the DTLL design compared to fixed 10ns dead-times are as shown in Fig. 6. Results are presented for rated (10A), light (1.5A) and dynamic loads (10kHz repetition). The DTLL circuitry clearly eliminates switching losses under constant and dynamic loads, maintaining high efficiency. The DTLL advantage is even more promising as f_s scales to 4MHz, where the on-chip efficiency is 93% under a dynamic load.

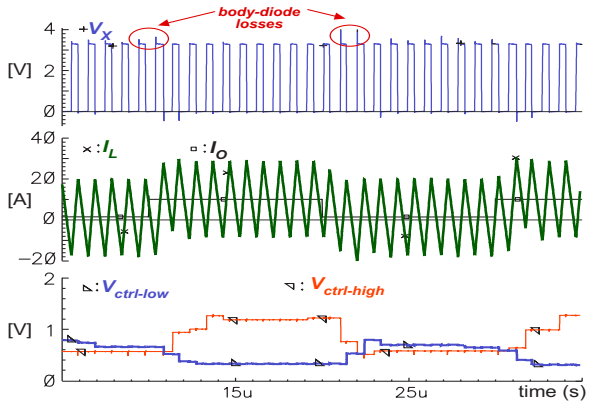

Fig. 5. HSPICE Transient waveforms of ZVS-QSW buck converter with DTLLs under a dynamic load (1.5A-10A).

III. Dynamic Voltage Scaling System

A. DVS Overview

A simplified closed-loop DVS system is shown in Fig. 8. [3], [14]. A Voltage Controlled Oscillator (VCO) generates f_{VCO}, which is proportional to the critical path delay of the VLSI core [16] over process and temperature changes. A clock-scheduling algorithm inside the VLSI chip produces the reference clock f_{ref}. A controller provides a Pulse Width Modulated (PWM) signal to the DC/DC converter to regulate V_{DD} and match f_{VCO} to f_{ref}. This feedback loop ensures that V_{DD} and P_{dyn} in eq. (2) are minimized over the entire range of f_{ref}.

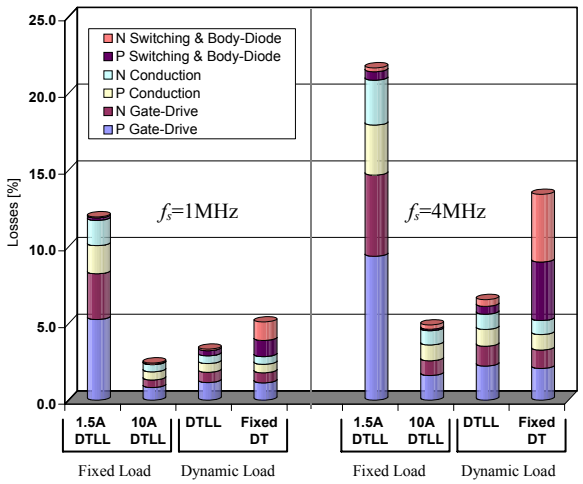

Fig. 6. On-Chip losses with DTLL/fixed dead-time. V_o=1.3V, devices optimized @10A, for 1 and 4MHz.

B. Fully Digital Closed-Loop Controller

An entirely digital controller is well suited to the DVS feedback loop in Fig. 8, due to the inherently digital nature of the clock inputs and PWM output. Furthermore, a fully digital controller can be integrated into the VLSI chip itself as in [2], where it can benefit from the power savings of DVS. Two options for a DVS controller are as shown in Fig. 7. In both cases, pulses from f_{ref} and f_{VCO} are accumulated over the period of f_{loop}. The signal $d[n]$ represents the control output that is converted into a PWM signal using a comparator that has one of its inputs

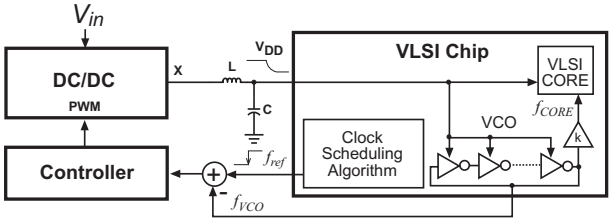

Fig. 8. Simplified block diagram of DVS feedback loop.

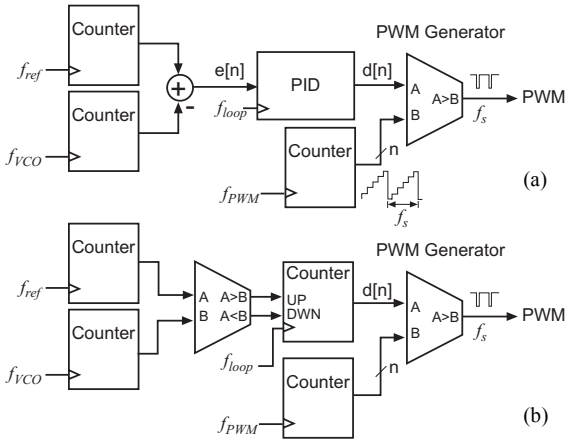

Fig. 7. (a) DVS controller using digital PID and (b) non-linear bang-bang controller.

connected to a free-running digital ramp clocked at f_{PWM}. The resolution of the digital ramp, n determines the switching frequency, f_S:

$$f_s = f_{PWM} \cdot 2^{-n} \tag{9}$$

The non-linear bang-bang controller as shown in Fig. 7 (b) simply increments/decrements the control signal $d[n]$ using a counter, depending on the sign of the error signal. This non-linear technique was demonstrated by [15] and shown to achieve good steady-state performance, yet the transient response is very poor since the PWM can only be incremented once per period of f_{loop}, regardless of the error between f_{loop} and f_{VCO}.

An alternate controller, as shown in Fig. 7(a), uses a digital PID regulator that is fed by the frequency error signal $e[n]$. A detailed implementation of this scheme for DVS, as well as a variable frequency controller is presented in [16]. The digital PID controller has the following characteristics:

$$d[n] = K_P \cdot e[n] + K_I \cdot \sum_{i=0}^{n} e[i] + K_D \cdot \left(e[n] - e[n-1]\right) \tag{10}$$

where K_P, K_I, and K_D represent the proportional, integral and derivative gains of the controller, respectively. A simple, digital implementation of this control law is presented by [16], and can achieve superior dynamic performance with properly selected PID coefficients. This scheme is therefore preferable for the dual-mode DVS system, as verified experimentally in Section VI.

IV. Dual Mode DC/DC Converter

Relying solely on the DVS feedback loop in Fig. 8 for power supply regulation as proposed in [7] has several important drawbacks. Firstly, the power consumed by the digital controller can be quite significant, due to the presence of the high frequency clocks f_{VCO} and f_{PWM} in the frequency counter and PWM generator, respectively. These clocks are typically in the several hundred MHz range. A clever variable loop-frequency scheme proposed by [16] helps to alleviate this power constraint. More importantly, the digital loop can simply not deliver the high dynamic response as a well-compensated analog current-mode controller, especially in the case of the bang-bang DVS scheme. Furthermore, f_s cannot easily be pushed beyond several MHz, as required for passive component miniaturization. This is due to fact that the digital PWM generator would require a highly unpractical f_{PWM} of 1.28GHz to achieve f_s= 5MHz with an 8-bit resolution. Reducing the resolution would only deteriorate the steady state tracking. An attractive solution, shown in Fig. 9, periodically uses DVS loop to update the voltage reference for the ZVS-QSW current-mode loop when the scheduling software asserts a new reference frequency. The requirements for the DVS loop can be relaxed to reduce complexity and power consumption. When temporarily operating in DVS mode, the DTLLs is reset and a fixed digital dead-time is used to avoid cross-conduction while

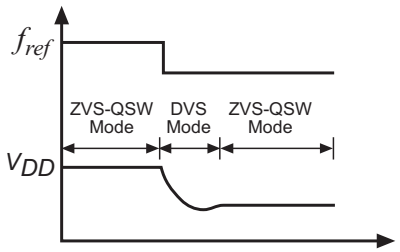

Fig. 9. Representation of a dual mode controller. The DVS loop is only used periodically to update the voltage reference for the ZVS-QSW loop when a new reference frequency is asserted.

the power stage operates as a synchronous buck converter. In the next sections, silicon implementation and experimental results are presented for a ZVS-QSW test chip operating in both modes.

V. Silicon Implementation

A ZVS-QSW controller chip, as show in Fig. 10 was implemented using TSMC's 0.18µm CMOS process to demonstrate the DTLL functionality. The block diagram of this controller chip is as shown in Fig. 11. In addition to realizing the circuit blocks depicted in Fig. 3(b), this chip also includes an 8-bit programmable digital delay line for setting fixed dead-times and a digital RAM file containing calibration data. Various DTLL parameters, such as the

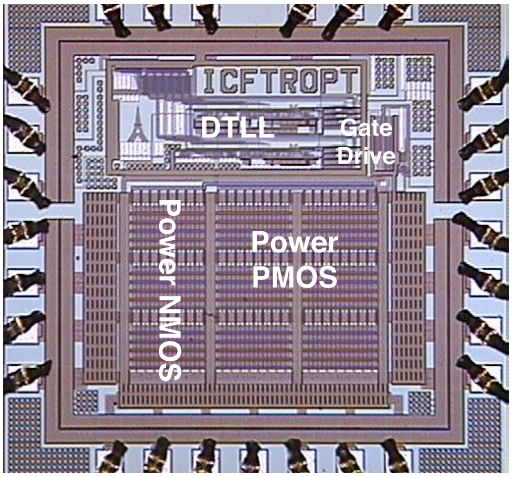

Fig. 10. A micrograph of the 0.18µm CMOS integrated ZVS-QSW DC/DC convreter chip. Die area is 1.56mm^2.

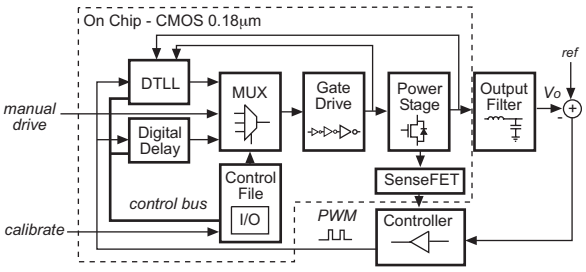

Fig. 11. Block diagram of the ZVS-QSW buck converter chip with integrated DTLLs.

$Comp_{VDS}$ offsets and the one-shot thresholds can be digitally trimmed. Both DTLL blocks can generate delays of up to 50ns. The scaled-down power stage has a nominal output of 0.2A with V_{in}= 2V and output voltage, V_o between 0.5 and 1.8V.

VI. Experimental Results

A. Soft-Switching Converter

Using the digital delay line to generate longer than ideal dead-times, body-diode conduction is evident, as shown in Fig. 13. However, with properly regulated dead-times, body-diode loss can be eliminated as shown in Fig. 14. The switching waveform is f_s=5MHz. The benefit of the dead-time error rejection and true soft-switching is verified by the measured efficiency of the ZVS-QSW converter with different inductor sizes (see Fig. 12). The measured performance for the ZVS-QSW chip is summarized in Table 1. A peak efficiency of 82% is achieved at 5MHz. The efficiency of above 75% is maintained until the conduction losses of the MOSFET switches start to dominate. The efficiency would be greatly improved with optimized power MOSFETs, which are unavailable in the low voltage process.

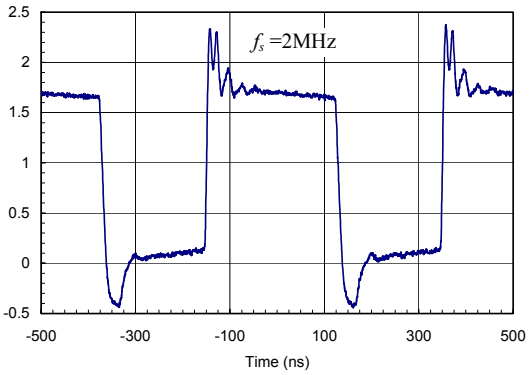

Fig. 13. Measured voltage waveform at node *X* of the ZVS-QSW converter. Manual gate-drive timing is used to show the body-diode conduction.

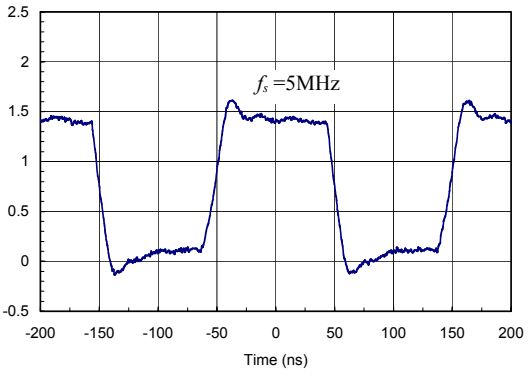

Fig. 14. Measured voltage waveform at node X of the ZVS-QSW converter. Proper gate-drive timing eliminates body-diode conduction after the resonant transitions.

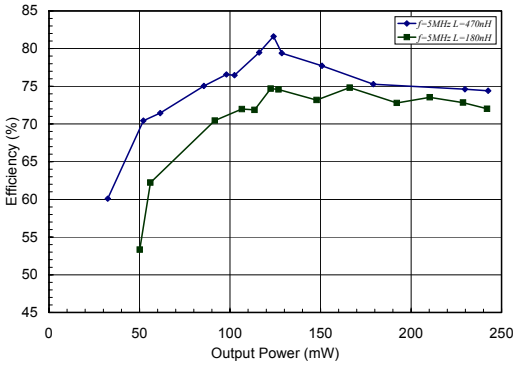

Fig. 12. Measured efficiency of the experimental ZVS-QSW converter for V_{in}=2V, V_o=1.4V.

TABLE 1
ZVS-QSW Chip Specifications

Technology	0.18μm Mixed-Signal CMOS
Input voltage	2V
Nominal output voltage	1V
Maximum dead-time	50ns
Die Area	1.56mm^2
DTLL power consumption	4.5mW
Peak efficiency	82%
Switching frequency	5 MHz
Output inductance	470nH
Output capacitance	6μF

B. DVS System

An experimental DVS system was developed a using state-of-the-art XC2C256 1.8V Complex Programmable Logic Device (CPLD) from Xilinx, as shown in Fig. 15. The ZVS-QSW is configured to have fixed dead-times when running in DVS mode, as explained in Section IV. Eight 8-bit Multiply-Accumulate (MAC) DSP blocks are synthesized, along with a random data generator, to evaluate the power savings of DVS. The MAC units can operate from 91 MHz to 141 MHz at V_{DD} = 1.35V and V_{DD} = 1.8V, respectively. The measured power saving for the MAC is shown in Fig. 16, The DVS loop of Fig. 15 is implemented using a ring oscillator as a VCO and digital DVS controller that generates the PWM command signal $d[n]$.

The reference frequency, f_{ref} can be toggled externally to evaluate the transient performance of the DVS loop. The transient performance of the experimental DVS system with a bang-bang and PID controller are shown in Fig. 17 and

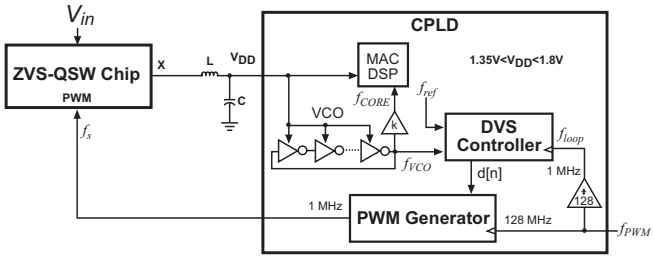

Fig. 15. Implementation of the DVS system using a XC2C256 Xilinx CPLD. The CPLD can function with a core voltage between 1.35V and 1.8V.

Fig. 18, respectively. The PID loop achieves a superior settling time of 22µs for the maximum V_{DD} step, compared

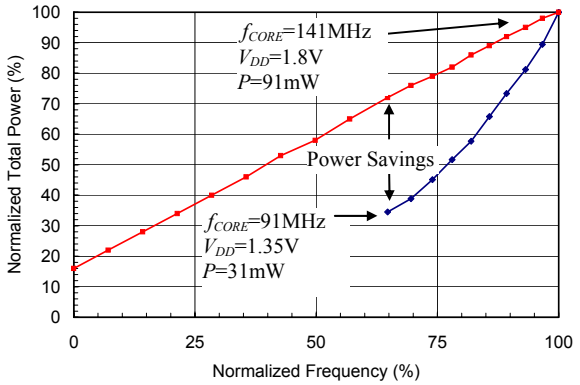

Fig. 16. Measured power savings for the MAC DSP module using the DVS scheme.

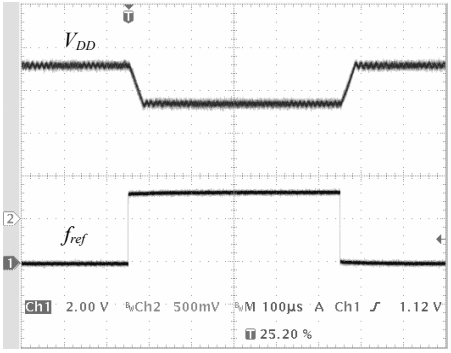

Fig. 17. Measured V_{DD} waveform with the bang-bang DVS controller. V_{DD} is scaled between 1.8V and 1.35V in 36µs. The lower waveform represents the step in f_{ref}.

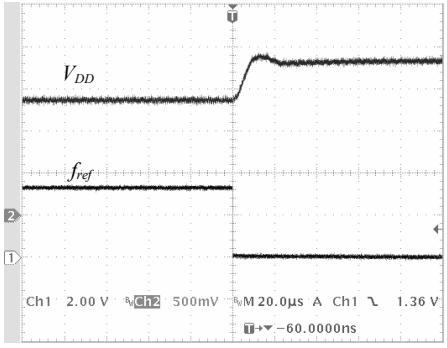

Fig. 18. Measured V_{DD} waveform with the digital PID controller. V_{DD} is scaled between 1.8V and 1.35V in 22µs. The lower waveform represents the step in f_{ref}.

to the bang-bang controller, which settles in 36µs.

VII. CONCLUSION

Conventional DC/DC topologies used to power modern VLSI circuits cannot satisfy future demands for shrinking voltages, rising frequencies, tighter regulation and high efficiency. Zero-Voltage-Switching can be applied to the Quasi-Square-Wave buck converter to eliminate switching losses, as long as the dead-times are adjusted in real-time to track load changes. This work demonstrates the feasibility of analog Dead-Time-Locked-Loops in a low voltage application for achieving fast dead-time error rejection and low steady-state switching losses. The ZVS-QSW chip is also capable of operating in Dynamic Voltage Scaling applications, simply by applying fixed dead-times during the DVS loop operation.

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