On-Chip PLL-Based Methods for Synchronizing Active Switches Across the Isolation Boundary in Dc-Dc Converters

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Abstract—Digital isolators are widely used in isolated power converters for transmitting high-frequency gating pulses. Optoisolators generally suffer from low reliability, while emerging RF-based isolators are expensive and power-hungry. In this work, two Phase-Locked-Loop (PLL) based synchronization schemes are introduced and demonstrated to operate a bidirectional Dual-Active-Bridge (DAB) dc-dc converter. The proposed Digital Isolator Sensing (DIS) scheme utilizes a miniature air-core pulse transformer for synchronization and data communication, while the Power Transformer Sensing (PTS) scheme eliminates the need for any digital isolator for synchronization by using the power transformer. The application of DIS scheme can be extended to any topology that requires active switches on both sides of the isolation boundary, whereas the PTS scheme is designed for the DAB converter. In both schemes, the reference clock is generated on the secondary-side controller, and sensed indirectly on the primary-side. A PLL with a 100 MHz delay line, precise 12-bit phase-shift control module, and high-frequency transceiver are implemented on-chip in a 0.18 μm 80V BCD process, and are used to control an off-chip DAB power stage.

I. INTRODUCTION

There is a growing demand for bidirectional power-flow capability and four-quadrant operation in Micro-Inverters (MIV) [3]. Multi-port MIVs with integrated storage, which is typically realized with a battery [4], [5] or super-capacitor [3], have been proposed for reactive power support and off-grid operation as well as active power smoothing [3]. Bidirectional EV charger topologies with Vehicle-to-Grid (V2G) capability can provide ac grid support using the on-board battery during peak load demand [6], [7].

A bidirectional MIV, as shown in Fig. 1(a) [7], requires active devices on both sides of the transformer in the dc-dc stage. Certain unidirectional dc-dc topologies, such as the LLC converter, may also be designed with active switches on both sides of the isolation for improved efficiency [8]. As the switching frequency is scaled up for improved power density in modern converters, driving multiple switches on both sides of the transformer with precise timing becomes a major challenge. Low-frequency communication is also required between the dc-dc and dc-ac stages for tasks such as start-up, fault-handling and feedforward control loops, hence the need for additional digital isolators. Opto-isolators are commonly used, however they suffer from poor matching, relatively long delays (typically ≥15 ns) and short life-time at high temperature [9], [10]. More recently, digital isolators and isolated gate-drivers based on miniaturized magnetic components or capacitive coupling either on the PCB [11] or on-chip [12]–[16] have addressed some of these shortcomings, while offering a high level of integration. An isolated gate-driver architecture with off-chip magnetics is proposed in [15], [16]. Digital isolators and drivers typically modulate the PWM signal with a carrier in the range of tens of MHz to several GHz in order to reduce the size of the isolation passive components [15], [16]. They require precise mechanical alignment between primary and secondary-side coils. The cost of this technology is typically high, due to multi-die packages or high isolation ratings required for the process technology, as well as the cost of extra components and board space. These isolators are also susceptible to Electromagnetic Interference (EMI) issues and consume nearly as much power as the gate-driver itself. Moreover, the driver cost scales with the number of active switches driven from the opposite side of isolation.

This work presents the first phase in a long-term project...
to monolithically integrate the power transistors, gate-drivers, digital controller and the digital isolation capability in a BCD technology for optimized cost and performance. In this paper, two alternative synchronization schemes are demonstrated on-chip to eliminate the need for using one isolator per transistor:

1) The Power Transformer Sensing (PTS) scheme relies on extracting the switching signal on the secondary-side directly from the reflected voltage across the power transformer, and reconstructing the driving waveforms accordingly on the primary side. The PTS was first reported in [17] with an Field Programmable Gate Array (FPGA) and discrete components.

2) The Digital Isolator Sensing (DIS) scheme, where the switching information is encoded in the data packets sent through a miniature high-frequency Galvanically Isolated (GISO) transceiver.

In both schemes, the active devices on the secondary-side of the dc-dc stage are driven by the dc-ac stage controller, as shown in Fig. 1(b), and a Phase-Locked-Loop (PLL) is used for clock recovery. While both schemes are compatible with a variety of isolated topologies, this paper is focused on the soft-switching Dual Active Bridge (DAB) converter with simple Phase-Shift-Modulation (PSM), as shown in Fig. 2(a). Both bridges operate with a duty cycle, $D$, of 50% and the power flow is given by:

$$P_{DAB} = \frac{V_{PV} V_{bus}}{n \omega_s L_{DAB}} \phi \left( 1 - \frac{\phi}{\pi} \right), \quad (1)$$

where $n$ is the transformer turns ratio, $L_{DAB}$ is the DAB inductance, which is the sum of transformer’s leakage inductance and the external inductance, $\phi$ is the phase-shift between the two bridges, and $\omega_s = 2\pi f_s$, where $f_s$ is the switching frequency.

This paper is organized as follows. The PTS and DIS schemes are discussed in detail in Section II. The wide-range PLL implementation is presented in Section III, while the performance of both of the synchronization schemes are demonstrated on an external DAB converter in Section IV. The concluding remarks are provided in Section V.

II. SYNCHRONIZATION SCHEMES

A custom IC was developed in a 80V 0.18$\mu$m BCD technology to demonstrate and compare the two synchronization schemes on a DAB converter. The high-level architecture is shown in Fig. 2. Synchronization can be achieved using either a high-frequency isolated communication channel (DIS mode, activated when $mode = 1$), or sensing through the power transformer (PTS mode, activated when $mode = 0$).

A. Digital Isolator Based Synchronization and Communication

The DIS scheme utilizes a single digital isolator to achieve two purposes: 1) synchronize both controllers on opposite sides of the isolation, and 2) to transmit data between the controllers, as needed for control and fault handling. A low-power, high-speed GISO transceiver was developed to demonstrate the DIS scheme. High-frequency modulation, up to 100 MHz, is adopted to reduce the air-core transformer size, which can also be implemented using PCB traces. The high-speed GISO transceiver is designed with 1.8V devices and transmits a differential low-amplitude signal (typically $\geq 50$ mV) across an on-chip 20 $\Omega$ termination resistor, with a common-mode voltage of 0.9 V, as shown in Fig. 3. The critical GISO
parameters, including the driver signal-swing and the receiver hysteresis are digitally programmable via the SPI interface.

A typical GISO communication packet includes two main components, as shown in Fig. 4(a). The first period of the packet is a preamble and serves as the reference clock, \texttt{clk.ref.} for the PLL. The PLL is enabled during the preamble period. The bits following the preamble contain the data and can be recovered using a variety of well-known methods, such as Manchester coding [18]. The start-up sequence in DIS mode is shown in Fig. 4(b). The PLL is put into a \texttt{hold} state, where the phase detector is disabled in between consecutive preamble periods, as shown in Fig. 4(b). The Voltage-Controlled-Oscillator (VCO) is therefore free-running during this time. It is necessary to maintain regular communication in order to guarantee an acceptable PLL drift. Furthermore, the PLL is placed in the \texttt{hold} state for 3\% of the switching period, \texttt{T.s}, during power-transistor switching, in order to minimize the disturbance on the synchronizing operation. The locked output of PLL, \texttt{clk.sync}, is used as the main system clock in order to generate the phase-shifted PWM signal, \texttt{clk.sync}, to control the primary-side bridge of the DAB converter. The phase-shift is achieved by using a combination of delay-line and a counter for fine and coarse delay adjustment, respectively, as shown in Fig. 3. The phase-shift resolution is \( k + m \), where \( k \) and \( m \) are the number of delay elements and counter bits respectively; \( k = 5 \) and \( m = 7 \) are adopted in this work, which results in a phase-shift resolution of 300 ps.

\subsection{B. Synchronization by Power Transformer Sensing and Communication}

Using the PTS scheme, synchronization is achieved by sensing the reflected voltage across the power transformer, hence eliminating the need for any digital isolator. The PTS scheme was first reported in [17] using discrete components, where it was also shown that low-frequency unidirectional communication can be achieved through switching frequency modulation. The reflected switching waveform on the secondary side is detected using a comparator, and the resulting waveform, \texttt{comp}, is fed as \texttt{clk.ref} to the PLL, as shown in Fig. 3. When locked, \texttt{clk.sync} is in phase with the secondary-side switching and can thus be phase-shifted by \( \phi \) in order to generate four PWM signals, \( C_{1-4} \). The resulting power flow is given by (1). The start-up sequence is illustrated in Fig. 5. Once the secondary controller activates the secondary-side bridge, the switching action is detected on the primary side and PLL is enabled. The charge-pump output voltage, \( V_c \), is regulated in order to synchronize \texttt{clk.sync} to \texttt{clk.ref}. Once PLL locking is achieved, the converter can start-up by driving \( C_{1-4} \).

\section{III. PLL Implementation}

In order to achieve synchronization across an isolated boundary, the system must be able to lock to an external clock source. The synchronization is achieved by using an on-chip PLL, as shown in Fig. 3. The PLL consists of a
VCO, clock divider, loop-filter, and phase detector blocks, as in a conventional architecture [19]. For this application, it is designed to lock over a very wide frequency range, from 500 kHz to 100 MHz, using digitally configurable clock divider and loop-filter in order to accommodate both PTS and DIS schemes.

The VCO is comprised of a ring of 32 current-starved inverters with voltage-controlled delay. The simulated frequency of the delay-line, $f_{dl}$, versus the inverter bias voltage, $V_c$, is shown in Fig. 6. A frequency range of 80-120 MHz is achieved for $V_c = 0.8-1.2$ V, in which the VCO is quite linear with a slope of 105 MHz/V. The maximum measured frequency range is lower due to the parasitics. The bias voltage $V_c$ is generated from an analog loop-filter which consists of three on-chip passive elements, $R_1$, $C_1$, and $C_2$. All these elements are implemented as programmable passive banks with $2^{14} = 16384$ different combinations, as shown in Fig. 7(a), and occupy a total space of 260 $\mu$m x 400 $\mu$m on-chip.

The charge-pump current, $I_{pump}$, is programmable in the range of 20-200 $\mu$A. This current is either pumped in or out of the loop-filter, depending on the $UP$ and $DOWN$ signals, generated by the phase-detector block. The phase-detector compares the rising edges of an external reference clock, $clk_{ref}$, and the internal synchronized clock of the delay-line, $clk_{sync}$, as shown in Fig. 7(b). It consists of two Flip-Flops and a NAND gate. A comparator is used in order to pre-charge the voltage $V_c$ to $V_c,ref$, a programmable value which is set within the VCO’s linear range.

### IV. EXPERIMENTAL RESULTS

The fabricated DAB synchronization IC is shown in Fig. 8 and measures $2.5\times4.5$ mm$^2$. The chip was tested with a 50 W discrete DAB converter, with the parameters listed in Table I. The start-up process, as well as steady-state operation in the DIS and PTS modes, are shown in Figs. 9 and 10, respectively.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency, $f_s$</td>
<td>500</td>
<td>kHz</td>
</tr>
<tr>
<td>DAB Inductance, $L_{DAB}$</td>
<td>6.9</td>
<td>$\mu$H</td>
</tr>
<tr>
<td>Primary-Side Voltage, $V_{in}$</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>Bus Voltage, $V_{bus}$</td>
<td>90</td>
<td>V</td>
</tr>
<tr>
<td>Transformer Turns Ratio, $n$</td>
<td>3.5</td>
<td></td>
</tr>
<tr>
<td>Nominal Power, $P_{DAB}$</td>
<td>50</td>
<td>W</td>
</tr>
</tbody>
</table>
In both modes, $V_c$ is well regulated to its final value in steady-state. With GISO frequency equal to 50 MHz ($clk_{ref} = 50$ MHz), it takes 18 GISO packets for the PLL to settle in DIS mode, while the settling time is 275 $\mu$s in PTS mode ($clk_{ref} = 500$ kHz). The PLL is constantly active in PTS mode, except for when $hold$ is high due to PWM edges. The PLL is put in the $hold$ state in between the data packets in the DIS mode. The DAB current waveform in the DIS and PTS modes are shown in Fig. 11(a), (b), respectively. The DAB current waveform in Fig. 11(a) is captured by activating the persistence mode of the oscilloscope, and shows very low PLL jitter in DAB operation in the DIS mode. The delay-line, which is the most power hungry part of the PLL, consumes 0.846 mW on average when oscillating at the maximum frequency of 100 MHz. The GISO transmission consumes 27 mW in the transmitter and 63 $\mu$W in the receiver when operating continuously at 100 MHz. The average power consumption of GISO block in DIS mode can be much lower based on the packet transmission frequency.
### Table II
**Comparison of Driving Schemes in Isolated Converters**

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Conventional</th>
<th>PTS</th>
<th>DIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Communication Capability</td>
<td>No</td>
<td>Yes (unidirectional)</td>
<td>Yes</td>
</tr>
<tr>
<td>Continuous Communication</td>
<td>No</td>
<td>Yes (required to avoid PLL drift)</td>
<td>Optional</td>
</tr>
<tr>
<td>PLL Operation</td>
<td>None</td>
<td>Low frequency</td>
<td>High frequency</td>
</tr>
<tr>
<td>Absolute Phase Reference</td>
<td>N/A</td>
<td>Available through comp</td>
<td>Communicated</td>
</tr>
<tr>
<td>Number of Digital Isolators Required for Driving (DAB)</td>
<td>4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>High</td>
<td>Limited by transformer leakage inductance</td>
<td>Low</td>
</tr>
<tr>
<td>Power Converter Topology</td>
<td>No limitation</td>
<td>Yes (transistor)</td>
<td>No limitation</td>
</tr>
<tr>
<td>High Voltage Comparator</td>
<td>None</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

![Fig. 11. Synchronized DAB converter waveforms in the (a) DIS mode with continuous GISO\textsubscript{in} input clock, and (b) PTS mode (I\textsubscript{L,DAB}: 5A/div).](image)

**V. Conclusions**

This work presents the first on-chip demonstration of both PTS and DIS synchronization schemes for isolated dc-dc converters. While both PLL-based schemes are superior to the conventional approach of using one opto-isolator per transistor, they have important differences: DIS is more expensive and consumes more power than PTS, since it requires an off-chip air-core transformer for the GISO, however it is much more flexible in terms of data communication and power topology.

A qualitative comparison of the PTS and DIS schemes is provided in Table II. The PTS scheme eliminates the need for any digital isolator, while the DIS scheme requires one digital isolator. However, the application of PTS is limited to certain topologies, while DIS scheme can be applied to a variety of isolated topologies. The PLL in PTS scheme is designed to lock to a low frequency compared to the DIS scheme. This shrinks the size of the on-chip PLL for the DIS scheme; however, the power consumption is higher. In general, both of these schemes are superior in cost and performance to the conventional approach of using one digital isolator per transistor in addition to the data channel. The developed IC in this work is promising for future use in isolated dc-dc converters with high switching frequencies beyond 1 MHz.

**VI. Acknowledgement**

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**References**


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