A Two-Chip Quasi-Resonant Buck Converter with a 700V Power-Stage and Mixed-Signal Current-Mode Control

Masafumi Otsuka and Olivier Trescases
Department of Electrical and Computer Engineering
University of Toronto
10 King's College Road, Toronto, ON, M5S 3G4, Canada
E-mail: masafumi.otsuka@utoronto.ca

***Abstract*— In sensor-node applications, the auxiliary power is drawn from the ac mains to supply the mixed-signal sensor components. There is therefore a need for low-cost, sub-1W, miniature non-isolated ac-dc down-converters. In this work, a new two-chip architecture is proposed to implement a high-voltage quasi-resonant buck converter with peak current-mode control. The current and voltage control loops are implemented in the high-side (HS) and low-side (LS) IC, respectively. Each IC includes a 700V power transistor, sensing and control circuits. The LS IC transmits the digital peak current command, along with mode selection information, to the HS IC using a low-power 20 MHz isolated communication interface. The architecture achieves a peak simulated efficiency of 85.6% when converting from 339 V to 12 V and allows the size of the input filter to be greatly reduced due to the current-mode operation. State-of-the-art UHV BCD technologies offer a unique opportunity to increase the level of integration and reduce the system cost in the targeted sensor node applications, despite the relatively poor figure-of-merit of the HV devices compared to discrete Silicon super-junction or GaN alternatives.**

Keywords: High Voltage DMOS, Soft-Switching, Non-isolated DC-DC, Digital Control, Off line converter.

I. Introduction

Future green buildings will offer a drastically reduced energy footprint [1], by leveraging a wide range of new monitoring and control techniques that rely on distributed sensors. These sensors may be either wired to the ac power network or operate wirelessly using power harvesting. In wired applications, power can be drawn from the ac mains, which creates the need for low-cost, sub-1W, non-isolated ac-dc down-conversion to supply the mixed-signal sensor components. In applications requiring isolation, the flyback topology is most popular in this low-power range due to its simplicity and low component count, as shown in Fig. 1(a) [2]–[4].

If isolation is not mandatory, the cost can be further reduced by using a simple buck converter, as shown in Fig. 1(b). In this case the high-voltage (HV) buck converter is supplied directly by the rectified ac voltage. The output voltage regulation is performed using variable-frequency hysteretic control. Since the controller is implemented with a ground referenced to the switch node, LX, the output voltage can only be measured indirectly through a diode when the main switch is off [5]. This control approach is simple but has a relatively poor accuracy and the slow dynamic response. In turn, this requires the use of a large input capacitor to filter ac line disturbances. Alternatively, using current-mode control can drastically improve the rejection of line disturbances and reduce the input capacitor size. Implementing both current and voltage sensing on-chip in this high-voltage, low-cost application is a major challenge. While emerging Gallium Nitride (GaN) based converters [6] are are very promising for increasing the switching frequency and power density, at this time the cost remains prohibitive for this low-power application. A silicon implementation also allows a higher level of integration with the availability of monolithic high-voltage power stage, driver and control circuits.

In this work, a new two-chip architecture is proposed, where an analog peak-current control loop is implemented in the high-side (HS) IC, while an accurate outer voltage loop is implemented digitally in the low-side (LS) IC. The converter uses soft-switching to achieve both high efficiency and high power density. Using the two-chip architecture accommodates the use of high-voltage low-side power transistors in the half-bridge and facilitates the implementation of peak current-mode control for fast transient response.

The paper is organized as follows. The proposed dc-dc converter control scheme is outlined in Section II. The detailed IC implementation is described in Section III. Simulation and results are reported in Section IV. Finally, conclusions are presented in Section V.

II. Two-Chip Soft-Switching HV IC Architecture

The high-level architecture of the proposed two-chip HV synchronous buck converter is shown in Fig. 2(a). The converter consists of a HS and LS IC, each having a 700V-rated power transistor. The controller senses the LX node voltage to turn on and turn off each switch respectively, as shown in Fig. 2(b). A two-chip approach is needed since a BCD technology with a competitive high-side power DMOS is generally not available in this voltage class. The HS chip is powered using a conventional bootstrap scheme with an off-chip diode. The complete mixed-signal current-mode control scheme is shown

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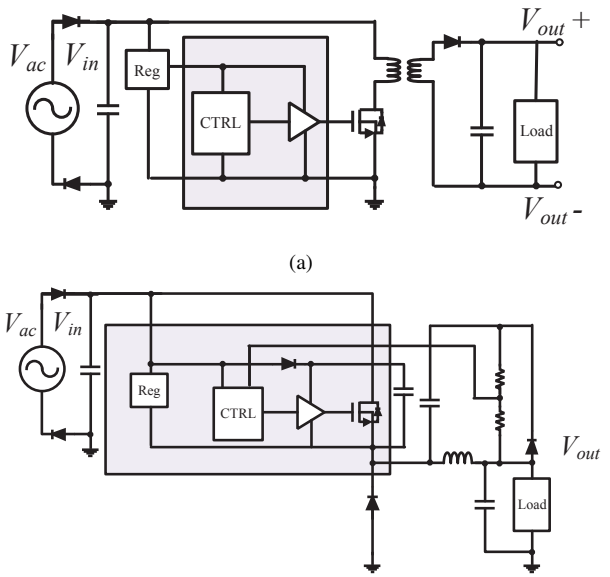

Fig. 1. (a) Flyback converter and (b) high-voltage buck converter for generating the supply voltage directly from the ac mains in low-power sensor node applications.

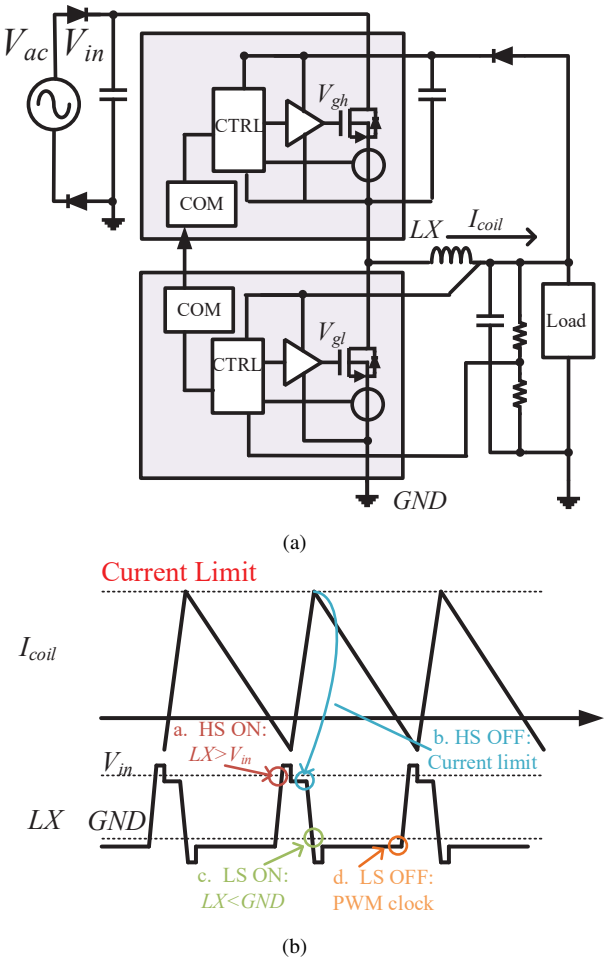

Fig. 2. (a) Two-chip control architecture. (b) Basic control waveforms in full soft-switching mode.

in Fig. 3. The output voltage regulation is performed by the LS chip, which samples V_{out} using a Successive Approximation (SAR) ADC and transmits a peak current command to the HS IC using a low-cost isolated digital communication interface. Current sensing is implemented in the HS IC using a senseFET approach.

A. Operating Modes

The converter is designed to operate in three modes, as described below. The mode selection is based on the output voltage and load current.

1) Full Zero-voltage-switching Mode (Full-ZVS): As shown in Fig. 4, a negative inductor valley current is used to achieve ZVS turn-on. Automatic dead-time adjustment is implemented to improve the efficiency. The HS IC delays turn-on of the HS DMOS until LX crosses V_{in}. Similarly, the LS IC delays turn-on of the LS switch until LX swings below ground. Each IC is thus responsible for one ZVS turn-on event, without the need to transmit any timing edges from one IC to the other. This mode has the lowest total switching losses. And the Frequency is fixed based on the internal PWM oscillator.
2) Partial Zero-voltage-switching Mode (Partial-ZVS): This mode is used when the conduction loss penalty for operating in full ZVS outweighs the reduction in turn-on switching loss. As shown in Fig. 5, the valley current is positive and the LSF IC must transmit the timing edge in each cycle to turn on the HS switch.
3) Current-Mode Pulse-Frequency Modulation Mode (PFM): PFM mode is implemented in order to improve the light-load efficiency. As shown in Fig. 6, the main difference between PFM and Partial-ZVS mode is the variable frequency turn-off timing of the LS switch. In this case, when the LS IC detects that V_{out} has fallen below the limit, V_{min}, it transmits the current-command value to HS switch. The peak current is fixed in PFM mode. The controller in the LS IC performs diode emulation; a comparator is used to detect the inductor zero current crossing conditions before turning off the LS switch.

B. Negative Current Condition

In order to achieve full-ZVS, such that LX reaches V_{in} during the resonant transition, the following condition must be satisfied

$$E = \frac{1}{2} L I_{vly}^2 > \frac{1}{2} C_x V_{in}^2, \tag{1}$$

where L is inductance, I_{vly} is the inductor valley current value and C_x is lumped switch-node capacitance. Note that

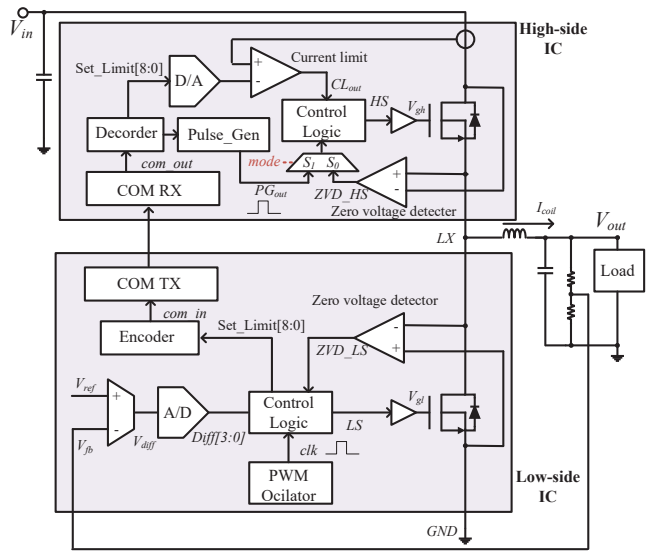

Fig. 3. Detailed control structure; analog peak current-mode control is implemented in the HS IC and digital voltage regulation is implemented in the LS IC.

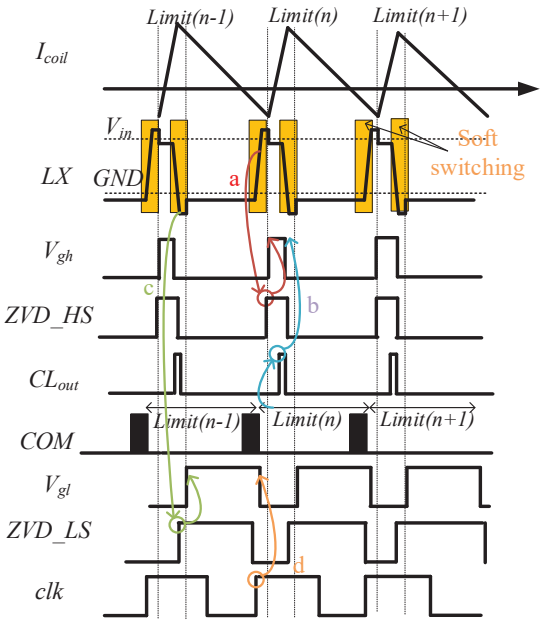

Fig. 4. Ideal converter waveforms and communication packet from LS to HS chip in full ZVS mode.

I_{vly} must be negative for soft-switching. The required valley current must be below

$$I_{vly} = -\sqrt{\frac{C_x}{L}}, \tag{2}$$

in order to resonate the switch node voltage to the input rail and achieve soft-switching. In practice, a more negative I_{vly} compared to (2) is used to reduce the transition time. The relation between the parasitic capacitance and I_{vly} is shown in

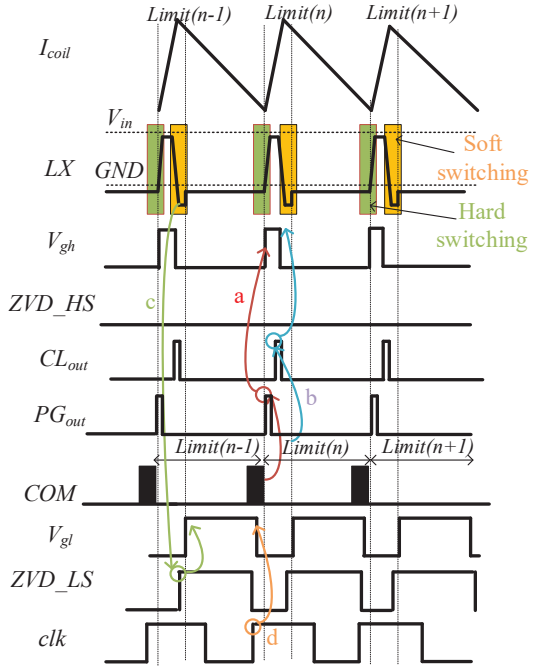

Fig. 5. Ideal converter waveforms and communication packet from LS to HS chip in partial ZVS mode.

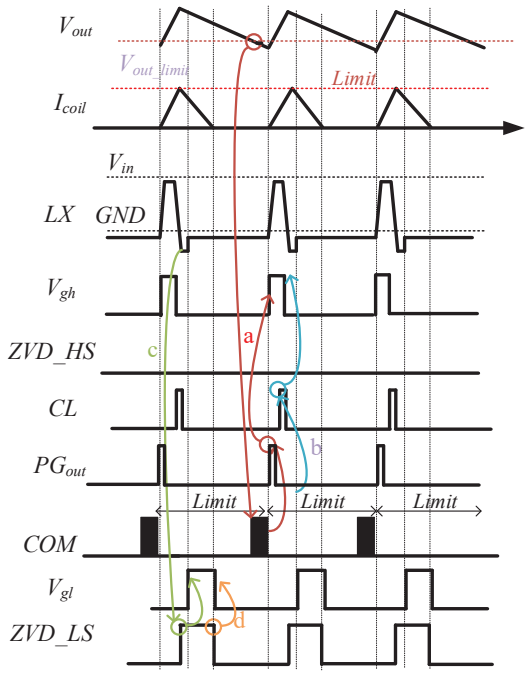

Fig. 6. Ideal converter waveforms and communication packet from LS to HS chip in PFM mode.

Fig. 7. When using a lower inductance, a more negative valley current is needed. In this work a 700V rated on-chip power device is used with a relatively large capacitance, resulting in a high RMS current to achieve soft-switching.

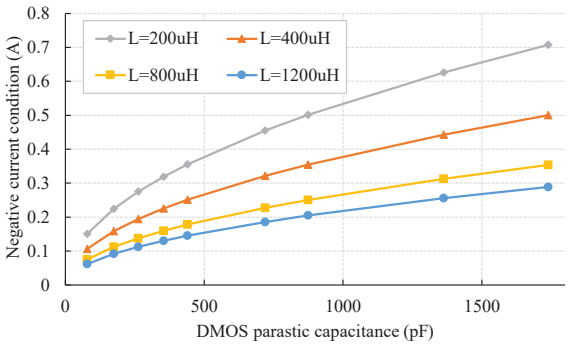

Fig. 7. Minimum valley current required for ZVS mode based on switch node capacitance.

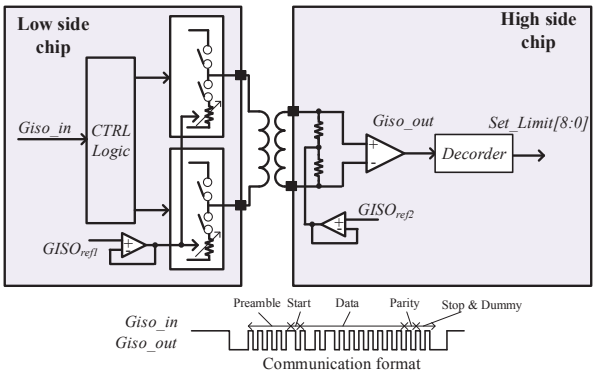

Fig. 8. Isolated communication protocol. The communication from LS to HS IC is implemented solely with low-voltage 0.35μm devices, eliminating the need for a high-voltage level-shifter.

III. Implementation

The IC was designed in Magnachip's 700V 0.35μm BCD technology. To facilitate testing, a single demonstrator IC was designed to include all the functional blocks needed to implement both the LS and HS ICs, as shown in Fig. 3. Each IC can be externally programmed to behave as either a HS chip (current-mode controller and communication receiver) or LS chip (voltage loop regulator and communication transmitter).

A. Isolated Communication Scheme

A simple low-power isolated communication scheme is implemented using the low-voltage 0.35μm transistors to transmit the digital peak current reference value from the LS to the HS chip during each switching cycle. A low-cost air-core transformer fabricated using the PCB traces is used to transmit the low-amplitude differential signal at a frequency of 20 MHz. The transmitter has a programmable differential swing to across the termination resistor in order to optimize the trade-off between power consumption and noise immunity.

Manchester encoding is used for the data packet, as shown in Fig. 8. The receiver includes a regulator to set the common-mode voltage on the receiver coil. The communication format also includes the preamble and the parity bit. In order to increase the system reliability, if a parity error is detected by the HS IC due to a communication failure, the data packet is disregarded. In the event of a communication failure, the current command is retained from the previous cycle. By using this isolation interface, the communication can be achieved reliably without any high-voltage level-shifters or external digital isolators.

B. Stacked DMOS Structure and Current Sense

The structure of power transistor and the current sensing circuit is shown in Fig. 9. The main switch is constructed using a stacked/cascode structure, where a 700V depletion mode device is connected in series with a 20V enhancement mode DMOS. This cascode structure results in a superior overall specific on-resistance compared to the available 700 V enhancement mode DMOS in this technology. This is especially pronounced at low gate-drive voltage, due to the low threshold voltage of the 20V DMOS pair. In addition, the current sensing accuracy in the cascode structure is improved, since the senseFET is constructed using a matched 20V DMOS.

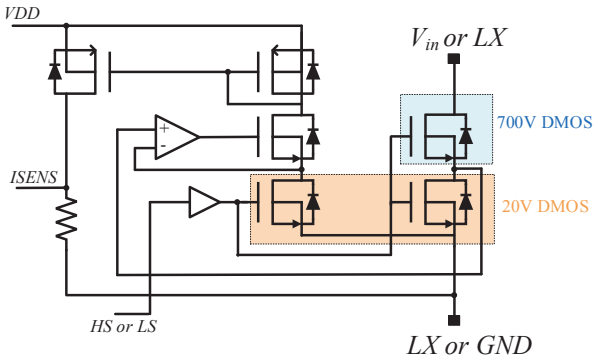

Fig. 9. Stacked power-stage architecture and senseFET current sensing circuit.

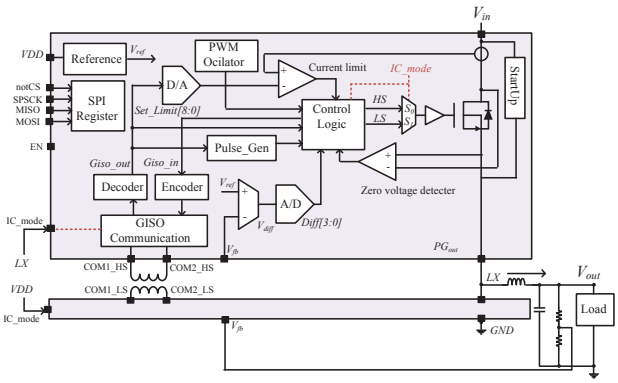

Fig. 10. HVIC architecture; to simplify the testing, one identical IC is designed to fulfil the HS and LS functionality and can be configured accordingly.

TABLE I

DESIGNED CHIP SPECIFICATIONS

Parameter	This Work (3.3V)	This Work (12V)	[5]	Unit
Output Voltage	3.3	12	12	V
SW Frequency	20	15	5-63	kHz
Inductance	1	2	2.2	mH
Input Capacitance	0.4	0.4	4.7	uF
Max Output Power	1	1	2.5	W
Operation mode	PFM, Partial ZVS	Full-ZVS, Soft SS	Hysteric Voltage	

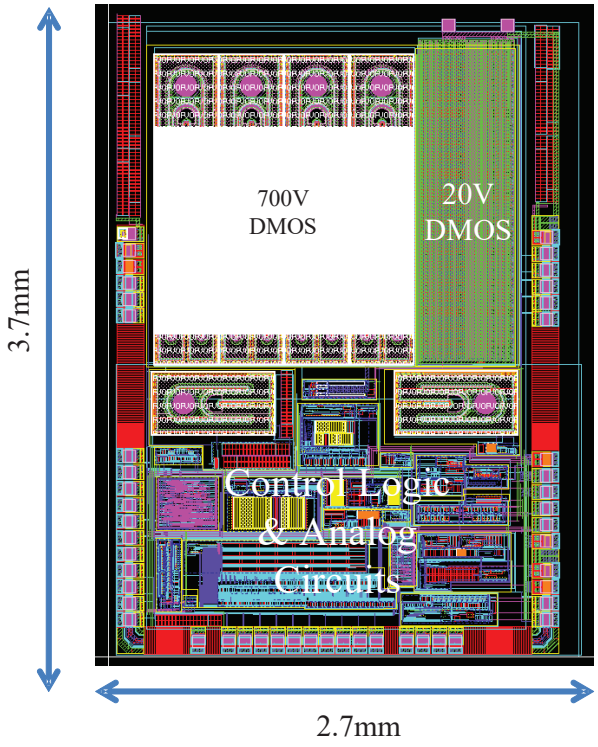

Fig. 11. Chip layout.

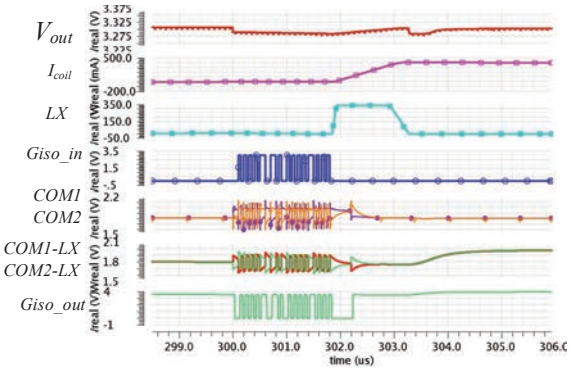

Fig. 12. Simulated communication waveform. Giso-out is the received data stream.

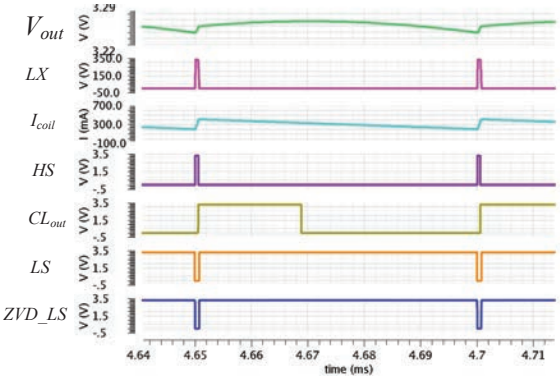

Fig. 13. Simulated partial-ZVS operation for V_{out}= 3.3 V.

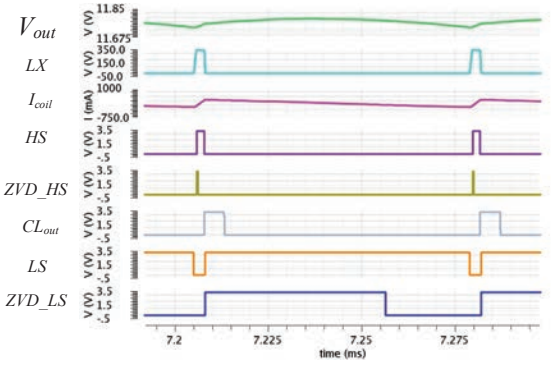

Fig. 14. Simulated full-ZVS operation for V_{out}= 12 V.

IV. SIMULATION RESULTS

To facilitate testing, a single demonstrator IC was designed to include all the functional blocks needed to implement both the LS and HS chips, as shown in Fig. 10. Each IC can be externally programmed to behave as either a HS chip (current-mode controller and communication receiver) or LS chip (voltage loop regulator and communication transmitter). The converter parameters are listed in Table I. The simulated communication waveforms at V_{out} = 3.3 V are shown in Fig. 13 during closed-loop operation. Operation in full-ZVS mode is shown in 14 at V_{out} = 12 V, V_{in} = 240 VAC and an inductor valley current value of 120 mA. The simulated efficiency is shown in Fig. 15. A peak efficiency of 85% is achieved at V_{out} = 12 V and 69 % at V_{out} = 3.3V. PFM mode allows efficiency improvements when operating below 0.4 W.

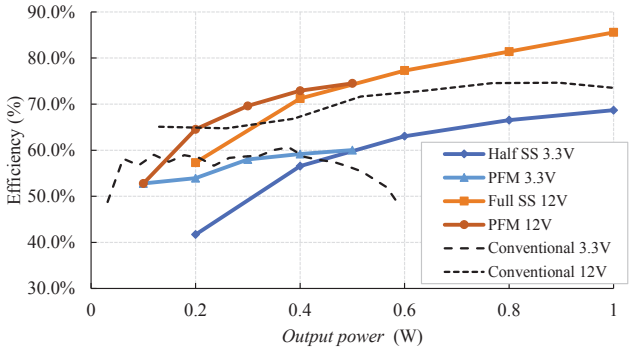

Fig. 15. Simulated efficiency compared to the conventional HVIC in [5].

V. Conclusions

The main contribution of this work is the concept of a high-voltage two-chip half-bridge, where the HS IC operates as a stand-alone current-mode controller and the LS IC regulates the output voltage. The current command is transmitted from the LS to the HS IC using a dedicated isolated interface built entirely out of low-voltage devices. The architecture achieves a peak simulated efficiency of 85.6% when converting from 339 V to 12 V and, more importantly, allows the size of the input filter to be greatly reduced due to the current mode operation. State-of-the-art UHV BCD technologies offer a unique opportunity to increase the level of integration and reduce the system cost in the targeted sensor node applications, despite the relatively poor figure-of-merit of the HV devices compared to discrete Silicon super-junction or GaN alternatives.

References

[1] T. Weng and Y. Agarwal, "From buildings to smart buildings 2014 sensing and actuation to improve energy efficiency," *IEEE Design Test of Computers*, vol. 29, no. 4, pp. 36–44, Aug 2012.

[2] S. Zhao, J. Zhang, and Y. Shi, "A low cost low power flyback converter with a simple transformer," in *Power Electronics and Motion Control Conference (IPEMC), 2012 7th International*, vol. 2, June 2012, pp. 1336–1342.

[3] K.-H. Chen and T.-J. Liang, "Design of quasi-resonant flyback converter control ic with dcm and ccm operation," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 2750–2753.

[4] J.-K. Kim, J.-B. Lee, and G.-W. Moon, "Zero-voltage switching multi-output flyback converter with integrated auxiliary buck converter," *Power Electronics, IEEE Transactions on*, vol. 29, no. 6, pp. 3001–3010, June 2014.

[5] "High voltage switcher for non-isolated ac/dc conversion," Online report, IC Specification, 2005, available http://www.ti.com/lit/ds/symlink/ucc28880.pdf.

[6] S. Mao, R. Ramabhadran, J. Popovic, and J. Ferreira, "Investigation of ccm boost pfc converter efficiency improvement with 600v wide band-gap power semiconductor devices," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, Sept 2015, pp. 388–395.