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Title: A Dynamic Voltage Scaling Controller for Maximum Energy Saving Across Full Range of Load Conditions. (***student paper***)

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A Dynamic Voltage Scaling Controller for Maximum Energy Saving Across Full Range of Load Conditions

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Abstract – **For devices operating mainly in the standby or low power mode, energy saving from dynamic voltage scaling (DVS) is limited due to very poor efficiency of the PWM DC/DC converter operating at light load conditions, resulting in shorter than expected battery life. This paper first presents the design of a DVS controller – realized on a Xilinx CoolRunner 2 CPLD – having a 25 μs worst case transient response and 15 mV average V_{dd} step size across an 1.30-1.90 V range. Next a scheme is proposed in which the DVS controller automatically selects between the PFM and PWM mode DC/DC conversion to realize maximum power saving across full range of load conditions.**

I. INTRODUCTION

The shrinking of minimum feature size and economic benefit of large scale integration has lead to an explosive increase in both power density and total power consumption in modern VLSI circuits. In order to reduce thermal management costs and prevent deterioration in reliability, effective power management is required in today's top-of-the-line microprocessors. Additionally, due the need for extended battery life, power reduction is also essential in a wide range of mobile applications such as wireless communication devices, and portable media players which contain power hungry VLSI circuits.

Power management can be effectively implemented through dynamic voltage scaling (DVS). By varying the supply voltage and clock frequency according to the computation load, the amount of energy consumption only needs to be as high as required to satisfy a desired circuit performance at anytime. Since the dynamic power $P_{dynamic}$ is both a quadratic function of the supply voltage V_{dd} and a linear function of the frequency f, significant dynamic power reduction is possible through DVS:

$$P_{dynamic} = \alpha f C_L V_{DD}^2 \qquad (1)$$

Furthermore, static power – an increasingly significant component of power dissipation in deep submicron technologies – can also be effectively suppressed through DVS [1]. According to a recent research [2], using voltage scaling, significant reduction in sub-threshold and gate leakage current on the order of V_{DD}^3 and V_{DD}^4 respectively was achieved in a 1.2 V, 0.13 μm technology.

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Most existing research on DVS treats the problem of minimizing VLSI circuit energy consumption and DC/DC converter design separately, neglecting the important fact that variation in converter efficiency directly determines the amount of DVS power saving realizable at any given computation load. At high load conditions, the PWM mode DC/DC converter – commonly used for voltage scaling – exhibits efficiency exceeding 80%, but have dismal conversion rate at light load conditions due to switching losses. Since many mobile devices such as cell phone spend a majority of the time operating in the standby mode, poor light-load efficiency leads to limited DVS power saving, and as a result lower than expected battery life. The PFM mode DC/DC converter offers significant improvement in efficiency at light load conditions but performs poorly at high load conditions.

This paper presents the design of a DVS controller in section II, and proposes in section III a scheme in which the controller automatically switches between the PFM and PWM modes to obtain maximum power saving across full range of load conditions.

II. DESIGN OF THE DVS CONTROLLER

A. *Design Considerations*

Transients during voltage scaling must be minimized. Slow down-scaling of V_{dd} leads to excessive non-optimal power dissipation, on the other hand, slow V_{dd} up-scaling causes excessive delay before circuit performance becomes sufficient enough to handle an increase in the computation load. Bad transient behavior can significantly degrade both power saving and circuit performance.

The supply voltage should be scaled in the finest possible increments. The larger the V_{dd} steps are, the less likely minimum energy dissipation will be achieved at a given computation load. Total DVS power saving is inversely proportional to V_{dd} step size.

Additional considerations include controller robustness, stability and overhead power consumption.

B. *Operating Principle and System Topology*

In the simplified DVS system shown in Fig. 1, performance of the VLSI load is measured by a VCO, whose total delay of $1/(2f_{osc})$ is directly proportional to the critical path delay over process and temperature variations [3]. A smart software algorithm is employed to generate the reference frequency f_{ref}. By keeping the difference between f_{ref} *and* f_{osc} equal to 0, the circuit will always operate with the desired performance while consuming the minimum amount of energy. If this difference is positive, then circuit performance is

inadequate and the supply voltage V_{dd} must be increased to compensate. On the other hand if the difference is negative, then an excessive amount of power is being dissipated, so V_{dd} must be scaled down. The PID controller constantly adjusts the supply voltage V_{dd} to ensure matching between f_{ref} and f_{osc}. This voltage control is facilitated by the PWM generator which translates PID compensator output in the form of duty cycles into gating pulses that is then converted to V_{dd} by the buck converter.

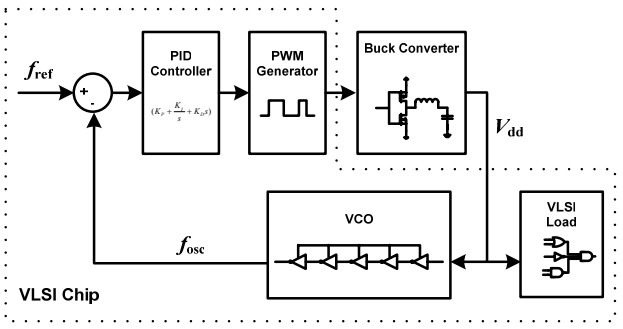

Fig. 1. Block diagram of a simplified DVS system.

C. *S-Domain PID Controller Design*

Preliminary PID coefficient tuning is based on the analog model of the DVS system. The following open-loop transfer function is employed:

$$H_{OL} = K_{PWM} K_{VCO} H_{buck} H_{PID} e^{-sT} \tag{2}$$

The PWM generator and VCO are modeled as the constant gains K_{PWM} and K_{VCO} respectively, while loop delay is accounted for with e^{-sT}. The buck converter transfer function H_{buck} [3] is given by the equation:

$$H_{buck} = \frac{1/LC}{s^2 + \left(\frac{R_s}{L} + \frac{1}{R_p C}\right)s + \frac{1}{LC}\left(1 + \frac{R_s}{R_p}\right)} \tag{3}$$

where the resistances R_s and R_p are the lumped series and parallel quantities, while inductance L and capacitance C correspond to filter parameters. Due to high Q factor of the complex conjugate poles, H_{buck} exhibits significant gain peaking at the LC resonant frequency. To achieve a high bandwidth system that is stable, PID compensation employing pole zero matching is applied. The PID compensator transfer function H_{PID} is given below first in the conventional form and then followed by another formulation that is more suited for P-Z matching:

$$H_{PID} = (K_P + \frac{K_I}{s} + K_D s) = A\left(\frac{s^2 + 2\xi\varpi s + \varpi^2}{s}\right) \tag{4}$$

By setting ω^2 in (4) equal to $1/LC(1 + R_s/R_p)$ as specified in (3) and suitably choosing the value of ξ, cancellation of the buck converter poles is realized in (2). The new H_{OL} is effectively a single pole system which has good stability characteristics. Fine tuning is done by adjusting the gain factor A to achieve the desirable stability margin and bandwidth. However, because there is a trade off between the two parameters, simultaneous improvements are not possible. Also, perfect pole-zero cancellation never happens in a real system due to mismatches. Therefore, PID controller design should take this factor into account. Lastly, all the preceding steps can be performed in MATLAB with the aid of *rltool* [4] or *sisotool* in the most recent release of the software package.

D. *Z-Domain Transformation and Discrete time PID Law*

The discrete time PID algorithm used in a digital PID controller is obtained by transforming the continuous time compensator to its discrete time equivalent. Conversion of the PID transfer function from the S domain to the Z domain is performed using the combined backward rectangular and Tustin transform [5] in Table I below, with the sampling interval denoted as T.

TABLE I
S-DOMAIN TO Z-DOMAIN CONVERSION

Components	**S-Domain TF**	**Z-Domain TF**
Proportional	K_P	K_P
Integral	$\frac{K_I}{s}$	$K_I \frac{T}{2}\left(\frac{z+1}{z-1}\right)$
Differential	$K_D s$	$K_D\left(\frac{z-1}{Tz}\right)$

Collecting the three components together results in the Z-domain PID transfer function:

$$H_{PID}(Z) = \frac{D(z)}{E(z)} = \frac{C_0 z^2 + C_1 z + C_2}{(z-1)z} \tag{5}$$

where the coefficients C_0, C_1 and C_2 are given as:

$$C_0 = \frac{K_I T^2 + 2K_P T + 2K_D}{2T} \tag{6}$$

$$C_1 = \frac{K_I T^2 - 2K_P T - 4K_D}{2T} \tag{7}$$

$$C_2 = \frac{K_D}{T} \tag{8}$$

By apply the inverse Z-Transform to (5) the discrete time PID control law is determined to be:

$$d[n] = d[n-1] + C_0 e[n] - C_1 e[n-1] + C_2 e[n-2] \tag{9}$$

where d[n] is the current duty cycle being sent to the PWM generator and e[n] is the most recent mismatch between f_{ref} and f_{osc}. Due to its relative simple form, (9) can be readily implemented using digital circuits.

E. *Simulation and PID Coefficient Tuning*

A Simulink model of the closed loop digital DVS system is created to facilitate rapid system level prototyping and PID coefficient tuning. Real system behaviors such as quantization, noise, and delay are reflected in the model.

The time domain simulations exposed the problem of limited cycle oscillation in the DVS loop which manifested itself as ripple voltage in the steady state when [6] a voltage is being controlled with a resolution higher than that can be achieved. This problem was solved by increasing the PWM resolution. The model was also very helpfully in investigating transient behaviors such as overshoot and setting time, allowing the "near-realistic" tuning of PID coefficients, shortening the calibration time required at the hardware implementation stage.

A MATLAB GUI is created to facilitate rapid DVS system design according a variety of system variables. A picture of this program is shown in Fig. 2.

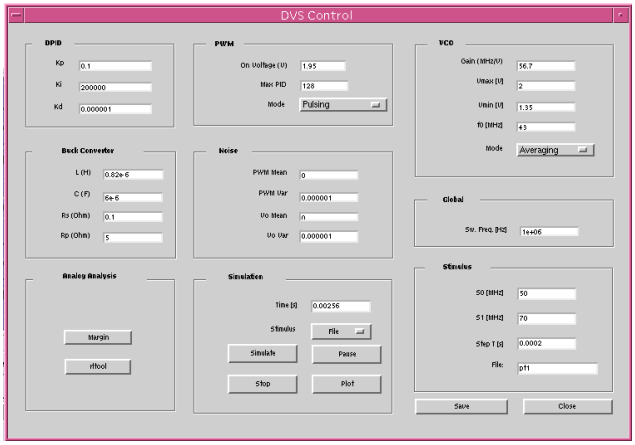

Fig. 2. A screen capture of the MATLAB GUI.

F. *CPLD Implementation*

The DVS design is realized on a 0.18 µm, 1.8V X2C256 Complex Programmable Logic Device (CPLD), and is configured as shown in Fig. 3.

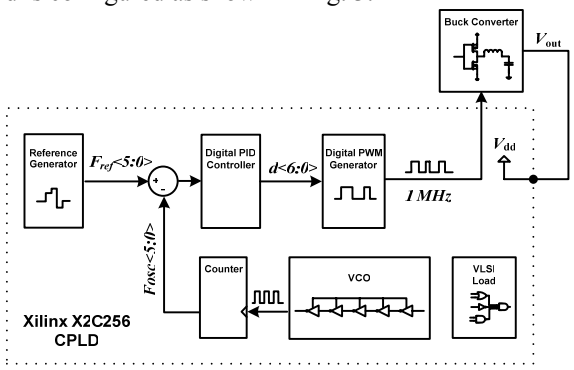

Fig. 3. A diagram detailing the DVS system topology.

With the exception of the power stage which is provided by the ZVS-QSW chip [7], all the other loop components are implemented in digital logic. A summary of the system performance is listed in Table II:

TABLE II
PERFORMANCE SPECIFICATIONS

Components	Z-Domain TF
Worst Case Transient Response	25 µS
Overshoot and Ringing	Less than 5%
Average Voltage Step Size	15 mV
Scaling Range	1.3 – 1.90 V
Input Voltage	2.0 V
Switching Frequency	1 MHz
Filter Size	C = 1 µF, L = 0.82 µH

Various f_{ref} patterns can be produced via the reference generator. Shown in Fig. 4 is the V_{dd} response as f_{ref} is being swept in increasingly small steps between its minimum and maximum values, demonstrating the DVS performance across the entire operating region. In Fig. 5, the close up of a V_{dd} transition is shown to illustrate transient specifications. Additionally, a plot of the measured V_{dd} versus reference frequency is presented in Fig. 6. From the minor non-linearity in the graph, it can be seen that V_{dd} step size decreases slightly as f_{ref} is lowered.

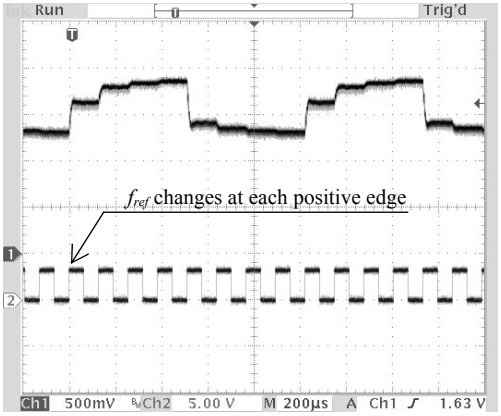

Fig. 4. A scope capture showing V_{dd} being scaled in increasingly small steps between it's maximum and minimum values.

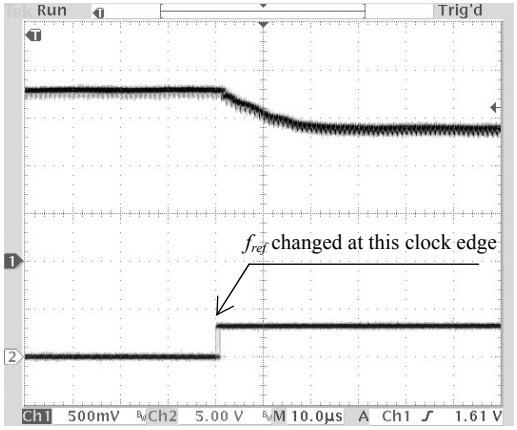

Fig. 5. A scope capture showing V_{dd} transitioning from 1.8V to 1.35V.

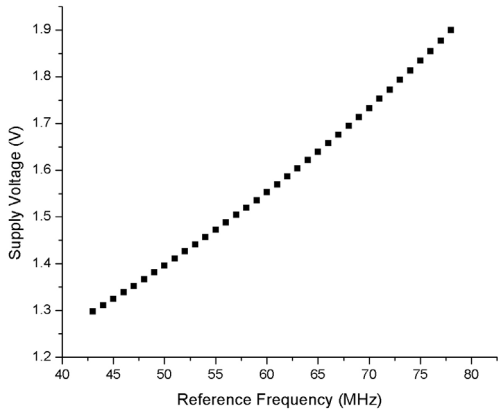

Fig. 6. A plot of supply voltage versus reference frequency, showing all operating points of the DVS system.

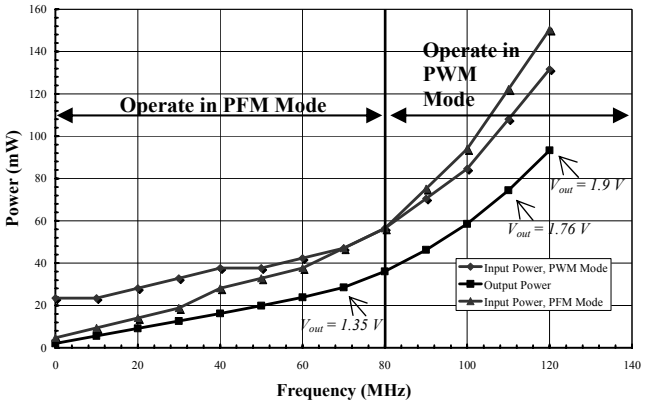

Fig. 7. A set of experimental data comparing the input power required by the PWM and PFM mode DC/DC conversion to generate the same output power at the various circuit operating frequencies under DVS. By appropriately switching between the two modes of operation the input power consumption is minimized.

III. PROPOSED DVS WITH AUTOMATIC PFM AND PWM MODE SWITCHING

When a PWM mode DC/DC converter is operating at light load conditions, the switching loss becomes a considerable fraction of the total power consumption, causing degradation of conversion efficiency. In PFM mode operation, a constant on time is maintained while the frequency of the gate drive pulses is modulated. Since switching activity decreases with load, significantly higher efficiency is achieved at light load conditions. However, at high load, switching activity becomes excessive and efficiency degradation follows. By appropriately switching between the two modes of operation, maximum power efficiency can be realized across the entire load range.

DVS is carried out separately using the PWM and PFM mode conversion to demonstrate how the input power consumption in the two modes varies with load. The result is plotted in Fig. 7, where the x-axis is the frequency at which the VLSI load is operating. The output power at each of these frequencies is minimized through DVS. At low operating frequencies, the PWM mode conversion consumes significantly more input power to deliver the same output power, where as the PFM mode conversion consumes more input power at high operating frequencies. The cross over point is approximately at 75 MHz. Since supply voltage scaling in the DVS controller is done through setting f_{ref} which is directly proportional to the circuit operating frequency, the cross over frequency can be easily detected through monitoring f_{ref}. The maximum power efficiency across all load conditions can then be realized under DVS by switching between PFM and PWM mode operation as needed.

III. CONCLUSION

Power saving from DVS at light load conditions is limited due to low DC/DC converter efficiency. A DVS controller with 25 μs worst case settling time and 15 mV average V_{dd} step size across the 1.30 –1.90 V range is realized on a X2C256 CPLD from Xilinx. By monitoring reference DVS frequency, automatic switching between PFM and PWM mode can be carried out to realize maximum DVS energy saving across the entire load range.

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REFERENCES

[1] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits", Proceedings of IEEE, vol. 91, no. 2, pp. 305-327, February 2003.

[2] S. Tyagi et al., "A 130nm Generation Logic Technology Featuring 70nm transistors, Dual Vt Transistors and 6 Layers of Cu Interconnects," in Dig. Tech. Papers Int. Electron Devices Meeting, 2000, pp. 567-570.

[3] G.Y. Wei and M. Horowitz, "A Fully Digital, Energy-Efficient, Adaptive Power-Supply Regulator", IEEE Journal of Solid State Circuits, vol. 34, pp. 520-528, April 1999.

[4] A. Prodic, D. Maksimovic, and R. W. Erickson, "Design and Implementation of a Digital PWM Controller for a High-Frequency Switching DC-DC Power Converter", The 27th Annual Conference of the IEEE Industrial Electronics Society, pp. 893-898, 2001.

[5] J. L. Tong and J. P. Bobis, "A Model For Designing Digital PID Controllers", Proceedings from Power Electronics and Motion Control, vol. 3, pp. 1157-1162, Nov 1992.

[6] A. V. Peterchev and S. R. Sanders, "Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters," IEEE Transactions on Power Electronics, vol. 18, pp. 301-308, Jan 2003.

[7] S. Chen, O. Trescases, W. T. Ng, "Fast Dead Time Locked Loop for High-Efficiency Microprocessor-Load ZVS-QSW DC/DC Converter", IEEE Conference on Electron Devices and Solid-State Circuits, pp. 391-394, Dec 2003.