A DLL/PLL Based Multi-Phase Interleaved DC-DC Converter with Digital Off-time Control and Active Series Balancing for Electric Vehicles

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Abstract—In this paper, a Delay-Locked Loop (DLL) and Phase Locked Loop (PLL) interleaving control scheme is demonstrated for multi-phase dc-dc converters in a light electric vehicle (LEV) application. Three interleaved non-inverting buck-boost (NIBB) sub-converters operate in peak current mode control (PCMC), and a fully digital off-time generator (OTG) is used in lieu of slope compensation for more accurate battery current sensing and improved converter dynamics. A DLL adjusts the master sub-converter off-time to maintain quasi fixed-frequency operation, while a PLL adjusts the two slave sub-converter off-times to achieve inductor current interleaving. Active series balancing is achieved by adding a single switch to the NIBB that connects to the adjacent series battery. The modified topology reuses the NIBB inductor to reduce system cost, complexity and weight, while providing balancing capabilities. The series balancing scheme is validated in simulation, and the DLL/PLL interleaving control schemes are demonstrated experimentally on a 12 V, 270 W dc-dc converter running at 555 kHz. With the DLL and PLL based frequency control, multi-phase dc-dc converter interleaving is achieved within 150 s, and stable QFF operation and interleaving are maintained through step-up and step-down transient events.

I. INTRODUCTION

While the cost of automotive lithium-ion (LI) batteries remains a major hurdle for mass adoption of the electric vehicle, many automotive manufacturers have embraced alternative energy storage systems such as hybrid electric vehicles (HEVs), fuel cell electric vehicles, (FCEV), and hydrogen power vehicles [1]–[5]. For light electric vehicles (LEVs) with limited range requirements, a multiple chemistry battery approach using LIs and lead-acid (PbA) batteries is an attractive low cost, zero-emission alternative. The target vehicle of this work is a Polaris Ranger EV utility vehicle, and the hybrid energy storage system (HESS) architecture is shown in Fig. 1.

The HESS uses four series 11.1 V, 90 Ah lithium-ion (LI) modules that make up a 44.1 V inverter bus, and four 12 V, 92 Ah lead-acid (PbA) modules that augment each LI through an Intelligent Hybrid Battery Manager (IHBM). The IHBM comprises of a dc-dc converter and controller, and a HESS module comprises of an IHBM and the two battery modules. The hybrid energy storage architecture and power-mix control algorithm allows for a reduced dc-dc converter peak power rating of 360 W. This peak power rating is a small fraction of the peak load demand of 2 kW for a single HESS module. The hybrid battery chemistry power-mix algorithm is outside the scope of this work, and is described in more detail in [6]. This paper examines the design and control of the dc-dc converter in a single IHBM.

Fig. 1: The proposed hybrid battery architecture, targeted for the Polaris Ranger EV utility vehicle.

The PbA and LI modules have a voltage range of 11-12.8 V and 10-12.4 V, respectively. A modified non-inverting buck boost (NIBB) converter that incorporates active series balancing capability is proposed. A multi-phase dc-dc converter approach, with parallel peak-current mode controlled (PCMC) sub-converters, is chosen. This spreads the converter hot-spots and flattens the efficiency curve over the load range [7], [8]. Interleaving the inductor ripple currents between independently controlled sub-converters allows for tighter control of power converter currents, alleviates current imbalance, and improves heat distribution. Interleaving is straightforward for fixed-frequency PCMC converters, but is a challenge for variable frequency PCMC converters.
Fig. 2: Steady-state operation of PCMC with $D > 0.5$ (a) without and (b) with slope compensation. (c) Steady-state operation with the OTG.

Phase-locked loops (PLLs) have previously been demonstrated for interleaving on-time and off-time controlled current mode dc-dc converters [9], [10], and delay-locked loops (DLLs) have been demonstrated for hysteretic controlled multi-phase integrated dc-dc converters and VRM applications [11], [12]. The PLL and the DLL methods are similar in principle. The PLL uses an absolute phase and frequency reference signal, and the DLL uses a delay line to generate a reference signal of desired switching period, $T_s$. The phase of $T_s$ is not locked to an external clock, and as such, the DLL requires only a first-order compensator, while a second order compensator is generally required for PLL operation. The small-signal model of the DLL and PLL are derived in [13], which concludes that the two frequency control schemes offer comparable bandwidth while the DLL offers superior robustness and smoother dynamics. A joint DLL and PLL approach is proposed for an off-time controlled multi-phase dc-dc converter. The master sub-converter uses a DLL to achieve quasi-fixed frequency (QFF) operation, and the slave sub-converters use PLLs to phase and frequency lock to the master sub-converter.

This paper is structured as follows. The DLL/PLL based, off-time controlled multi-phase inter-leaving converter is described in Section II. A series battery balancing capability is added to the NIBB with minimal additional hardware, and this scheme is presented in Section III. Finally, the experimental converter is demonstrated in Section IV.

II. ELECTRICAL DESIGN

A. Off-time Generator

Traditional PCMC is unstable for $D > 50\%$, as depicted in Fig. 2(a). With traditional PCMC, reference current transients also lead to unstable inductor ripple currents without additional control measures, as shown in Fig. 3(a). The aforementioned instability can be remedied by introducing slope compensation [14]. Slope compensation makes accurate average inductor current, $\langle i_L \rangle_{T_s}$, estimation difficult, which is critical for accurate battery SOC estimation, as shown in Fig. 2(b). Slope compensation is also expensive and highly complex to implement in the digital domain.

An off-time generator, (OTG), is a popular alternative where converter off-time, $t_{off}$, is adjusted on a cycle-by-cycle basis to avoid inductor current instability, as shown in Fig. 2(c). The value of $D$ is dependent on battery voltages such that

$$D = \frac{V_{LI}}{V_{LI} + V_{PbA}},$$

(1)

$t_{off}$ is related to $I_{PbA}$ and duty ratio by

$$t_{off} = D' \cdot T_s = \frac{T_s}{M+1} - t_{dead,1} - t_{dead,2},$$

(2)

and

$$I_{ref} = \frac{I_{PbA} \cdot (M + 1)}{M} + \frac{V_{LI} \cdot t_{off}}{2L}.$$  

(3)

The OTG method also has superior step current reference behavior compared to the other methods [15]–[17]. For traditional PCMC and slope compensation, a step in $I_{ref}$
leads to instability, as shown in Fig. 3(a) and Fig. 3(b), respectively. The variable switching frequency nature of the off-time controlled converter makes the switching operation resilient to steps in $I_{ref}$, as shown in Fig. 3(c). The OTG, leading edge blanking, and adaptive dead-time control are implemented in an FPGA with a timing resolution of 5 ns.

III. ACTIVE SERIES BATTERY BALANCING TOPOLOGY

By adding a single transistor to the conventional NIBB topology, active balancing can be achieved for series lithium-ion modules in the battery stack. The drain of the additional transistor is connected to the adjacent, upper battery’s positive terminal, and its source connects to the NIBB inductor, $L$, as shown in blue in Fig. 5(a). The additional transistor creates an alternate current flow path to transfer energy between unbalanced series battery modules, and allows for series battery balancing without adding additional magnetic components. The modified NIBB provides active series balancing capability with minimal hardware, which reduces system mass, complexity, and cost.

Fig. 5: (a) NIBB converter with an additional high-side switch for series battery balancing. (b) Balancing architecture for four series lithium battery modules.

The equalization mode operation emulates the next-to-next topology [18], [19], used for active series battery balancing, and the delta converter topology [20], used for series photovoltaic applications. The balancing converters for a four series battery configuration is shown in Fig. 5(b). In equalization mode, the gate signals $c_2$ and $c_5$ switch at high frequency, while gate signal $c_3$ is held on. Energy flows in the direction away from the higher voltage battery and into the lower voltage battery. The simplest implementation of
equalization mode involves fixing the $c_2$ and $c_5$ duty cycle, $D$, to 0.5, and allowing the difference in battery voltage dictate the direction of current flow.

The simulated balancing performance of the converter operating in equalization mode is shown in Fig. 6. Capacitor $[n]$ has an initial condition of 12 V, while capacitor $[n+1]$, $[n+2]$, and $[n+3]$ have an initial conditions of 11.5 V, 11.75 V, and 11.8 V, respectively. The charge from the various storage devices is shuttled around and the capacitor voltages converge to the average value of 11.75 V over time.

With $D = 0.50$ and $T_s = 600$ kHz, a 5% difference in battery state-of-charge (SOC) can be reduced to zero within 3 hours, and a 1% difference in SOC can be reduced to zero within 40 minutes for the target 11.1 V, 90Ah lithium batteries.

IV. EXPERIMENTAL RESULTS

Three separate sub-converter PCBs connect to a common controller PCB that houses the FPGA controller, as shown in Fig. 7(a). Busbars connect the sub-converters to the lead-acid and lithium-ion batteries, depicted in Fig. 7(b). The 12 V to 11.1 V, peak 36 A rated dc-dc converter achieves 88.5% efficiency at 100 W output power with single sub-converter operation, 88% efficiency at 180 W with dual sub-converter operation, and 87% efficiency at the rated 270 W power with three parallel sub-converters, as shown in Fig. 8(a). As a result of the parallel sub-converter operation, the measured efficiency is relatively flat, between 87% and 88.5%, from 70 W to 270 W output power. The dc-dc converter is able to maintain the higher efficiencies by enabling the parallel sub-converters depending on the total current reference, $I_{ref,tot}$, where

$$I_{ref,tot} = I_{ref,A} + I_{ref,B} + I_{ref,C},$$

which is known as phase-shedding. To demonstrate the dynamic phase-shedding operation, the converter was run for a thirty minute period, and $I_{ref,tot}$ is ramped down from a digital value of 2000, roughly 25 A. As $I_{ref,tot}$ falls, the sub-converter reference currents adjust, and the sub-converters turn off accordingly, as shown in Fig. 8(b). All three sub-converters are disabled when $I_{ref,tot}$ falls below 6 A because light-load efficiency is relatively poor.

The single sub-converter operating with PCMC and an off-time generator is shown in Fig. 9(a), where the adaptive dead-times, $t_{dead,1}$ and $t_{dead,2}$, are shown for the $c_1$ and $c_2$ signals. Values of 35 ns and 10 ns are typical for $t_{dead,1}$ and $t_{dead,2}$, respectively, for nominal battery voltages at the rated 270 W load. The startup sequence for multi sub-converter operation is staggered 10 ms between sub-converters to reduce the step loading on the gate-driver power supply, as shown in Fig. 9(b). The three sub-converters are unsynchronized at startup, and the DLL and PLL frequency loops work to lock the switching frequency and phases.

Upon this no-load to 20A load startup condition, the DLL-controlled master sub-converter switching period, $T_s,A$,
reaches a target switching period of $T'_s = 1.82 \mu s$ within 60 micro-seconds, while the PLL-controlled slave sub-converters converge on $T'_s$ after 150 micro-seconds, as shown in Fig. 10(a). The second order PLL causes the $T_{s,B}$ and $T_{s,C}$ to oscillate around $T'_s$ before settling, while the first order DLL causes $T_{s,A}$ to settle more quickly and smoothly [13]. The phase-locking of the interleaved sub-converters for the same startup condition is shown in Fig. 10(b). After some initial oscillation, the sub-converters lock to a final phase within 150 micro-seconds. The DLL, PLL stability and off-time generator performance is limited by the 5 ns resolution of the FPGA.

The controller can adaptively change the interleaving phase shift depending on the number of active sub-converters. The measured interleaved inductor ripple current waveforms of two sub-converters, operating with 180° phase shift, and three sub-converters, operating with 120° and 240° phase shift, are shown in Fig. 11(a) and Fig. 11(b), respectively. With the adaptive off-time control, the multi-phase converter does not exhibit oscillations during a step response as seen with the traditional PCMC or the slope compensation methods described in section II. During a 7A to 20A current step, the off-time controlled sub-converters have a single switching period response, and are resilient in maintaining stable QFF operation through the transient, as shown in Fig. 12(a). Fig. 12(b) shows the same fast response and stability for a negative step in the current reference signal.
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V. CONCLUSIONS

A novel DLL and PLL based PCMC scheme is demonstrated that achieves synchronization of off-time controlled multi-phase dc-dc converters. The master sub-converter uses a DLL to achieve quasi-fixed frequency (QFF) operation, and the slave sub-converters use PLLs to lock their phase and frequency to the master sub-converter. The fully-digital OTG and frequency control loops are realized on an FPGA controller. This allows for tight switching frequency control between sub-converters with minimal analog control circuitry and simplified hardware design, reducing system mass, volume and cost. The converter settles within one cycle to a reference current step, with smooth dynamic interleaving. The proposed modified NIBB topology also integrates a series battery balancing topology into the existing hardware without the need for additional magnetics. The scheme adds balancing capability with little additional mass and cost.

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REFERENCES


Fig. 12: Measured transient (a) step-up response and (b) step-down response.