A Segmented Digital Pulse Width Modulator with Self-Calibration for Low-Power SMPS

Olivier Trescases, Guowen Wei and Wai Tung Ng

Abstract—The next-generation, digitally controlled DC-DC converters require a high frequency, high resolution, low power and area efficient digital pulse width modulator (DPWM). This paper introduces a self-calibrated segmented DPWM that uses a delay-locked loop to calibrate adjacent delay segments. An 8-bit prototype designed in a 0.13-µm CMOS process operates at a switching frequency of 11.6 MHz, draws 190 µA from a 1.2 V supply and occupies only 0.0075 mm².

I. INTRODUCTION

Digital control for high-frequency, low-power switch mode power supplies (SMPS) is gaining popularity due to the immense processing capability offered by advanced digital processes. The advantages of digital control include inherent noise immunity, on-the-fly configuration, potential for advanced non-linear control, compatibility with low voltage deep-sub-micron processes, design re-use, low parts count and automated design flow. However, the industry has been somewhat reluctant to adopt digital control for low power (<10W) applications due to the perceived cost and performance disadvantages of digital control compared to state-of-the-art analog solutions. Traditional digital controllers for SMPS are indeed power hungry due to the high oversampling clock frequency requirements. One of the main bottlenecks is the digital pulse width modulator (DPWM), which is the focus of this work.

This paper is organized as follows. Existing DPWM architectures are discussed in Section II and the self-calibrated segmented DPWM (SC-DPWM) is described in Section III. Finally, simulation results for a 0.13µm CMOS test-chip are given in Section IV.

A. Importance of DPWM Linearity in DC-DC Converters

The DPWM converts an N-bit duty cycle command \( d[n] \) from the digital compensator to a pulse having an on-time of \( d[n]/(2^{N-1} \cdot f_s) \). Selecting the resolution (in bits) of the different processing stages to achieve a stable output voltage under a wide range of conditions is generally non-trivial. The ADC resolution is usually selected to satisfy the voltage regulation specification and the DPWM resolution must then be chosen sufficiently high to avoid limit cycles [1]:

\[
G_0 \cdot q_{DPWM} < \alpha q_{A/D}
\]  

where \( G_0 \) is the DC control-to-output gain, \( q_{DPWM} = 1/2^N \) is the LSB duty cycle, \( q_{A/D} \) is the ADC quantization voltage and \( \alpha < 1 \) is used to provide a safety margin. The condition of (1) must be satisfied to ensure that the output voltage can be positioned in the zero-error bin of the ADC. Non-linearities in the DPWM block cause \( q_{DPWM} \) to vary with the duty cycle \( d[n] \), which can lead to limit cycle oscillations for certain output voltages. The effect of non-linearity on limit-cycle behavior is covered by [2]. This effect is especially relevant in applications requiring a wide output voltage and duty cycle range, as in dynamic voltage scaling [3]. From (1) it is apparent that, unlike data converter applications such as class-D amplifiers, a certain amount of non-linearity is tolerable in digital DC-DC converters [4].

II. EXISTING DPWM ARCHITECTURES

A detailed description of existing DPWM solutions is provided by [4] and only the key points and trade-offs are reviewed here. The most simple and area efficient DPWM is the direct digital equivalent of analog PWM, as shown in Figure 1. An N-bit counter is used to generate a digital sawtooth waveform, followed by a comparator that selects the proper time slot to produce the desired duty cycle. The high-frequency clock at \( f_{RAMP} = 2^N \cdot f_s \) makes this approach unsuitable for converters operating with \( f_s > 1 \) MHz due to high power consumption.

![Fig. 1. Block diagram of counter-based DPWM.](image)

An alternative DPWM implementation uses a delay-line with \( 2^N \) delay elements and a \( 2^N \)-to-1 multiplexer combination to eliminate the need for \( f_{RAMP} \) [5]. The delay-line DPWM approach trades high power for large area consumption but the \( 2^N \) delay cell count is unpractical for DPWMs having \( N > 6 \). The linearity is limited by the device matching in a relatively large number of cells and is therefore worse then in the counter-based approach. The area can be reduced by using a hybrid combination of coarse delay using a counter and fine delay using a delay line [6]. A segmented binary-weighted
delay line can also be used, as shown in Figure 2 for a 3-segment, 6-bit DPWM [4]. The additional delay compensation circuit is not shown for simplicity. Each segment has a 4-to-1 multiplexer controlled by two bits of \( d[i] \). The delay in each of the four elements of the \( i^{th} \) segment is given by (2):

\[
\Delta t_i = 4\Delta t_{i-1} = 2^{2i}\Delta t_0
\]

The \( \Delta t_i \) delays are created by simply replicating the \( \Delta t_0 \) delay cell, resulting in the same overall number of delay cells, neglecting the additional dummy load cells. The modest area reduction compared to the traditional non-segmented delay-line DPWM (NS-DPWM) comes from the multiplexer, since a 64-to-1 multiplexer is replaced by four 4-to-1 multiplexers.

III. SELF-CALIBRATED DPWM CONCEPT AND DESIGN

A. Delay-Locked Loop for DPWM Linearization

The area and power consumption of the segmented DPWM can be greatly reduced by using identical, tunable delay elements instead of replicating \( \Delta t_0 \). The control voltage of each segment, \( V_{\text{entrl}} \) is adjusted to meet (2) using a delay-locked loop (DLL), as shown in Figure 3 for an 8-bit DPWM. Though DLLs have previously been used to tune DPWM delay cells [5] [9], this is the first reported work where an embedded DLL is used to linearize a segmented DPWM.

Using this self-calibrated architecture, each segment is identical and differs only in its \( V_{\text{entrl}} \). Each segment’s DLL calibrates the delay cells to be four times longer than the previous segment. While this approach can achieve very good linearity with a minimum number of delay cells (2\( N \) instead of 2\( N^2 \)), the four DLLs consume a large area.

The self-calibrated DPWM (SC-DPWM) design shown in Figure 4 has a single DLL and is therefore a compromise between the architectures of Figure 2 and Figure 3. Each delay element in \( \text{Seg3} \) and \( \text{Seg1} \) is made using four delay cells from \( \text{Seg2} \) and \( \text{Seg0} \) respectively. The \( \text{Seg0} \) and \( \text{Seg1} \) blocks do not require a \( \text{cal} \) output and therefore the total number of 4-to-1 multiplexers is reduced from 8 to 6. The total number of delay cells is increased from 16 to 40 compared to the DPWM shown in Figure 3. The delay cells in \( \text{Seg0} \) and \( \text{Seg1} \) do not require an explicit \( V_{\text{entrl}} \). The oscillation frequency can be adjusted simply by varying the DPWM \( V_{\text{DD}} \) reference. The \( V_{\text{DD}} \) should be regulated anyways in all DPWMs to achieve a constant switching frequency, unless a differential delay-line is used as in [8]. This requirement is also present in high-performance analog controllers, where the PWM supply is usually derived from a bandgap reference and LDO combination. The DLL adjusts the \( \text{Seg2} \) and \( \text{Seg3} \) delays to maintain linearity while the \( V_{\text{DD}} \) is adjusted to set the LSB delay.

The delay calibration between \( \text{Seg2} \) and \( \text{Seg1} \) is achieved by synchronizing the \( \text{row} \) and \( \text{cal} \) rising edges, as shown in Figure 5(a). The DLL uses a precision phase comparator and a charge pump to regulate the delay.

Delay-line DPWM circuits typically include a reset mechanism to ensure that all the internal delay-line nodes are at the same voltage at the start of each PWM cycle. An innovative approach uses cascaded D flip-flop delay cells, where each flip-flop is used to reset the preceding cell [6]. The SC-DPWM includes a reset circuit that simultaneously resets all the delay cells and eliminates the need for an external clock, which is a major advantage over existing segmented DPWMs such as [4]. The ideal timing waveforms for the reset circuit are shown in Figure 5(b). When properly calibrated, the delay between the rising edges of \( \phi \) and \( \text{row} \) is equal to \( 4\Delta t_3 = 256\Delta t_0 \), which should be equal to \( T_s = 1/f_s \). The period is slightly extended by \( t_{rs} \ll \Delta t_0 \) due to non-zero propagation delays.

B. Tunable Domino Delay Cell

The DPWM delay cell must have a low transistor count and a wide delay tuning range. The proposed delay cell, which is shown in Figure 6 is based on the popular domino logic
inverter. The $\phi$ pre-charge signal is used to reset all the delay cells at the end of each PWM cycle by pre-charging node $X$ to $V_{DD}$. Once pre-charged, the cell acts as a current starved delay cell [5]. The $C_X$ discharge current and hence the propagation delay is controlled by $V_{cntrl}$ [5]. The additional inverters are used to achieve a sharp output rise-time. The delay-cell transistor count is only 10, compared to at least 30 for the DFF-based delay cell used in [6].

The current-starving transistor, $M_1$, is a long-channel, low-leakage (high-VT) device. The simulated internal delay of seg2 versus $V_{cntrl}$ for different channel lengths is shown in Figure 7. The target $\Delta t_2$ delay is 5.2 ns for $f_s$=12 MHz. This delay can be achieved over a range of $L$, resulting in a shift in the steady-state $V_{cntrl}$ operating point. More importantly, the control-to-delay gain, which directly affects the DLL loop gain, is also affected by the choice of $L$.

\[ \text{Delay} = \frac{\Delta t_2}{L} \]

\[ V_{cntrl} = \frac{V_{DD}}{2} \left( 1 - \frac{\Delta t_2}{\text{Delay}} \right) \]

The multiplexers connected to the delay-cell outputs degrade the linearity since the parasitic input capacitance is code-dependent. In addition, the voltage on the dynamic node of each delay cells is not identical due to leakage through the input transistor. This minor effect was reduced by using a high-VT starving transistor and sizing the pre-charge transistor to increase the parasitic $C_X$. The domino delay circuit is also susceptible to charge sharing and propagated noise. The additional inverters in the delay cell help reduce the delay dependence on the output capacitance, which may vary substantially due to routing constraints. The most obvious source of non-linearity in the SC-DPWM is the delay mismatch due to process variation across one segment. This effect cannot be canceled out by the DLL. The mismatch in the seg3 delay elements will clearly have the most detrimental effect on the linearity. The mismatch is expected to be reduced compared to a standard segmented DPWM, where the large number of delay cells distributed over a large area is much more prone to mismatch.

IV. IC IMPLEMENTATION AND SIMULATION RESULTS

The 8-bit SC-DPWM of Figure 4 was designed in a 0.13-\textmu m process from IBM in order to demonstrate the self-calibration concept. The target switching frequency was set to 12 MHz. A standard, non-segmented delay-line DPWM was also designed using identical delay-cell and multiplexer blocks for comparison purposes. The DLL, which includes a programmable bias circuit, a phase comparator, a charge pump and a 1 pF filter capacitor, occupies less than 15\% of the SC-DPWM area, as shown in Figure 8. Careful attention was paid during the layout phase to equalize the parasitic routing capacitance on the delay-cell outputs to avoid linearity degradation. The multiplexers are implemented using transmission gates and include a pre-charge mechanism similar to the domino cell of Figure 6. The test-chip layout is shown in Figure 9.

The output pulse width versus digital code for the DPWM-SC with the DLL operating in steady state is shown in Figure 10. The DNL and INL are shown in Figure 11 and Figure 12 respectively. Both the DNL and INL are well within the $\pm 0.5$ LSB limits. A linearity degradation is expected for the experimental prototype due to device mismatch, however these results demonstrate that that the DLL successfully linearizes the DPWM output between the delay segments.

The area is drastically reduced from 0.050 mm$^2$ for the non-segmented DPWM to 0.00750 mm$^2$ for the DPWM-NS. The SC-DPWM achieves a figure of merit of 50.9 MHz/mW.
with an 8-bit accuracy, which exceeds previously published DPWM data. The simulated results for the novel SC-DPWM are compared with two state-of-the-art delay-line DPWMs in Table I.

## V. Conclusion

This work builds on a previously developed segmented DPWM by introducing an embedded DLL to calibrate adjacent delay segments. An 8-bit prototype based on domino logic delay cells and designed in a 0.13-\( \mu \)m CMOS process operates at a switching frequency of 11.6 MHz, consumes 190 \( \mu \)A from a 1.2V supply and occupies only 0.0075mm\(^2\).

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### References


