A Digitally Controlled DC-DC Converter Module with a Segmented Output Stage for Optimized Efficiency

Olivier Trescases[1], Wai Tung Ng[1], Haruhiko Nishio[2], Masaharu Edo[2] and Tetsuya Kawashima[2]
[1]University of Toronto, 10 King's College Road, Toronto, ON, M5S 3G4, Canada
[2]Fuji Electric Advanced Technology Co. Ltd. 4-18-1, Tsukama, Matsumoto, Nagano 390-0921, Japan
E-mail: trescas@vrg.utoronto.ca

***Abstract*— This paper presents a 4 MHz, 0.9 W digitally controlled DC-DC converter with a miniature planar inductor for 1.8 V portable devices. In applications such as cellular phones, it is crucial to achieve high conversion efficiency over the entire load range. A binary-weighted segmented power stage is used to dynamically optimize the converter efficiency by reducing the gate-drive losses at mid-to-light loads. An all-digital segment controller based on a load current estimator is demonstrated. This approach is most effective in the mid-load range, where the losses are reduced by 33 %, corresponding to an efficiency improvement of 7.5 % at V_{in} = 4.2 V. A peak efficiency of 89 % is achieved at f_s = 4 MHz and V_{in} = 2.7 V.**

I. Introduction

The operation of DC-DC converters in the multi MHz range leads to fast dynamic response and small filter components at the expense of high gate-drive and switching losses. The power stage MOSFETs are usually sized to meet the maximum current handling and peak efficiency specifications. The relatively high power consumption in the high-frequency gate-drivers degrades the efficiency:

$$P_{gate} = f_s(C_{gate,P} + C_{gate,N})V_{in}^2 \quad (1)$$

where f_s is the switching frequency, $C_{gate,P}$ and $C_{gate,N}$ are the equivalent gate capacitances of the PMOS and NMOS power transistors respectively. For a given process technology, the inherent limitations on the power MOSFETs $Q_{gate} \cdot R_{on}$ product can lead to poor efficiency in the mid-to-light-load range. The gate drive power consumption can be reduced by operating the gate-drivers from a reduced voltage supply [1] but requires additional internal voltage regulator. Alternatively, an analog gate charge modulation method [2] has been used but a closed-loop charge control circuit is not provided. In this work, the limitation imposed by the $Q_{gate} \cdot R_{on}$ product can be overcome by digitally varying the effective size of the output stage MOSFETs on-the-fly. The trade-off between P_{gate} and the RMS conduction losses can be continuously optimized as the load current changes. This paper describes how this strategy can be implemented using a digital controller for optimized efficiency over the full load range.

This paper is organized as follows. The digital controller and automatic segment selector block for the output stage are covered in Section II. The micro inductor and hybrid packaging targeted in this work are described in Section III and measurement results for the DC-DC converter prototype are presented in Section IV.

II. Digital Controller and Segmented Output Stage

The architecture of the DC-DC converter is shown in Figure 1. The output voltage regulation loop is implemented using a standard digital PID voltage-mode control loop [3]. The three terms of the discrete-time PID difference equation are generated using area-efficient lookup tables (LUT) [3]. The digital pulse-width modulator (DPWM) provides an output pulse having an on-time of $t_{on} = d[n]/2^M$, where $d[n]$ is the M-bit duty cycle command computed by the compensator. A windowed ADC provides a digital error signal, $e[n]$ to the compensator.

A 4 MHz, 6-bit DPWM was created by using a hybrid approach [3], where a 16-element delay-line and 2-bit counter are used to generate the fine and coarse delay adjustment respectively. The effective DPWM resolution is augmented to 8 bits by using a 2-bit digital dither technique [4] over four switching cycles. A standard low-power analog pulse-frequency modulator (PFM) block is included for improved light-load efficiency. A *mode* pin is used to switch between PWM and PFM operation.

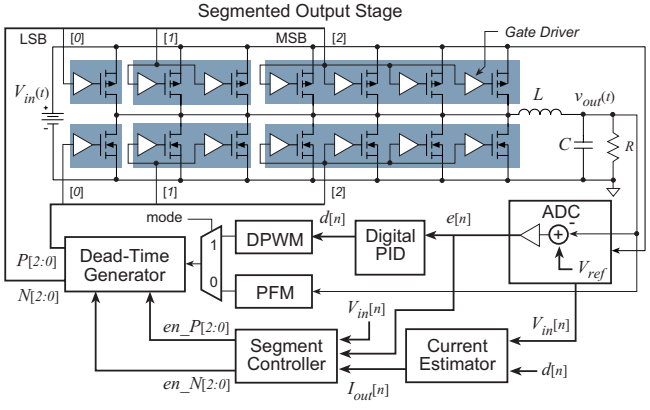

Fig. 1. Architecture of the digitally controlled DC-DC converter with a segmented output stage.

A. Sensor-less Load Current Estimation

An estimate of the load current is required by the segment controller to optimize the output stage efficiency. The current estimation process [5] is based on the relation between the steady-state duty ratio and the load current:

$$I_{out} = \frac{DV_{in} - V_{out}}{r} \tag{2}$$

where r is the converter series resistance, $r = DR_{on,P} + (1-D)R_{on,N} + R_L \approx R_{on} + R_L$, R_L is the inductor series resistance and D is the steady-state duty ratio. The output voltage is equal to V_{ref} in steady-state, therefore the relation given by (2) can be computed in the digital domain using a set of LUTs, assuming that a reasonable estimate for r is available. Clearly, the input voltage ADC sampling rate can be much lower than the switching frequency to conserve power.

The resolution of the current estimation method is directly related to the size of the ADC zero error bin, ΔV, where $e[n] = 0$ for $|V_{out} - V_{ref}| < \Delta V/2$. In the worst case, a change of $\Delta I_{out} = \Delta V/r$ is required to trigger a change in the duty cycle LSB, corresponding to the minimum detectable change in current. For the values of r = 1.2 Ω and ΔV = 30 mV ($\pm$ 15 mV $\approx \pm$ 1 % of 1.8 V), ΔI_{out} = 25 mA. The relatively large ΔV used in this work is a practical limitation due to the off-chip implementation of the controller.

B. Automatic Segment Selector

The PMOS and NMOS output stage transistors in Figure 1 are partitioned into three independently controlled segments. The transistor segments are created by using identical unit cells connected in parallel to achieve a binary weighting and a monotonic resistance versus segment enable code. The gate-drivers are segmented in a similar fashion to reduce the timing skew. The DPWM output is gated by the 3-bit segment enable buses, *en_P* and *en_N* within the dead-time circuit block. The 3-bit granularity is more than sufficient for this work. The enable codes can be controlled independently, leading to 49 possible power stage configurations in synchronous PWM mode. Most importantly, the area penalty due to segmentation is minimal because the power transistor active area is unaffected, since the source and drain nodes are shared.

Storing the optimal enable code for each combination of $V_{in}[n]$ and $I_{out}[n]$ is clearly unfeasible due to the large memory requirement. Therefore, a more practical code selection algorithm is proposed, as illustrated in Figure 2. One of the 12 possible PWM mode slots is selected depending on the estimated current and the input voltage. The enable codes are equal and have one of four possible values in PWM mode, simplifying the hardware. The only data which needs to be characterized and stored are the three optimal threshold currents, labeled as $i_{th2\text{-}0}$ that separate the current slots. Three sets of $i_{th2\text{-}0}$ must be stored, one for each input voltage range. The threshold currents increase with V_{in} since the $P_{gate} \propto V_{in}^2$ from (1). The decision to switch into PFM mode, where *en_P* = '001' and *en_N* = '000' is based on the *mode* pin, since the estimation method for $I_{out}(t)$ is not accurate in the light-load range. In this work, a simplified approach is used where the current estimate is based solely on $d[n]$ and a different LUT is hard-coded for each input voltage corner during testing.

The state diagram of the automatic segment controller is shown in Figure 3. The controller operates in one of four possible states. In transient state, the error signal $e[n] \neq 0$ and *en_N,P* = '111'. The controller enters the optimization state when $e[n] = 0$ for N_1 consecutive cycles. Upon entering this state, *en_N,P* are set based on the selection slots of Figure 2 and the current estimate computed prior to exiting the transient state. The current can only be estimated when *en_N,P* = '111' since r in (2) is dependent on R_{on} and hence *en_N,P*. The controller stays in the optimization state until the duty cycle has been adjusted by the PID control loop to correct for the new R_{on}. Steady-state is entered when $e[n] = 0$ for N_2 consecutive cycles. Once in steady-state, the optimal segments remain selected until a perturbation ($e[n] \neq 0$) causes a transition back to the transient state.

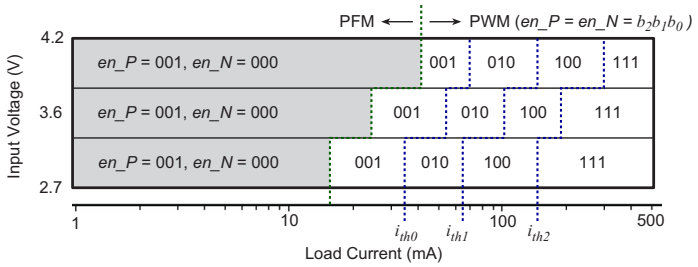

Fig. 2. The enable codes are switched based on the measured optimal current thresholds, $i_{th2\text{-}0}$. The optimal threshold currents are drawn to-scale, based on the efficiency measurements presented in Section IV.

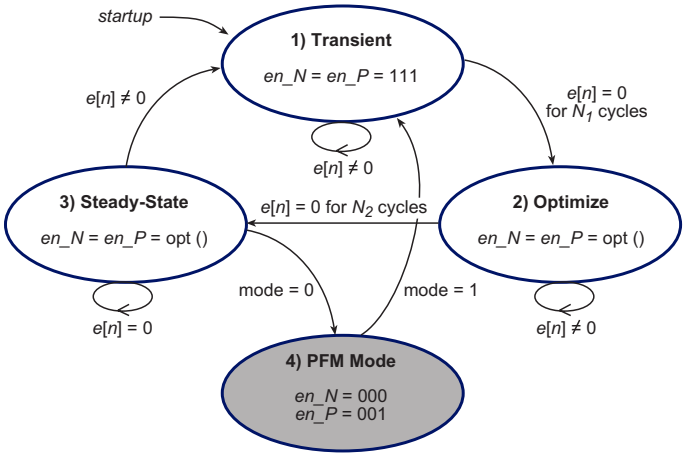

Fig. 3. Finite State Machine inside the segment controller.

III. Chip Size Module

The output filter inductor usually occupies the majority of the converter PCB area. In this work, a miniature planar inductor was fabricated in a ferrite substrate, as shown in Figure 4(a). The 3×3×0.525 mm^3 inductor is flip-chip packaged with the DC-DC converter IC to form the Chip Size Module (CSM), as shown in Figure 4(b). This hybrid packaging increases the

converter power density and results in a significant footprint reduction. The measured AC characteristics of the inductor with a different number of turns are shown in Figure 5 to highlight the trade-off between low series resistance and high inductance. The 11-turn inductor was selected in this work. The large variation in inductance versus current, 2.5× from 0 to 500 mA, affects both the converter efficiency and control loop dynamics. The inductor current ripple, Δi_L and hence the total AC conduction losses increase with the load current. This effect is partially offset by the drop in the inductor AC resistance.

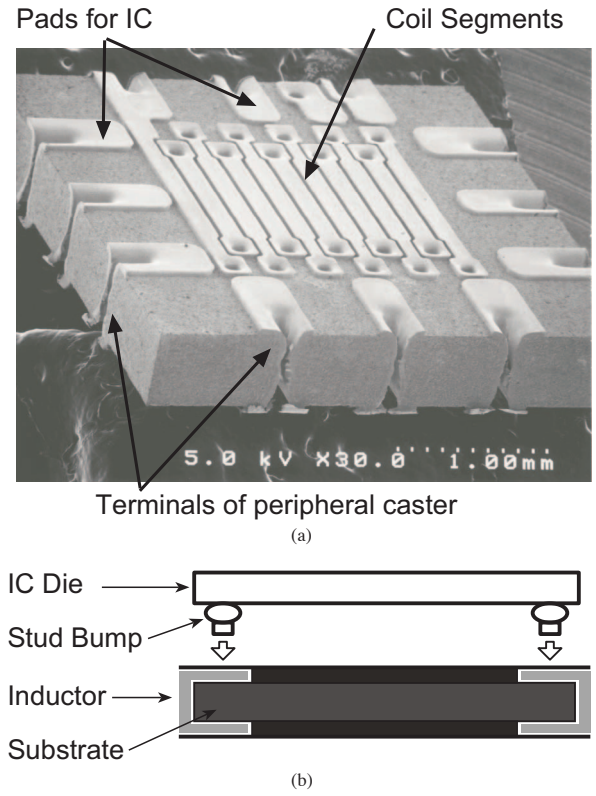

Fig. 4. (a) SEM of the 3×3×0.525 mm^3 miniature planar inductor built on a ferrite core. (b) The CSM assembly process; the IC terminals are connected to the IC using stud bumps before depositing a protective underfill.

IV. Experimental Results

The experimental chip was implemented in a 0.6 μm CMOS process and includes the segmented output stage with a rated current of 0.5 A, as well as gate drivers. The digital controller described in Section II was implemented off-chip using an FPGA during the proof-of-concept project phase. An external 4 μF capacitor was used with the 11-turn micro inductor.

A. Efficiency Improvement with Segmented Output Stage

The measured R_{on} of the segmented power transistors and gate-drive power consumption are shown in Figure 6. When operating with only the minimum sized segment at 4 MHz, P_{gate} is reduced by 6.3× while $R_{on\text{-}NMOS}$ and $R_{on\text{-}PMOS}$ are increased by 2.4× and 3.1×, respectively. The efficiency measurements for V_{in} = 2.7 V with different enable codes are shown in Figure 7. By selecting the optimal enable codes, the converter efficiency is significantly improved by a maximum of 7.5 % when compared to the non-segmented case as shown in Figure 8 and Figure 9 for V_{in} = 2.7 V and V_{in} = 4.2 V, respectively. The peak efficiency is limited by the relatively high inductor series resistance and high-switching losses in the power stage at f_s = 4 MHz.

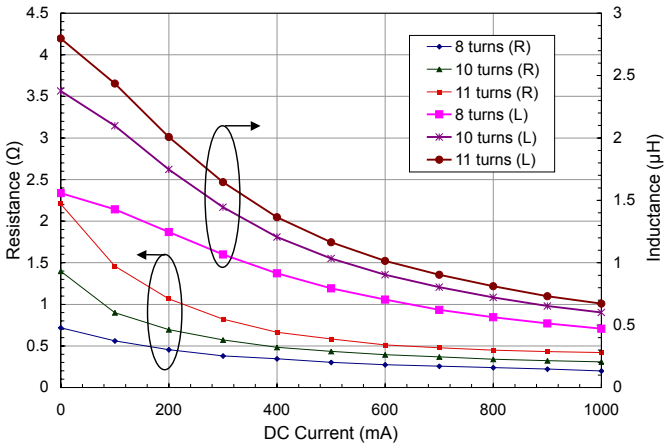

Fig. 5. Measured AC characteristics of the planar inductor showing the trade-off between resistance and inductance for different geometries.

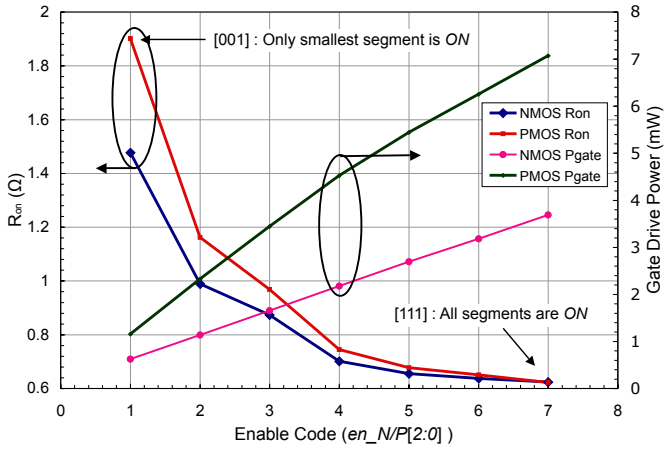

Fig. 6. Measured R_{on} and gate-drive power dissipation of the prototype IC for different enable codes at V_{in} = 3.6 V.

B. Converter Dynamics with Segment Selector

The converter load transient response for the converter operating without the segmented driver (en_P = en_N = '111') is shown in Figure 10(a). A digital signal is used to indicate when $e[n]$ = 0, indicating that $v_{out}(t)$ is in the zero error bin, which was set to 1.8 V ± 15 mV. The settling time is below 20 μs. The load step current is chosen to be well below the rated value, such that the optimal enable code is below '111' at V_{in} = 2.7 V. The dynamic response with the segment controller enabled is shown in Figure 10(b). After the control loop has recovered from the 20 - 100 mA load step, the segment controller waits for $\Delta t_1 = N_1/f_s = 100$ μs,

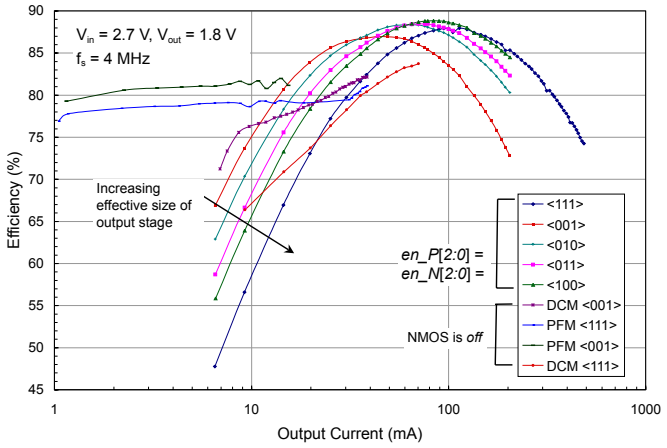

Fig. 7. Measured efficiency versus output current for V_{in} = 2.7 V for different enable codes.

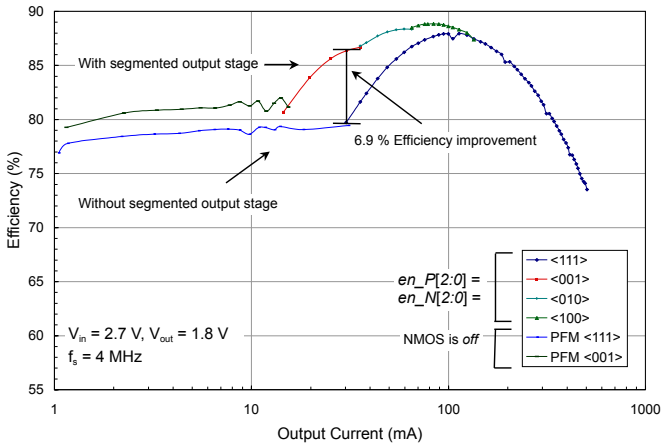

Fig. 8. Measured best-case efficiency comparison with and without the segmented output stage for V_{in} = 2.7 V.

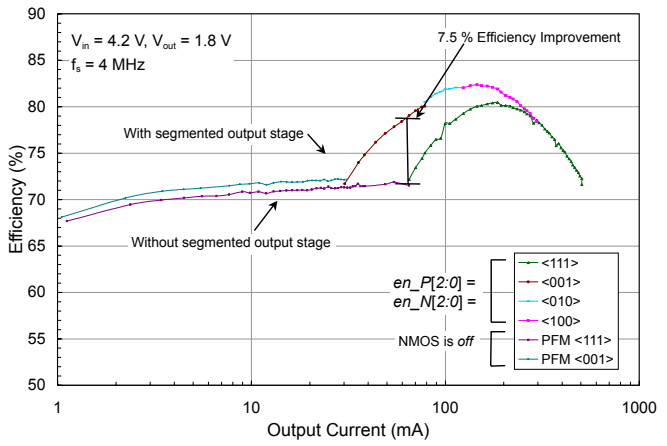

Fig. 9. Measured best-case efficiency comparison with and without the segmented output stage for V_{in} = 4.2 V.

after which the optimal code of '100' is selected. Once v_{out} is regulated back into the $\pm$ 15 mV zero error bin, the converter switches to steady-state after a delay of $\Delta t_2 = N_2/f_s =$

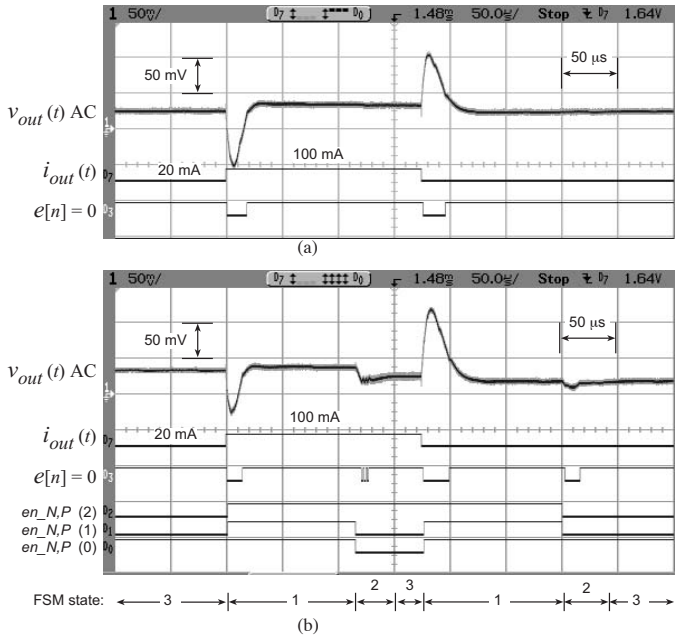

Fig. 10. Transient response for a 20 - 100 mA load step with (a) all segments enabled and (b) the automatic segment controller.

25 μs. The 100 - 20 mA transition brings the controller into transient mode. For positive load transients, the instantaneous change in *en_P,N* reduces r in (2), hence the voltage excursion on v_{out} is reduced. The response is slightly degraded for negative load transients due to the same effect.

V. Conclusions

The binary-weighted segmented output stage approach described in this work is most effective in the mid-load range, where the losses are reduced by 33 %, corresponding to an efficiency improvement of 7.5 % at V_{in} = 4.2 V, and f_s = 4 MHz. An all-digital automatic segment controller based on a load current estimator was demonstrated. It is shown that the automatic segment controller has a minor effect on the transient response.

VI. Acknowledgments

The authors would like to thank NSERC, CMC, Auto21, U of T open fellowship and Fuji Electric Device Technology Co. Ltd. for their support, as well as Guowen Wei for contributing to the verilog / MATLAB code development.

References

[1] V. Kursun, S. Narenda, V. De, and E. Friedman, "Low-voltage swing monolithic dc-dc conversion," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 51, pp. 241–248, 2004.

[2] M. Mulligan, B. Broach, and T. Lee, "A constant frequency method for improving light-load efficiency in synchronous buck converters," *Power Electronics Letters*, vol. 3, pp. 24–29, March 2005.

[3] B. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC," *IEEE Transactions on Power Electronic Circuits*, vol. 18, Jan 2003.

[4] A. Peterchev and S. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Transactions on Power Electronic Circuits*, vol. 18, pp. 301–308, Jan 2003.

[5] A. Prodić and D. Maksimović, "Digital PWM controller and current estimator for a low-power switching converter," in *IEEE Computers in Power Electronics 2000*, pp. 123–128, 2000.