Design of a rugged 60 V VDMOS transistor

H.P.E. Xu, O.P. Trescases, I.-S.M. Sun, D. Lee, W.T. Ng, K. Fukumoto, A. Ishikawa, Y. Furukawa, H. Imai, T. Naito, N. Sato, S. Tamura, K. Takasuka and T. Kohno

Abstract: Vertical double diffused MOSFET (VDMOS) is an established technology for high-current power-switching applications such as automotive circuits. The most serious failure mode is destructive damage during inductive switching, resulting from avalanche breakdown of the forward-blocking junction in the presence of high current flow. Improving the ruggedness of the device is achieved by enhancing its ability to absorb inductive energy under avalanche conditions. The purpose of the paper is to explore the possibility of improving the ruggedness of VDMOS through TCAD simulations. A p^+-strip buried underneath an n^+-source is proposed to suppress the turn-on of the parasitic bipolar transistor. VDMOS transistors with this design modification are expected to have higher ruggedness while maintaining its superior figure-of-merit.

1 Introduction

Growing demand for efficient power MOSFET switches has created a need for robust vertical double diffused MOSFET transistors (VDMOS) with ultra-low power loss. In applications with higher frequency switching (e.g. >1 MHz), the gate-drive loss becomes significant. Therefore the optimisation of a low-loss (switching and conduction losses) power MOSFET requires a better tradeoff between on-state resistance and gate input capacitance [1, 2]. Moreover, the most serious failure mechanism is destructive damage to the power VDMOS during inductive switching. This is commonly caused by avalanche breakdown of the forward-blocking junction in the presence of high current flow [3, 4].

In this paper, a 60 V VDMOS technology based on an existing technology from Asahi Kasei Microsystems Co. Ltd (AKM) is introduced. A simple process modification proposed to further improve the device ruggedness is confirmed by TCAD simulations.

2 Device structure

The conventional n-VDMOS structure is as shown in Fig. 1. The cell layout is usually hexagonal in shape and maximises the ratio of device channel width to the chip area in order to maximise its figure-of-merit (FOM). This number is the product of the on-resistance (R_{on}) and gate charge (Q_g) of the device, and is widely used to evaluate the performance metrics of power MOSFETs. The device structure is based on the double diffusion of the p-body and n^+ source regions using the edge of the polysilicon as a masking boundary.

The device fabrication process and device structure were developed using TCAD tools (ISE). The voltage handling capability is determined by the breakdown voltage of the p-body/n-epi layer junction and is strongly dependent on the thickness and the doping of the lower doped n-epi layer. Fig. 1 also shows the electric field distribution upon breakdown at 65 V. The device is optimised to have the highest electric field occur at the bottom of p-body/n-epi layer junction.

3 VDMOS fabrication process

The reference VDMOS was based on a 0.5 μm process developed by AKM. The starting wafer is a ⟨100⟩-oriented, n^+-type wafer with a nominal arsenic-doping concentration of 10^{19} cm^{-3}. At the beginning of the fabrication process, the wafers undergo epitaxial growth of an n^--layer with phosphorus doping concentration of 10^{16} cm^{-3}. Then, field oxidation is carried out to form a thick layer of oxide followed by active lithography and oxide etching to define the device area. After that, through gate oxidation, polysilicon deposition, doping and annealing, gate lithography and polyetching, a hexagon mesh gate pattern is formed. A self-aligned implantation of boron followed by annealing forms the p-body, while a self-aligned implantation of arsenic followed by annealing forms the n^+-source. The lateral diffusion difference of the p-body and n^+-source forms a controlled channel length along the Si-surface. The choice of doses is based on diffusion trials and extensive process and device simulations. A masked high dose boron implantation is carried out to form a p^+-region in the p-body to enhance body contact. After that, a thick inter-level oxide deposition of tetraethyl orthosilicate (TEOS) is followed by contact lithography and oxide etching to form the contact window. Finally, metallisation covers the chip surface and forms the butting source/body contacts for the VDMOS. By distributing metal contacts on the polysilicon gate around the edge of the chip, the

doi:10.1049/iet-cds:20070008

Paper first received 5th January and in revised form 23rd May 2007

H.P.E. Xu, O.P. Trescases, I.-S.M. Sun, D. Lee and W.T. Ng are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, Ontario, Canada M5S 3G4

K. Fukumoto, A. Ishikawa, Y. Furukawa, H. Imai, T. Naito, N. Sato, S. Tamura and K. Takasuka are with Asahi Kasei Microsystems, Shinjuku First West 16F, Nishi-Sinjuku 1-23-7, Shinjuku-ku, Tokyo, 160-0023, Japan

T. Kohno is with Asahi Kasei Corp., Analysis and Simulation Center, 2-1 Samejima, Fuji, Shizuoka 416-8501, Japan

E-mail: xu@vrg.utoronto.ca

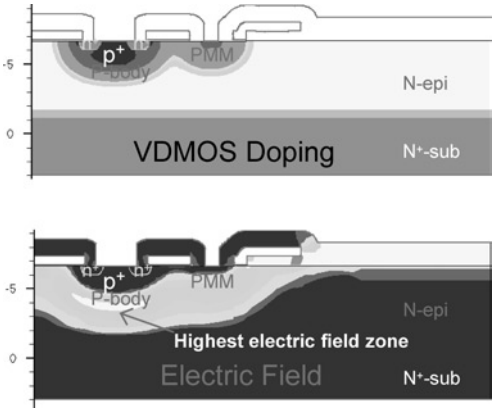

Fig. 1 *Simulated n-VDMOS structure and its electric field distribution at a breakdown voltage of 65 V*

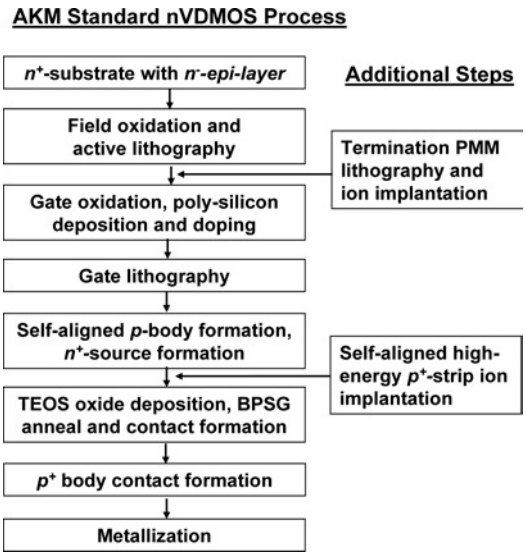

Fig. 2 *AKM VDMOS process flow with additional steps to enhance device ruggedness*

device's gate resistance is minimised. Fig. 2 illustrates the general flow of this fabrication process. The proposed p^+-strip implemented by self-aligned ion implantation of boron at 140 keV with dose of 1×10^{15} cm^{-2} is added before TEOS oxide deposition to improve the ruggedness of the device. Since the out-diffusion of this p^+-strip should be strictly controlled, the borophosphosilicate glass (BPSG) anneal at 870 °C for 20 min is the only major

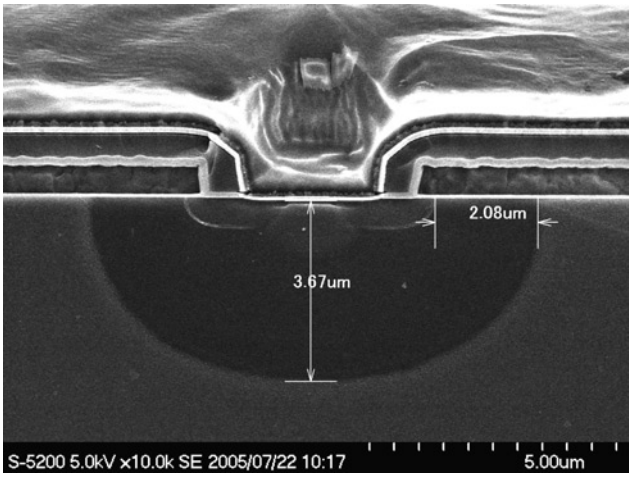

Fig. 3 *SEM cross-sectional structure of a fabricated n-VDMOS*

thermal process that has minimum effect on the out-diffusion of the implanted boron.

A cross sectional micrograph of the reference device taken using a scanning electron microscope is shown in Fig. 3. It has a channel length of about 2.6 μm and a p-body/n^--epilayer junction depth of 3.67 μm. The device achieves a specific on-resistance of 1.2 mΩ cm^2, breakdown voltage of 63 V and an FOM of 1210 mΩ nC.

4 Device ruggedness analysis

In order to improve the ruggedness of the device, the ability to withstand an avalanche current during an unclamped inductive load switching event must be improved. At the same time, the turn-on of the parasitic drain-body-source *npn* bipolar junction transistor (BJT) must be suppressed. ISE's device simulation shows that the maximum electric field, in a conventional VDMOS, spreads across the p-body underneath the n^+ source region. As shown in Fig. 4, the avalanche breakdown initiated in this high electric field region could generate massive electron-hole pairs. From there, electrons are swept across the drain while holes flow through the p-body regions and the p^+ diffusion towards the source metal contact. The resistance in these p-regions will cause a potential drop beneath the n^+ diffusion. If this resistance is large enough, the pn-junction may become forward-biased.

On the other hand, if defects are present in the silicon or if the device fabrication does not yield uniform characteristics across the entire transistor, avalanche multiplication will

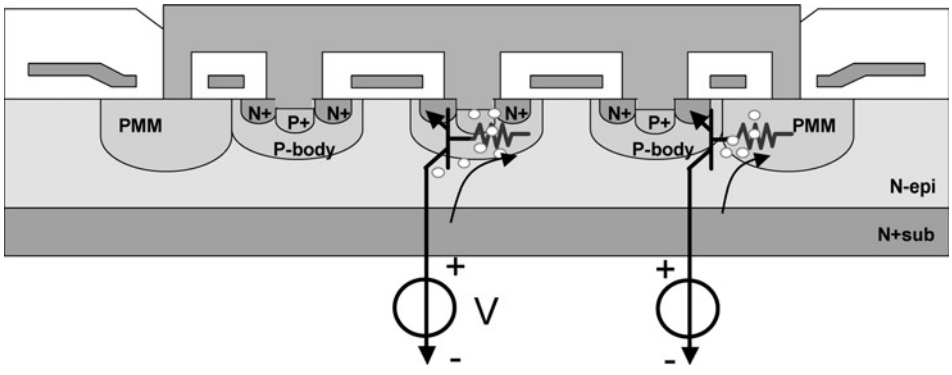

Fig. 4 *Schematic diagram of turning-on parasitic drain-body-source npn BJT in a VDMOS upon switching*
Open circles represent holes, the paired electrons are not illustrated

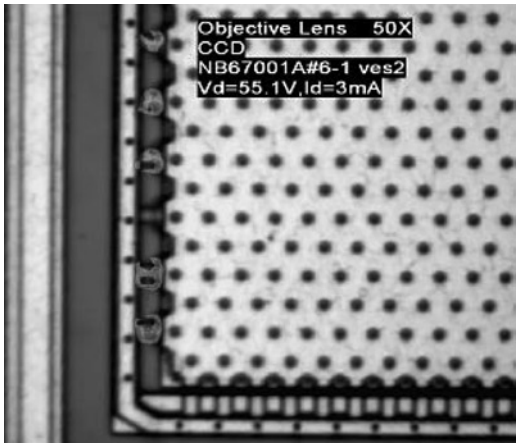

Fig. 5 *Photo-emission analysis of an experimental device with breakdown occurring at the periphery, indicating possible parasitic npn turn-on during UIS testing*

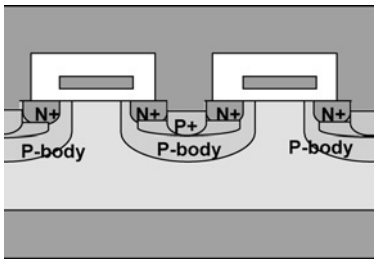

Fig. 6 *Schematic cross-section of a modified n-VDMOS with buried p^+-layer placed underneath the n^+ source*

most likely be a local event. This could cause a high avalanche current density flowing beneath the source n^+ region and give rise to a potential drop sufficient to forward-bias the *pn*-junction. All these factors could turn-on the parasitic *npn* BJT inherent in the VDMOS structure.

An unclamped inductive switching (UIS) test [5] in single-shot mode is employed to quantify the ruggedness in the event of an avalanche breakdown. In preliminary testing, the device in a DPAK package achieves a UIS avalanche energy of 150 mJ, which is almost at the same level as the commercially available IRFZ24N device. As the photo-emission analysis shows in Fig. 5, the device generates a large amount of hot electrons at the periphery upon UIS avalanche breakdown. The positive temperature coefficient associated with a forward-biased *pn*-junction leads to current crowding, which will rapidly drive the device to a secondary breakdown and eventual destruction.

In order to reduce the possibility of activating the parasitic *npn*, we propose a unique source structure, as illustrated in Fig. 6. In comparison with a conventional VDMOS, a strip of highly doped p^+-region is inserted at the n^+-source/*p*-body junction. This results in a lower drift resistance without increasing gate-drain capacitance and device on-resistance.

To verify the effectiveness of this p^+-buried layer under the source region, the tendency to show snapback breakdown behaviour is evaluated. Fig. 7 shows the half-structure of a MEDICI-simulated *n*-VDMOS device. The current flowline scenario of a conventional device is different from the one with a p^+-strip buried under the source region. In this figure, each current flowline represents 5% of the total current. It is clearly shown that the parasitic *npn* transistor is turned on in the conventional structure. The lateral flowlines at the bottom of the n^+-source generate the body-to-source voltage that eventually turns the transistor on; simulation also shows the behaviour in the event of a snapback breakdown. In contrast, the current flowlines as shown in Fig. 7*b* are shunted by the buried p^+-strip because of its low resistance.

Fig. 8 gives the doping profiles along the n^+-source centre-line of the simulated devices, with different doping concentrations of the p^+-strip, the corresponding I_{ds} against V_{ds} curves are also illustrated in the same figure. With p^+-strip peak concentration increased to over 1×10^{19} cm^{-3}, the snapback behaviour could be avoided.

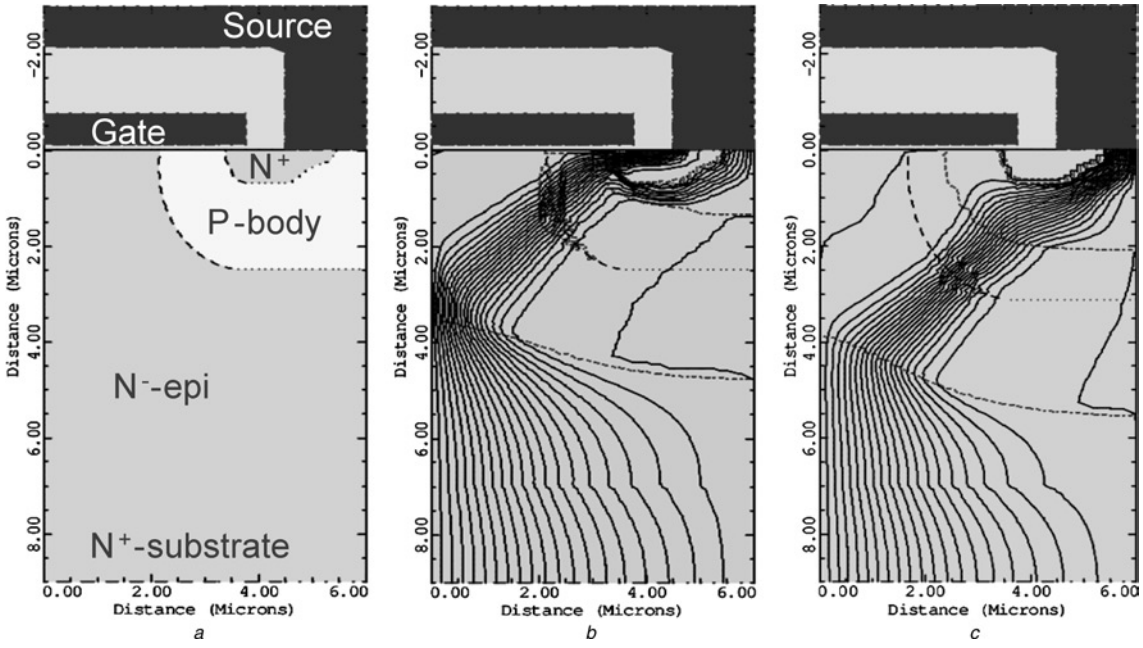

Fig. 7 *Effectiveness of p^+-buried layer*

a Half structure of a simulated conventional n-VDMOS device
b Its 5% flowlines upon snapback breakdown
c 5% flowlines of the p^+-strip buried device without snapback breakdown

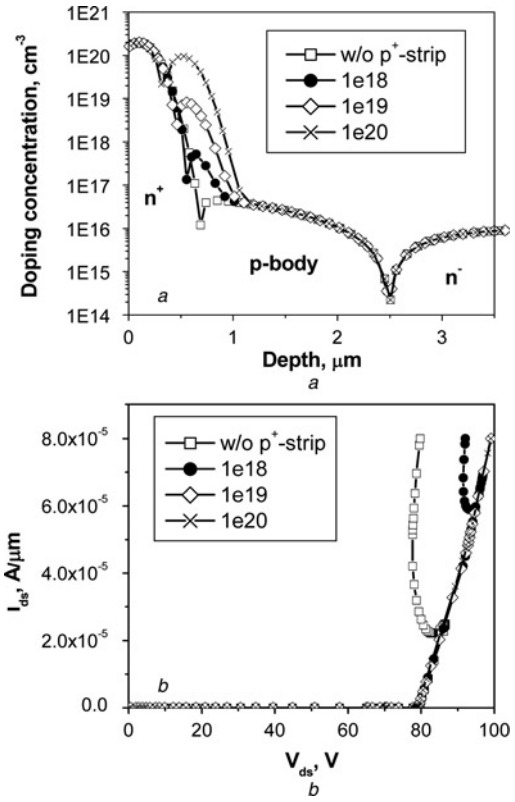

Fig. 8 *Improvement of drain current behaviour by introducing confined p^+-strip underneath n^+-source*

a Doping profiles along the n^+-source centre-line
b Breakdown behaviour

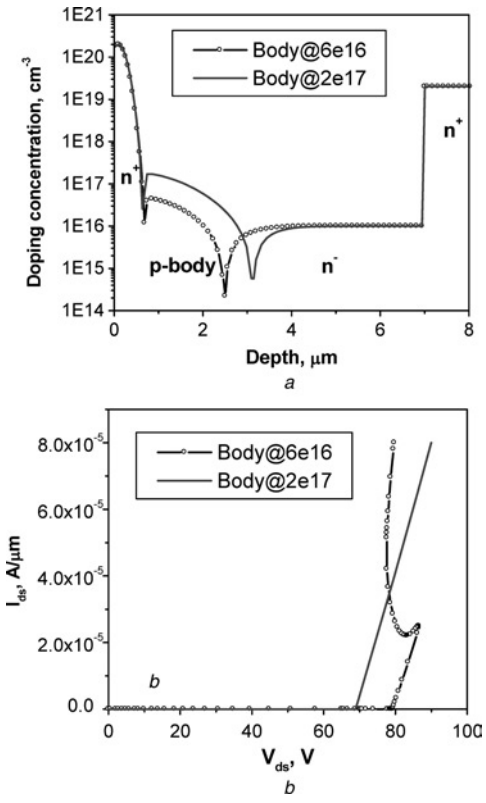

Fig. 9 *Improvement of drain current behaviour by increasing p-body peak concentration*

a Doping profiles along the n^+-source centre-line
b Breakdown behaviour

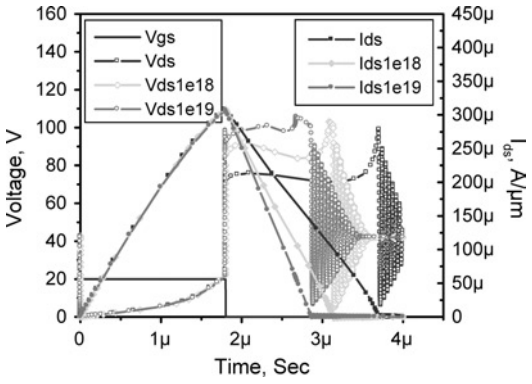

Fig. 10 *Waveform of devices with different p^+-strip peak concentrations during UIS switching*

Oscillations indicate numerical instability at the end of the simulation

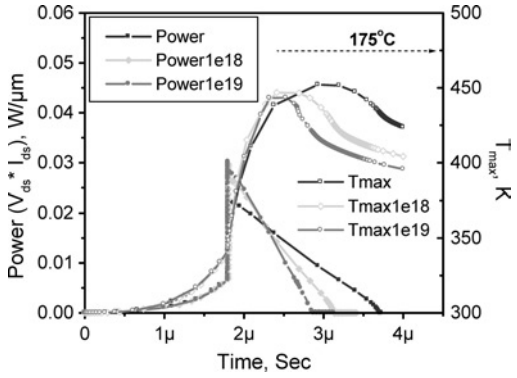

Fig. 11 *Transient of instantaneous power consumption and maximum lattice temperature during UIS switching of devices with different p^+-strip peak concentrations*

Note the device is referred to be burned if T_{max} reaches 175 °C

Simulation also confirms that device channel length, threshold voltage as well as the drain-to-body capacitance (C_{gd}) remain the same.

In contrast, Fig. 9 shows the doping profiles along the n^+-source centre line of the reference devices with different p-body doping concentration and their $I_{ds} \sim V_{ds}$ curves. Increasing the p-body doping concentration from 6×10^{16} to 2×10^{17} cm^{-3} can also suppress snapback behaviour. However, this decreases the device breakdown voltage from 72 to 65 V. The threshold voltage increases from 3.1 to 5.8 V while the channel length also increases from

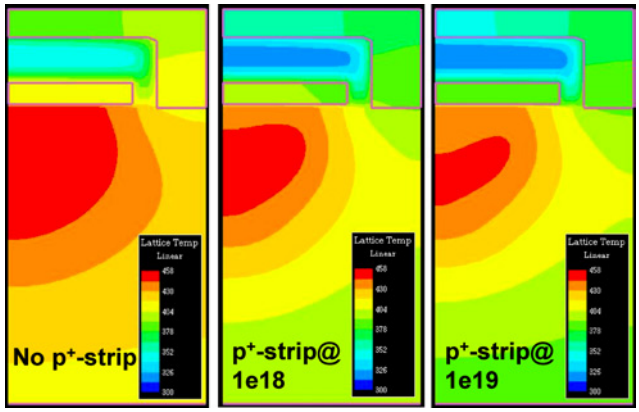

Fig. 12 *Temperature contours of devices with different p^+-strip peak concentrations when T_{max} reaches its peak during UIS simulation*

1.36 μm to 1.76 μm. As a result, the device's on-resistance increases. Moreover, it also increases C_{gd}, which is the dominating factor in VDMOS that slows down the device switching speed. Therefore, increasing the *p*-body doping concentration is not a good approach to improve device ruggedness.

Since the potentially destructive DC snapback breakdown behaviour can be triggered by a UIS event, it would be appropriate to simulate UIS characteristics. UIS simulations were also carried out using MEDICI. Fig. 10 shows the waveform generated during UIS switching. The instantaneous power and maximum lattice temperature (T_{max}) in the simulated device are also plotted in Fig. 11 as a function of time. Under the same UIS switching condition, I_{ds} drops quicker with increasing p^+-strip peak concentration. As a result, the integrated energy dumped from the inductor is less and the peak T_{max} is much smaller. It is obvious that UIS energy can be increased by 24% with a p^+-strip of 10^{19} cm^{-3} so that the peak T_{max} curve is similar to that of the conventional. In other words, the UIS ruggedness is improved by about 24% if a p^+-strip of 10^{19} cm^{-3} is introduced. Fig. 12 shows the lattice temperature contour when simulated devices reach their peak T_{max}. It is clear that the device structure without the p^+-strip has a vast number of hot spots that will eventually turn-on the parasitic *npn* transistor, leading to the destruction of the device.

5 Conclusions

A simple way to improve VDMOS ruggedness without introducing factors that can degrade other performance parameters, has been presented. The new process only requires an additional, thin layer of highly doped p^+-strip underneath the n^+ source/*p*-body junction. A TCAD simulation proved its effectiveness of the p^+-strip in improving device ruggedness, an improvement of UIS ruggedness as high as 24% over the conventional device is expected.

6 Acknowledgments

The authors would like to thank Auto21, CMC, NSERC and Asahi Kasei Microsystems Inc. for the financial and technical support.

7 References

1 Johnson, C.M.: 'Current state-of-the-art and future prospects for power semiconductor devices in power transmission and distribution applications', *Int. J. Electron.*, 2003, **90**, (11–12), pp. 667–693
2 Chang, H.-R.: 'Numerical and experimental comparison of 60V vertical double-diffused MOSFETs and MOSFETs with a trench-gate structure', *Solid State Electron.*, 1989, **32**, (3), pp. 247–251
3 Kinzer, D., Ajit, J.S., Wagers, K., and Asselanis, D.: 'A high density self-aligned 4-mask planar VDMOS process'. Proc. Power Semiconductor Devices and ICs, Hawaii, USA, 1996, pp. 243–247
4 Murray, A., Davis, H., Cao, J., Spring, K., and McDonald, T.: 'New power MOSFET technology with extreme ruggedness and ultra-low RDS(on) qualified to Q101 for automotive applications'. PCIM2000, Europe, pp. 102–107
5 Philips Semiconductor Applications AN10273_1: 'Power MOSFET single-shot and repetitive avalanche ruggedness rating'. Philips Semiconductors, 2003