Self-Tuning Digital Current Estimator for Low-Power Switching Converters

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Abstract - **An inductor current estimator suitable for low-power digitally controlled switch-mode power supplies (SMPS) is introduced. The estimation of the average current value over one switching cycle is based on the analog-to-digital conversion of the inductor voltage and consequent adaptive signal filtering. The adaptive filter is used to compensate for variations of the inductance and series equivalent resistance affecting accuracy of the estimation. Based on the response to an intentionally introduced and known current step, the filter tunes its own parameters such that a fast and accurate estimation is obtained. A practical realization of the estimator resulting in a modest increase in digital controller complexity is shown. Besides a simple digital IIR filter and a load step circuit, it only requires a slow analog-to-digital converter for the input voltage measurement. The estimator is tested on a 6.5 V to 1.5 V, 15 W, digitally-controlled buck converter prototype. The results show that between 20 % and 100 % of the maximum output load the estimator has accuracy better than 10 % and one switching cycle response time.**

I. INTRODUCTION

In low-power dc-dc converters, current sensing or measurement is not only used for protection from overload conditions [1]. It is often utilized for increasing converter efficiency through multi-mode operation [2,3] and improving dynamic response [4]. Generally, the measurement methods can be categorized in voltage drop and observer based methods. In voltage drop based methods, a current passing through a sense-resistor or a MOSFET is extracted from the voltage drop it causes [5]-[9]. The observer-based systems usually estimate current from the voltage across the power stage inductor [10]-[12].

In most cases, the existing methods are not well-suited for the integration with rapidly emerging digital controllers of SMPS for battery-powered portable devices, communications, and consumer electronics where the overall size, the system cost, and the overall efficiency are among the main concerns [2,3]. The voltage drop methods either decrease efficiency of the converter [5] or require a wide-bandwidth amplifier, which are very challenging to realize in the latest CMOS digital processes. This is due to very limited supply voltages of standard digital circuits (often in sub 1 V range), at which traditional analog architectures cannot be used. Hence, bulkier and less reliable multi-chip solutions each requiring a sensing circuit and controller implemented in different IC technologies. On the other hand, the observers suffer from a limited accuracy

[12,13]. The current estimation relies on prior knowledge of the inductance and equivalent series resistance values [12,13], which depend on operating conditions and change under external influences.

The main goal of this paper is to introduce a self-tuning current estimator, shown in Fig.1, which utilizes flexibility of digital implementation to compensate for the changes in the inductor parameters. The estimator is also fully implantable in the latest digital CMOS technologies allowing for a simple integration with the upcoming digital controllers.

In the following sections the basics of the inductor voltage based current estimation are briefly reviewed and the principle of the operation of the self-tuning digital estimator is explained. In Section III we address practical implementation challenges and a solution for them. In the final section results obtained with a digitally-controlled buck converter prototype verifying accurate and fast operation of the new estimator are demonstrated.

II. PRINCIPLE OF OPERATION

Figures 2.(*a*) and 2.(*b*) are used to explain the principle of operation of both the conventional analog current estimator [12] and the self-tuning digital system introduced in this paper. In the analog implementation of Fig.2.(*a*), the inductor current $i_L(t)$
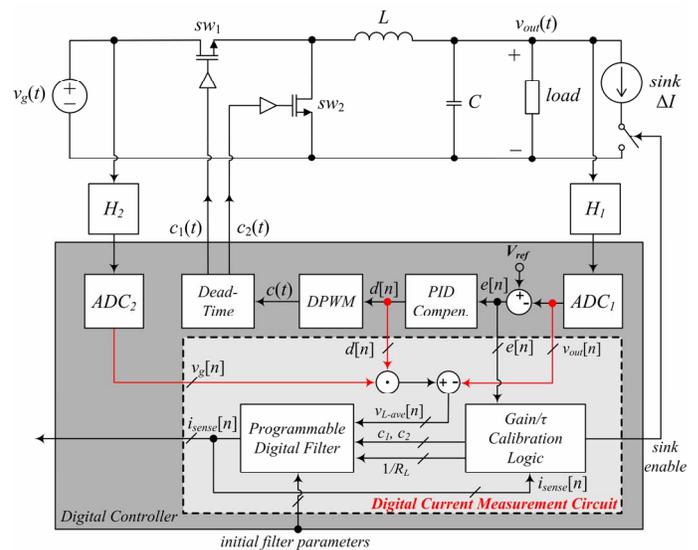
Fig. 1. A digitally-controlled buck converter with the self-tuning current estimator.

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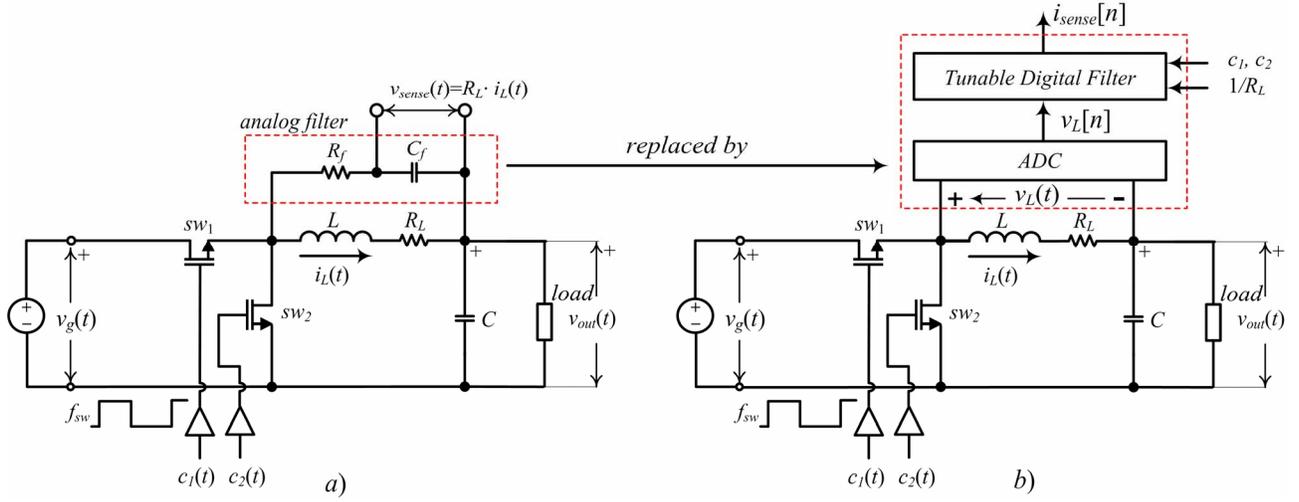
Fig. 2. Current sensing techniques: *a)* conventional analog implementation *b)* implementation with a self-tuning digital filter.

is extracted by placing an *R-C* filter in parallel with the power stage inductor and measuring the filter's capacitor voltage $v_{sense}(t)$. The relationship between the voltage and the inductor current is given by the following transfer function:

$$V_{sense}(s) = I_L(s) \cdot R_L \cdot \frac{1 + s \cdot \dfrac{L}{R_L}}{1 + s \cdot R_f C_f} = I_L(s) \cdot R_L \cdot \frac{1 + s \cdot \tau_L}{1 + s \cdot \tau_f}, \quad (1)$$

where L and R_L are the inductance and its equivalent series resistance values, respectively, and R_f and C_f are the values of the filter components. When the filter parameters are selected so that $\tau_f = R_f \cdot C_f = L/R_L = \tau_L$, the capacitor voltage becomes an undistorted scaled version of the inductor current (the zero and pole cancel each other). This allows the inductor current to be reconstructed from the capacitor voltage measurements.

As mentioned earlier, the main drawback of this method is that the inductor parameters are not exactly known and do change in time, often causing large errors in the estimation [13]. To compensate for these variations, an analog filter with programmable resistive networks is proposed in [14], [15] where, in the later publication, an on-chip implementation of the filter is shown. Even though the method significantly improves the estimator accuracy, its implementation still requires a relatively large number of analog components, making it less suitable for the integration with digital controllers or low-power SMPS.

In the new estimator of Fig. 2 (*b*) the analog filter is replaced with a fully-digital equivalent, where in contrast, the digital filter is tunable. In this implementation, the voltage across the inductor is converted into a digital value $v_L[n]$ and then processed in the digital domain, to result in the output value $i_{sense}[n]$ directly proportional to the inductor current.

By manipulating (1) and applying a bilinear transformation the following difference equation for the digital filter can be derived:

$$i_{sense}[n] = \frac{1}{R_L} \cdot \{c_1 \cdot i_{sense}[n-1] + c_2 \cdot (v_L[n] + v_L[n-1])\}, \quad (2)$$

where c_1 and c_2 are filter coefficients:

$$c_1 = (2 \cdot \frac{L}{R_L T_s} - 1)/(1 + 2 \cdot \frac{L}{R_L T_s}), \quad (3)$$

$$c_2 = (1 + 2 \cdot \frac{L}{R_L T_s})^{-1}, \quad (4)$$

and T_s is the filter sampling rate. The estimator adjusts the filter gain factor $1/R_L$ from (2) and coefficients c_1 and c_2 through a self-calibrating process. It is obtained with the help of a test current sink connected at the converter output, as shown in Figs. 1 and 3. Periodically, the sink, which can be implemented with a known resistor and a small switch connected parallel to the load, turns on for a short time. Then, based on the response of the filter, the *Gain/τ Calibration Logic* block adjusts the filter gain and coefficients so that the increase in $i_{sense}[n]$ corresponds to the exact increase in the load current. The calibration technique introduced here is similar to that one presented in [15] where a known test current is injected into the inductor during the converter start-up phase for the purpose of calibrating an analog filter for current estimation. However, the limitation of the test current injection method [15] is that it cannot be used during regular converter operation because it requires that both converter switches are turned off during the filter calibration phase. Since the series inductor resistance R_L and inductance L dynamically change,
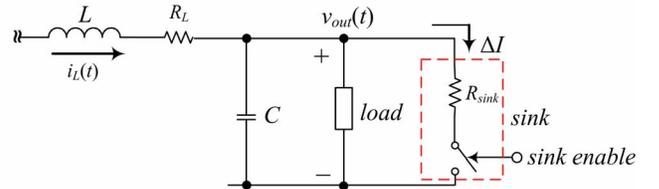
Fig. 3. Test current sink used for the filter calibration.

due to variations of converter operating conditions (e.g. output load current or temperature), the accuracy of the current estimation might be compromised.

Since the current sink of Fig. 3 does not require any change in converter operation, the method we present here can be used during normal converter operation and the calibration can be performed regularly.

III. PRACTICAL IMPLEMENTATION

Even though the principle of operation of the self-tuning digital estimator is relatively simple, its practical implementation is not so straightforward. Seemingly, it requires a very fast ADC, with sampling rate significantly higher than the switching frequency, as well as an equally fast processor for the filter implementation. Each of these can make the presented estimator impractical for the cost-sensitive low-power applications.

The precision and speed of the estimator depend on the accuracy of the measurement of the average value of the inductor voltage. Even a small error in the measurement can cause a large estimation error. To obtain a fast estimation, the accurate measurement of the inductor voltage over one switching cycle is required. It could be done with an ADC converter whose sampling rate is much higher than the switching frequency. The need for a very high sampling rate converter can be described through Fig.4, showing the inductor voltage of a buck converter as well as its gate drive signal $c_1(t)$ and the sampling signal of a fast ADC. In this case, the average value of the inductor voltage can be calculated by summing the sampled voltage values and dividing the result with the number of samples taken during one switching cycle. However, as it can be seen from Fig.4, the accuracy of this approach strongly depends on the number of samples taken, especially if the samples are not perfectly aligned with the inductor voltage transition point.

To eliminate the need for the fast ADC, the input voltage of the power stage $v_g(t)$ is sampled at a rate lower than switching frequency and the average value of the inductor voltage is calculated as:

$$v_{L-ave}[n] = d[n] \cdot v_g[n] - v_{out}[n], \qquad (5)$$
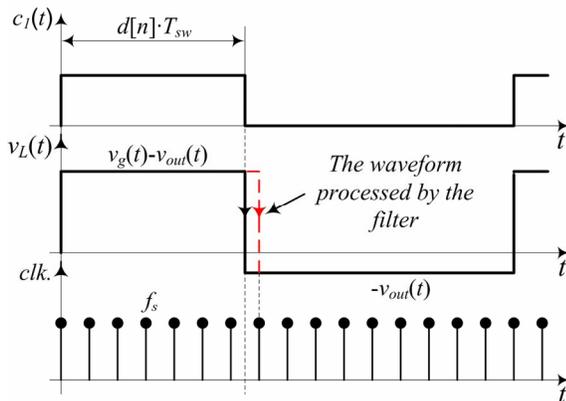
Fig. 4. Signals of a system implemented with an over-sampling ADC.

where $d[n]$ is DPWM's control variable and $v_{out}[n]$ is the converter output voltage, both of which are readily available in the control loop of Fig.1. The $v_{out}[n]$ is provided by the already existing ADC of the voltage control loop and the duty ratio is provided by the digital PID compensator. A lower sampling rate is possible because in the targeted battery-powered applications the input voltage often changes in a very slow fashion. It should be noted that the complete implementation of the new estimator, including ADC-s is possible in standard CMOS processes. Recent publications [2], [3], and [16] show application-specific ADCs for SMPS that are fully implantable in the latest low-voltage technologies.

A. Filter Architecture and Self-Calibration

The calculation of the average voltage described in the previous subsection reduces hardware requirements but at the same time affects the estimation accuracy. The actual average inductor voltage might differ from (5), due to the action of non-overlapping, i.e. dead-time circuit, and other parasitic effects. To compensate for this effect, as well as for the previously mentioned variations in the inductor values, a current sink and Gain /τ Calibration Logic (Fig.1) are used to tune the parameters of the infinite impulse response (IIR) digital filter, whose more detailed block diagram is shown in Fig. 5. The calibration of the filter coefficients described with (2) is performed in two phases.
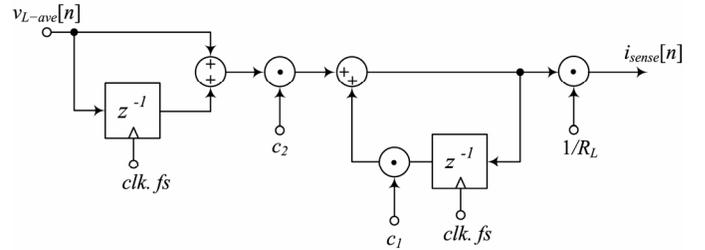
Fig.5. The architecture of the tunable IIR filter used in the current estimator.

In the first phase, a known load current step is introduced by the sink and the accurate value $1/R_L$ is found from the variation in the estimated inductor current.

In the next phase, another current step is introduced and the time constant $\tau_L = L/R_L$, determining coefficients c_1 and c_2 are calculated from the estimator output overshoot/undershoot.

A more detailed description of the calibration procedure is given in the following subsection.

A1. Filter Calibration Procedure

The block named *Gain /τ Calibration Logic*, shown in Fig. 1, periodically performs calibration procedure. The value of $1/R_L$ is determined from the difference between two steady state current values, estimated before and after a load step is applied as shown in Fig.6.

The initial steady state is detected by monitoring the error signal $e[n]$ and at the time instant A (Fig.6), the current, before the transient, is estimated $I_1=i_{sense}[n]$ and stored in a register.
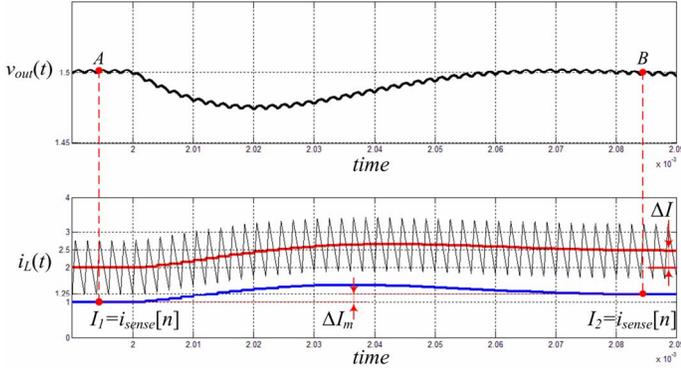
Fig.6. R_L calibration procedure: simulated response of the current estimator during output load change for two cases (bottom) the initial value of R_L is half the actual value (top) after the filter adjustment.

After a step ΔI is introduced and steady state reached again the new current $I_2 = i_{sense}[n]$ is found and difference ΔI_m

$$\Delta I_m = I_2 - I_1 \qquad (6)$$

is calculated. The calculated difference is then compared to the actual value of the current step and the actual value of R_L is calculated as:

$$R_L = \frac{\Delta I_m}{\Delta I} R_{L\_inital}, \qquad (7)$$

where R_{L_inital} is the initially set resistance value.

The uncertainty of an actual inductor value L affects the time constant τ_f (1) and therefore the time response of the filter. This effect is demonstrated in Fig. 7 showing the actual and estimated inductor currents during a load step for three different time constants: the actual time constant τ_L, and ± 50 % of this value. It can be seen that the estimated current accurately follows $i_L(t)$ only when a proper set of filter coefficients for the actual inductor value L is set. In two other cases, the estimated current exhibits overshoot for τ_f smaller than actual value and undershoot when τ_f is larger.

The calibration of the τ_f is performed during the transient, at the output voltage valley point (time instant B in Fig.7), where the inductor current is equal to that of the load [17,18]. At this time instant the estimated current is compared with the expected value $I_1 + \Delta I$ and tuning of the filter time constant is performed.

IV. EXPERIMENTAL SYSTEMS AND RESULTS

An experimental system was built based on the diagrams shown in Figs.1, 3, and 5. The power stage is a 15-W, 1.5-V buck converter, switching at f_{sw}=500 kHz, with the input voltage ranging between 2.6 V and 6.5 V. The digital filter, calibration logic and controller are realized with an Altera DE2 FPGA board. Two external ADCs sampling at f_{sw} and $f_{sw}/10$ are used for output and input voltage measurements respectively. The test current sink was set to produce a 500 mA pulse, which is only 5% of the maximum output current. To visualize the

operation of the estimator, its digital output was sent to a flash digital-to-analog converter (DAC) and the resulting analog signal was observed.

A. R_L Calibration

Figure 8 and its zoomed version, Fig.9, show closed loop
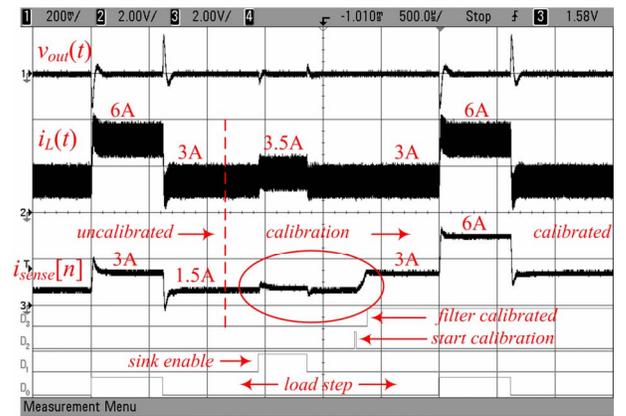
Fig.8. The system operation – Ch1: Output converter voltage (200mV/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; D0-D3- control signals; Time scale is 500μs/div.
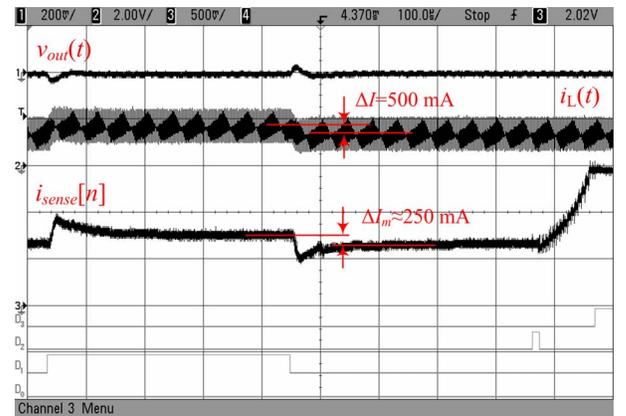
Fig.9. The calibration procedure using a 0.5A current sink – Ch1: Output converter voltage (200mV/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; D0-D3- control signals; Time scale is 100us/div.

Fig.7. Calibration of the time constant: simulated response of the current estimator during output load change between 2 A and 2.5A; (top) for τ_f=0.5τ_L; (middle) for τ_f=τ_L ; (bottom) for τ_f=1.5τ_L .

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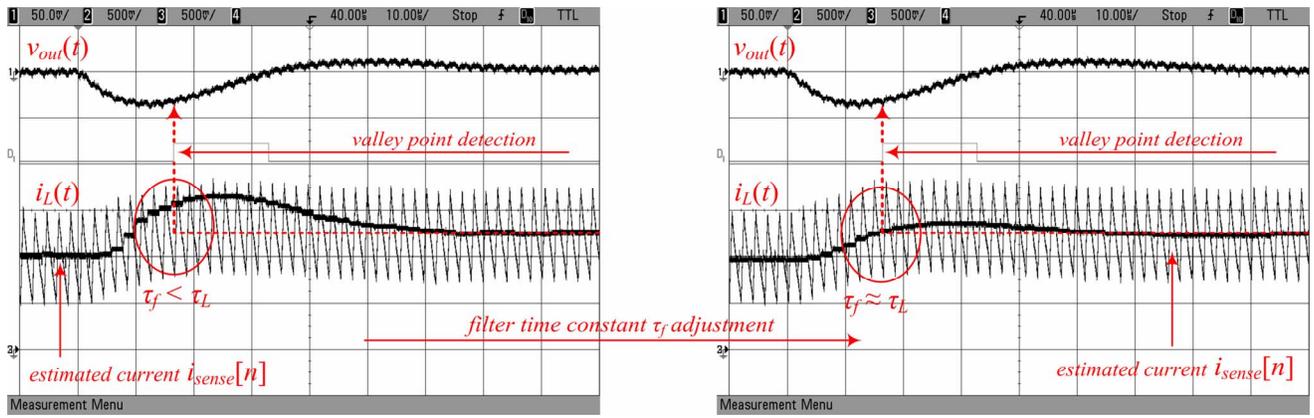
Fig.10. The estimator IIR filter time constant τ_f is tuned (left) iteratively to match the inductor time constant τ_L (right): Output converter voltage (50mV/div); Ch2: actual inductor current $i_L(t) - 2$ A/V; Ch3: estimated average current $i_L[n] - 2$ A/V; Time scale is 10μs/div.

operation of the controller during load transients between 3 A and 6 A and demonstrate self-tuning process of the estimator. In the first (uncalibrated) phase due to the mismatch in equivalent series resistance R_L, the gain $1/R_L$ and coefficients of the estimator are not properly adjusted and an error of approximately 100 % in the current estimation occurs (the step is wrongly recognized as a 1.5A to 3A transition). In the second (calibration) phase, a 0.5 A test-current step is introduced and the filter gain and the coefficients of the filter are tuned accordingly. The third phase shows repeated load transient, where the average current is estimated accurately, verifying the effectiveness of the self-tuning filter and the estimator operation.

B. Filter Time Constant Calibration

Tuning process of the filter time constant τ_f due to the variation of the inductance value L is demonstrated in Fig. 10. Initially, the filter time constant τ_f is half the inductor time constant τ_L and the estimated current exhibits an overshoot above the expected steady-state value at the output voltage valley point. This is recognized by the gain/τ calibration logic which automatically increases time constant τ_f by readjusting filter coefficients c_1 and c_2 until the time constants are closely

matched as shown in Fig. 10 (right).

C. Calibrated Operation

Figs. 11 and 12 demonstrate fast operation of the estimator when both gain and time constant are properly tuned. They compare actual and estimated inductor current during both light-to-heavy and heavy-to-light load change between 3 A and 6 A. As it can be seen, the average value of the current over one switching cycle is accurately estimated without significant delay, allowing the estimator to be used for overload protection and power stage efficiency optimization.

D. Overload Protection

A simple overload protection of the converter circuitry can be obtained by comparing the output of the current estimator with a predefined digital current threshold. Once the estimated current exceeds the threshold value, to prevent the converter damage, it is immediately turned off and the estimator stops its operation as shown in Fig 13. In Fig. 13, the output load current is intentionally increased from 2 A to 7.5 A above the threshold of 7 A. Therefore the overload protection signal is activated and the converter is rapidly turned off.

Fig.11. The estimated current during light-to-heavy load step between 3A and 6A– Ch1: Output converter voltage (200mV/div); Ch2: actual inductor current $i_L(t) - 2$ A/V; Ch3: estimated average current $i_L[n] - 2$ A/V; Time scale is 10μs/div.
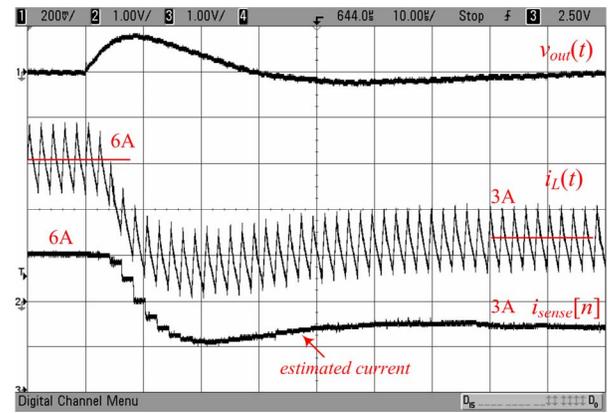
Fig.12. The estimated current during heavy-to-light load step between 6A and 3A– Ch1: Output converter voltage (200mV/div); Ch2: actual inductor current $i_L(t) - 2$ A/V; Ch3: estimated average current $i_L[n] - 2$ A/V; Time scale is 10μs/div.
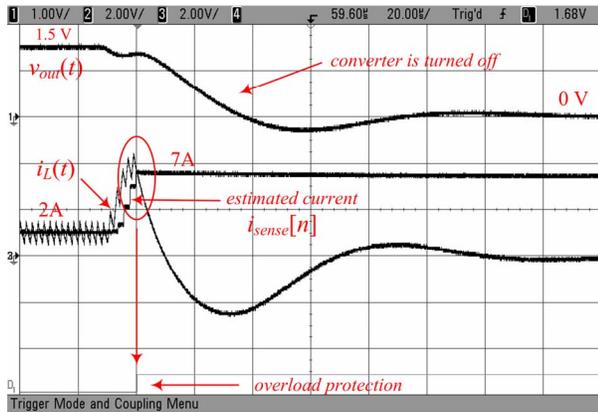
Fig.13. The overload protection implemented with the current estimator–Ch1: Output converter voltage (1V/div); Ch2: actual inductor current $i_L(t)$ – 2 A/V; Ch3: estimated average current $i_L[n]$ – 2 A/V; Time scale is 20μs/div.

E. Accuracy

The accuracy of the current estimator is tested by changing the output load current between 0.5A and 10.3A (maximum load) and monitoring the estimated current. The obtained data is shown in Fig. 14. It can be seen that the current estimator has accuracy better than 10% between 20% and 100% of the maximum load current with 5% accuracy at the maximum load current. These results are comparable to the most recent analog solutions.
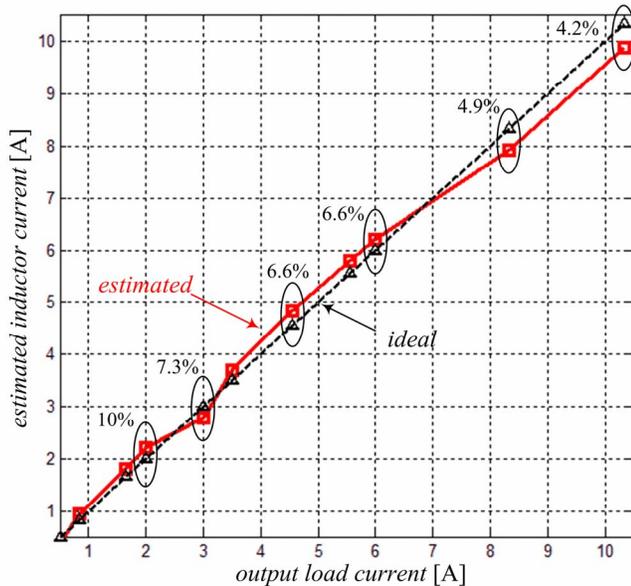
Fig. 14. Estimated inductor current versus the output load current

V. CONCLUSION

A self-tuning current estimator suitable for integration with digital controllers of low-power SMPS is introduced. Based on the measurement of inductor voltage and its processing in digital domain the estimator calculates the average value of the inductor current over one switching cycle. To compensate for the variations in inductor parameters, limiting accuracy of equivalent analog methods, the estimator automatically adjusts its coefficients using a test current sink and a tunable IIR filter. The fast and accurate operation of the estimator is demonstrated on a digitally controlled buck converter prototype.

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