ANALOG-TO-DIGITAL CONVERTER FOR INPUT VOLTAGE MEASUREMENTS IN LOW-POWER DIGITALLY CONTROLLED SWITCH-MODE POWER SUPPLY CONVERTERS

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Abstract - *This paper introduces a practical analog-to-digital (ADC) converter architecture for the input voltage measurements in low-power digitally controlled switch-mode power supplies (SMPS). The ADC utilizes known reference voltage and a duty ratio of a simple circuit mimicking operation of the converter to obtain the information about the input voltage value.*

The functionality of the ADC is verified through a discrete implementation, with a 1.5 V/3 W buck converter based experimental prototype. A better than 1.5% accuracy is observed over the entire 1.8 V to 3.3 V input voltage range. A small silicon size of about 0.025mm^2 is also estimated, based on the synthesized digital logic and already existing on-chip integrated system functional blocks.

Keywords - «Digital control», «High frequency power converter», «Voltage sensor», «Integrated Circuit (IC) »

I. INTRODUCTION

In numerous digitally controlled low-power switch-mode power supplies (SMPS), accurate input voltage information is usually needed. It is utilized in advanced controllers for obtaining fast dynamic response [1] and dynamically improving SMPS power processing efficiency [2]. Furthermore, emerging digital control features such as estimation and parameter extraction, auto-tuning, and power supply "health monitoring" usually need information about the input voltage value [1]. To obtain a digital equivalent of the input voltage, which can vary over a wide range, conventional general-purpose ADCs [3] are not the most suitable solution. The silicon size and power consumption of these systems are often significantly larger than those of the entire application specific controller [4] and, as such, prohibitive in the targeted low-power cost-sensitive application.

Hardware-efficient application specific ADCs for the SMPS output voltage measurement consuming low power and taking a very small fraction of the controller silicon area [5]-[8] are not suitable for this application. They operate around a confined output voltage reference window and cannot cover much wider range of the input voltage variations. Therefore, alternative hardware-efficient architectures of the input voltage acquisition are needed.

The main goal of this paper is to introduce a simple and accurate ADC architecture suitable for digitizing a wide range of input voltages. The ADC, shown in Fig.1, obtains information about the input voltage from an RC based circuit mimicking operation of an ideal buck converter.

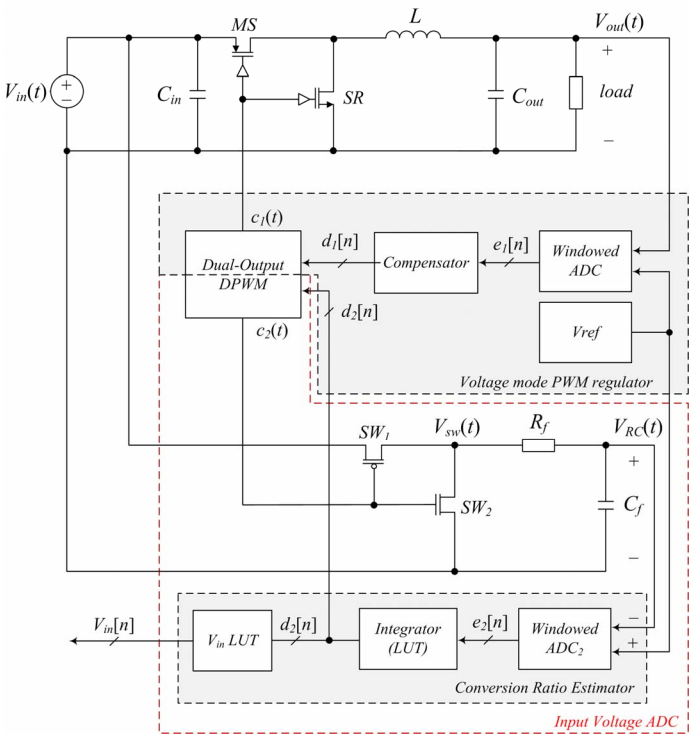

Figure 1. Proposed ADC architecture (outlined in red) used in conjunction with a voltage mode PWM controlled buck converter.

In the following section operation of the new ADC architecture is described. A practical implementation of the ADC is shown in Section III. In this section, an estimation of the silicon size needed for on-chip implementation is given as well. Section IV describes an experimental system implementation and presents results verifying a fast and accurate ADC operation.

II. Principle of Operation

Ideally, in a lossless buck converter operating with a feedback loop containing an integrator the input voltage V_{in} can be estimated based on the steady state duty ratio value D and the reference voltage V_{ref}, as

$$V_{in} = \frac{V_{ref}}{D} . \tag{1}$$

For a realistic converter of Fig.1, containing switching and conduction losses that affect the duty ratio value, such a simple estimation of the input voltage cannot be achieved. The duty ratio of the realistic converter changes with the load current and cannot be directly used for an accurate input voltage measurement.

To overcome this problem in the system of Fig.1, an *RC*-based circuit mimicking the dc operation of an ideal closed-loop buck converter, from the conversion ratio perspective, is placed next to the main feedback loop of the buck converter. The *RC* circuit is driven with a set of small complementary transistors SW_1 and SW_2 and their operation is controlled with a digital feedback loop containing a small windowed based ADC (ADC_2), an integrator, and one port of a dual digital pulse-width modulator (*DPWM*). All of these elements and a look up table of Fig.1 form the new ADC architecture for the input voltage measurement.

The feedback loop of the input voltage ADC produces the duty ratio control value $d_2[n]$ that regulates the operation of the switches. The switches are controlled such that the output voltage of the *RC* filter has the same dc value as the main buck stage, i.e. $<V_{RC}(t)> = V_{ref} = d_2 V_{in}$, as shown in Fig.2 that also demonstrates other key waveforms of the *RC* filter.

Then, the digital equivalent of the analog input value $V_{in}[n]$ is found by mapping $d_2[n]$ through the look up table implementing the following nonlinear equation:

$$V_{in}[n] = V_{ref} / d_2[n]. \tag{2}$$

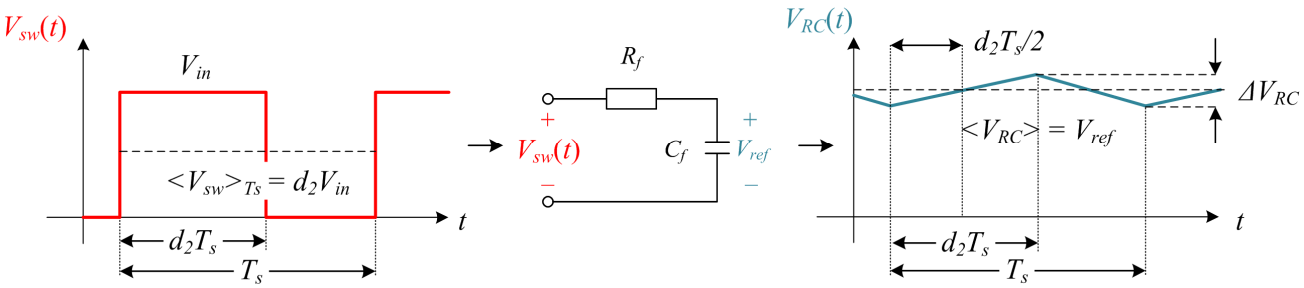

Figure 2. Idealized converter voltage waveforms illustrating the basic concept of operation.

III. Practical Implementation

The practical implementation of the proposed ADC architecture is explained in the following section. Since the ultimate goal is an IC implementation, special emphasis is given to potential CMOS process integration and design optimization. The sizing of the RC filter and selection of its transistors are described in the first subsection, followed by a detailed

analysis of the main digital blocks of Fig.1, namely the *ADC$_2$ and* the *Dual DPWM.* Potential quantization effects are addressed and design guidelines for achieving a desired accuracy are given. The final subsection is dedicated to the area requirements for a potential IC implementation.

A. RC output filter and logic-level transistor sizing considerations

The sizing and selection of the output filter and switching transistors are relaxed due to the fact that the idealized converter, i.e. RC circuit, does not have a load. In addition, it is only necessary to regulate the average output voltage equal to the reference voltage for proper operation, as described in section II. As such, the output filter needs only to have a bandwidth sufficiently less than the converter switching frequency in order to eliminate potential digital aliasing effects [9], based on general guidelines for the mixed-signal filter circuit design. The selection of the filter resistor and capacitor R_f and C_f also depends on the IC implementation technology and tradeoffs between the silicon size and power consumption of the filtering circuit for IC implementation.

Once the R_f value is calculated the logic-level transistors can be sized such that the conversion ratio between the input and output does not deviate significantly from (2). The new conversion ratio can be derived using steady-state analysis [10] of the non-ideal converter circuit shown in Fig 3.

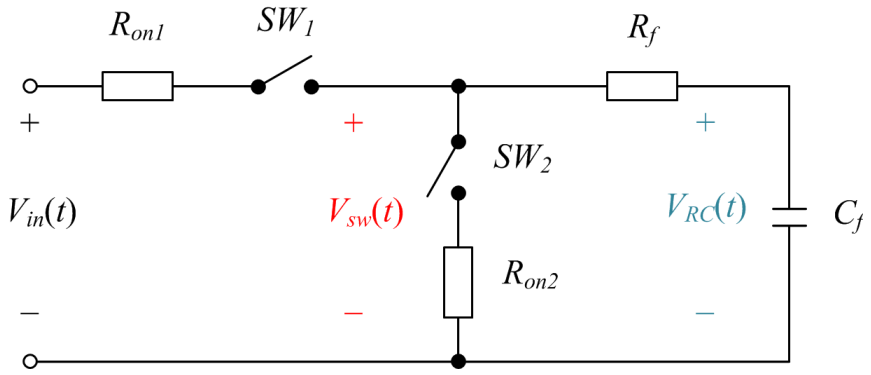

Figure 3. Idealized converter with transistor conduction losses

The new conversion ratio becomes

$$\frac{V_{in}}{V_{RC}} = \frac{1}{D} \cdot \left(1 + \frac{D' \Delta R_{on}}{R_f + R_{on2}}\right), \tag{3}$$

where ΔR_{on} is the difference between R_{on1} and R_{on2}. From (3) it is clear that compact transistors (ie. with relatively large on-resistances) can be utilized as long as fair matching can be maintained, without an impact on the accuracy. In fact, the error contribution can be kept below 0.1% for most of the standard implementation technologies.

B. Digital Logic

This subsection is devoted to the two main digital logic blocks of the proposed ADC architecture, the *Windowed ADC2* and *DPWM* respectively. Due to the presence of SMPS digital controllers in the targeted applications, a special emphasis on potential hardware sharing is made.

B1. Windowed ADC

In order to regulate the output filter voltage $V_{RC}(t)$ equal to the reference voltage V_{ref}, a subtraction block is required to detect significant deviations between the two values. Since the input voltage variations are usually of the small-signal kind in low-power application, ie. powered by a slowly (dis)-charging portable energy source, the resolution of the *Windowed ADC$_2$* can be minimal (2bit). As a result, application-specific windowed ADCs with a small silicon area and

power consumption requirements can be utilized, such as an all-digital delay-line based ADC [8] shown in Fig. 4. The silicon area required of such an ADC in 0.18 micron technology is 0.011 mm^2 [8] (0.008 mm^2 in 0.13 micron technology), which is 14 times smaller compared to a state of the art analog controller, typically taking around 0.15 mm^2 of silicon area [4] (0.3 mm^2 in 0.35 micron technology). A potential modification of the delay-line based ADC architecture, combining the output voltage ADC and the *Windowed ADC$_2$* block, might be possible as shown in Fig. 5. In this case in addition to the *Reference delay line* and $V_{out}(t)$ *measurement delay line*, a third delay line for the *Windowed ADC$_2$* block is added.

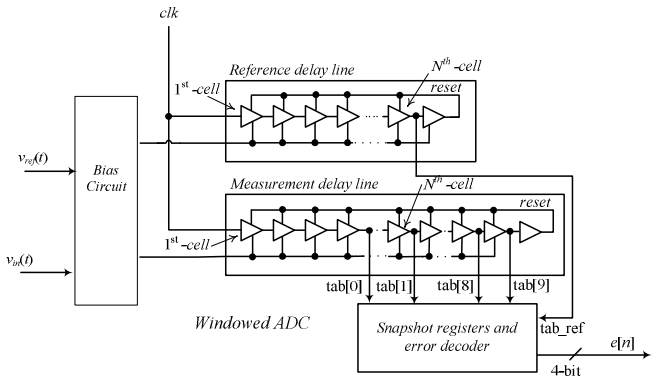

Figure 4. Delay-line based ADC

Since, the mimicking circuit potentially can operate at a higher switching frequency than the buck converter, to minimize the RC filter size a faster ADC conversion time than that of the buck voltage loop ADC might be needed.

This increase in the speed of the converter can be achieved by having the additional delay shorter than other lines, saving silicon area and power consumption. A *clock divider* can be utilized to sample the output voltage at the converter switching frequency which is slower than the operating frequency of the idealized converter. The modification of existing delay-line based ADC architecture is expected to increase the required silicon area by 25%, while combining the output voltage ADC with the *Windowed ADC$_2$* block. Alternatively, a simple two-comparator flash ADC can be used to implement the *Windowed ADC$_2$* block.

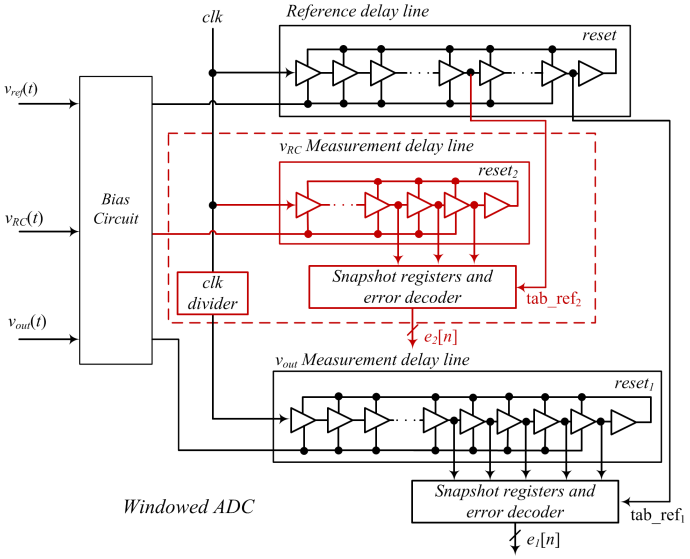

Figure 5. *ADC$_2$* block combined with delay-line ADC. Additional logic is highlighted in red.

B2. Dual-Output DPWM

While many different DPWM architectures exist to generate transistor control signals with a given resolution [11]-[14], most practical implementations are based on a hybrid configuration with a coarse and fine component. This type of configuration lends itself to straightforward hardware sharing for multiphase systems [12], such as the one targeted in this paper. By reusing the common digital logic the overall power consumption and area can be reduced as shown in Figure 6.

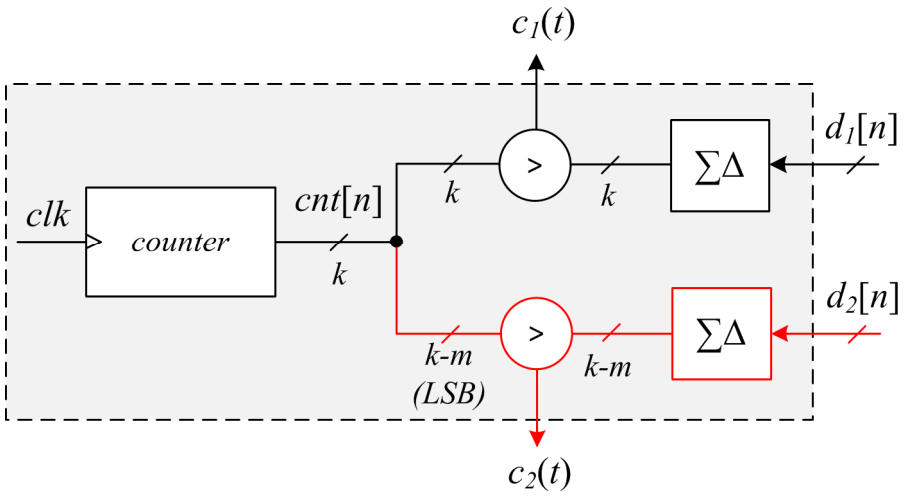

Figure 6. Dual output DPWM implementation, with the additional logic highlighted in red

In the above implementation the counter is re-used between the two control loops of Fig. 1, while an additional coarse 2nd order sigma-delta block and *greater than logic* are added. It should be noted that the two loops can operate at different frequencies if required, ie. to reduce the output filter size of proposed ADC, by simply utilizing a subset of bits from the counter. By comparing the $d_2[n]$ duty value to the *k-m* LSB bits of the counter the loop can operate at a frequency *m* times higher than the converters switching frequency. In addition, in order to compensate for the reduced counter resolution the sigma-delta can be utilized to implement a higher effective average DPWM resolution [13].

B3. Quantization Effects

Quantization effects can play a significant role in the proper and accurate operation of digital systems. For that reason they are analyzed in this section. From (2) we can see that the accuracy of the input voltage estimates is inversely proportional to the digital duty value resolution. Further insights can be gained by analyzing the small-signal properties of (2), giving us

$$(V_{in} + \Delta V_{in}) \cdot (d_2 - \Delta d) = (V_{ref} \pm \frac{\Delta V_q}{2}), \tag{4}$$

where ΔV_{in} is an input voltage change, Δd is the resulting duty cycle change, and ΔV_q is the *Windowed ADC*$_2$ quantization voltage. If we treat the Δd as the minimum duty cycle variation (DPWM resolution), then we can ensure limit-cycle free operation [11] as long as the quantization voltage ΔV_q is greater than

$$\Delta V_q = \Delta d \cdot V_{in}^{MAX}, \tag{5}$$

where V_{in}^{MAX} is the maximum input voltage. By combining (2), (4) and (5) we can derive the relationship between the maximum input voltage estimate error and the DPWM resolution, given by

$$error = \frac{\Delta V_{in}}{V_{in}} = \frac{\frac{V_{in}^{MAX}}{2V_{in}} + 1}{\frac{V_{ref}}{V_{in}}\frac{1}{\Delta d} - 1} \approx \frac{\Delta d}{V_{ref}} \cdot (\frac{V_{in}^{MAX}}{2} + V_{in}). \tag{6}$$

The worst-case error will occur when the input voltage is maximum and is illustrated in Fig. 7. For example, in the experimental system of the following section, where the input voltage is 3.3V and the reference voltage is 1.5V, an 0.1% error contribution due to the transistor on-resistance mismatch is also included.

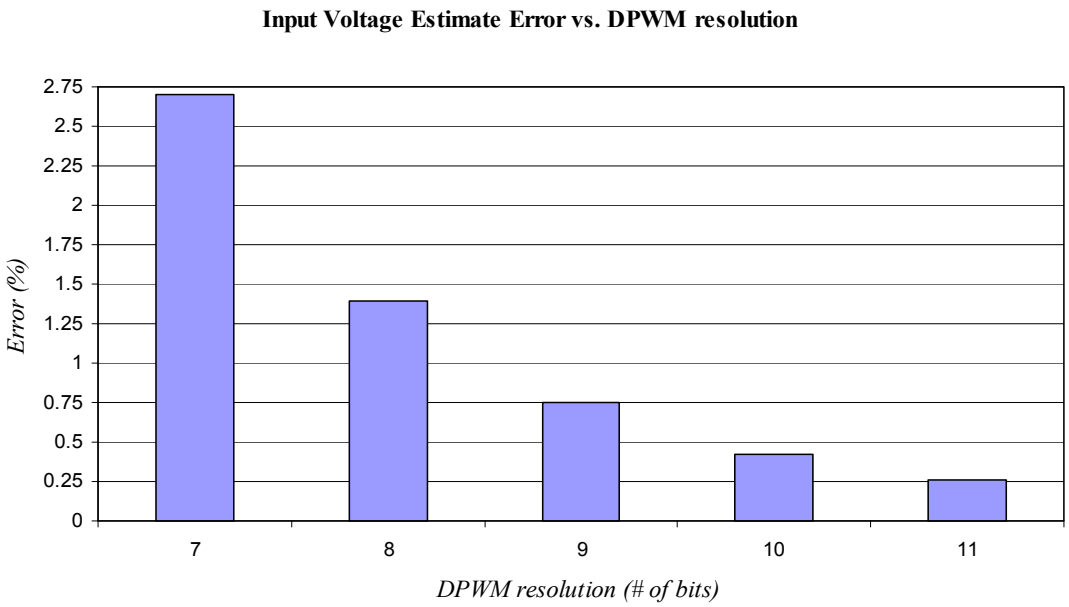

Figure 7. Input voltage estimate error as a function of the DPWM resolution

C. Area requirement for IC implementation

In order estimate the size of a potential IC implementation the digital blocks and the output filter were prototyped using IBM's CMOS 0.13 µm process toolkit. The main parameters of the prototype ADC IC and the resulting silicon area consumption are shown in Table 1.

TABLE I

MAIN PARAMETERS AND ESTIMATED SILICON SIZE

CMOS process	0.13 µm
f_{sw}	500 kHz
f_{adc}	4 MHz
R_f	1.9 MΩ
C_f	0.9 pF
Subtractor resolution	20 mV (2 bits)
DPWM resolution	10 bits
DPWM area (difference)	0.0012 mm^2
Integrator area	0.002 mm^2
V_{in} *LUT* area	0.008 mm^2
Subtractor area	0.008 mm^2
Output filter area	0.005 mm^2
Total area	0.0242 mm^2

It should be noted that the switching frequency of the *RC* filter, denoted as f_{adc}, was selected to be 8 times higher than the switching frequency of the power converter in order to reduce the output filter size. The output filter bandwidth was selected to be 20 times less than f_{adc}.

IV. EXPERIMENTAL RESULTS

In order to verify the operation of the proposed system a 3W, 500 kHz 3.3V-1.8V input voltage to 1.5V output voltage dc-dc buck converter, discrete input voltage ADC and FPGA based controller prototype were implemented with discrete

components. The *Dual output DPWM* resolution has an 8 bit effective resolution for both channels. To quantify the accuracy of the proposed system two separate load conditions were applied while varying the input voltage in the range of 1.8V to 3.3V. The results are compared to the input voltage estimate obtained using only the SMPS steady-state duty ratio value, $d[n]$, referred to as passive.

Figure 8 illustrates the input voltage estimate under zero-load current condition, both methods exhibit worst case 1.5% error. Figure 9 shows the case for the maximum load condition, 2.15A. Due to the increase in conduction losses, the input voltage estimation obtained using the SMPS steady state duty ratio value ($d_1[n]$) exhibits a 20% worst-case error. On the other hand, the proposed method input voltage estimate maintains accuracy within 1.5%.

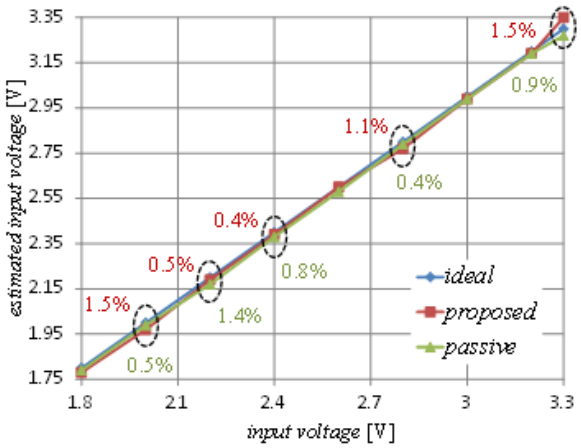

Figure 8: Input voltage estimates for zero-load current condition.

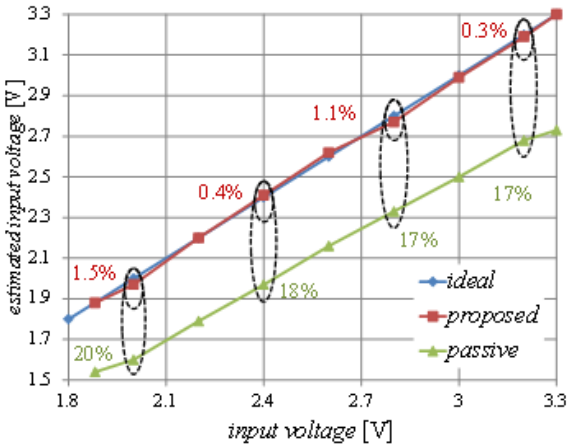

Figure 9: Input voltage estimates for 2.15-A load current condition.

To verify the dynamic performance of the proposed system, the input voltage of the converter was changed abruptly from 3V to 1.5V, the minimum possible input voltage. Then the output of the proposed ADC was fed into a DAC to demonstrate the analog comparison. As is shown in Fig. 10, the proposed input voltage ADC accurately tracks the change in input voltage and reaches the correct value within 260 us. Fig.11 presents the dynamic response for a more practical input voltage step. The input voltage ADC is able to accurately track the signal at all points.

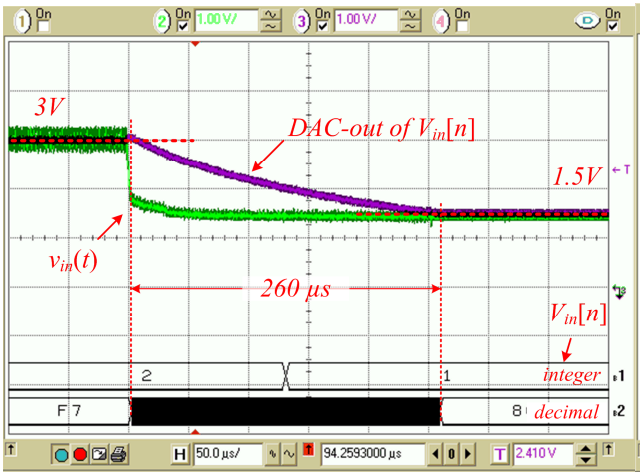

Figure 10: Input voltage tracking for the proposed ADC. The values are represented in HEX format for integer and fractional parts separately.

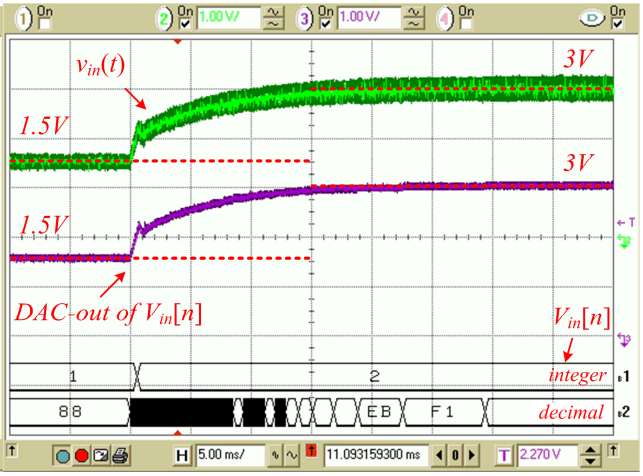

Figure 11: Comparison between the input voltage and the digital output of the proposed ADC for a practical input voltage transient.

V. CONCLUSIONS

A simple yet accurate implementation of an input voltage ADC for digitally controlled SMPS converters is proposed. The accuracy of the system is experimentally verified using a discrete buck converter over the wide operating range of input voltage and load current variation, with a worst-case measured error of 1.5%. The proposed design can easily be implemented on IC without adding significant hardware complexity, consuming only $0.025mm^2$ of silicon area using a 0.13 μm CMOS process.

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