An advanced control method for cascaded SMPS to reduce the energy storage requirements

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***Abstract*—Typical power factor correcting power supplies contain large energy storage components that filter the pulsating power that is created by an AC power source, or required by an AC power sink. This work focuses on using advanced digital control strategies to reduce the size of those energy storage components to reduce the overall size and cost of the PFC power converter.**

I. Introduction

Power factor correction (PFC) plays an integral role in any efficient alternating current power system. Rectifying PFCs are governed through standards such as the IEEE519, and the more stringent IEC61000-3-2. The IEC61000-3-2 standard applies to any piece of equipment with a power rating greater than $75W$ [1], [2], and in particular, consumer electronic devices such as laptop computers.

Inverting PFCs are becoming more popular through the proliferation of residential solar photovoltaic installations [3]. Micro-inverters provided by manufacturers such as Enphase and Enecsys are required to meet stringent power factor requirements governed by the IEEE1547 standard [4], [5].

One draw back of most existing PFC converters is the large size and cost of the energy storage components needed to simultaneously provide a constant DC output power, or input sink, and near unity power factor at the input, or output. The aim of this work is to exploit the flexibility offered by digital control hardware to greatly reduce the size of energy storage components in the power stage through advanced control methods.

The proposed controller is implemented in a PFC step down rectifier, and is shown in Fig. 1. It consists of two interleaved phases, each consisting of a flyback converter in series with a buck converter. The energy storage capacitor in this system is chosen to have the smallest capacity possible, and a large $120Hz$ voltage ripple will appear across this capacitor. The flyback topology was chosen as the power factor pre-regulator as it has been shown to be very good in PFC applications [6], [7], [8]. It is able to achieve near unity power factor as well as direct power transfer to the load. Furthermore, in comparison to the boost topology, the flyback converter electrically isolates the input and output.

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By significantly reducing the size of the energy storage capacitor, the converter will be lower cost and physically smaller, two characteristics that make this converter ideal for applications in portable consumer electronics and aviation. A smaller energy storage capacitor also permits the system designer to choose more reliable film or ceramic capacitors. These capacitors have a larger life span than electrolytic capacitors, and makes them ideal in solar photovoltaic applications, where products are sold with 20 to 25 year warranties [9], [10].

II. Proposed System

A. Energy Storage in PFCs

One of the largest problems PFC converters face when interfacing with a dc load or sink, is dealing with the second harmonic power ripple. The problem may be understood by studying the power entering a PFC rectifier, as shown in Equation (1) below. For a PFC inverter, the same logic can apply with the opposite direction of power flow.

$$P_{ac}(t) = V_g \cos(\omega t)\, I_g \cos(\omega t) = \frac{V_g I_g}{2}\left(1 + \cos(2\omega t)\right) \tag{1}$$

From this equation it is clear that the input power into a PFC supply contains a second harmonic ripple component. The output dc power is defined by the average value of Equation (1) over a period, $(V_g I_g)/2$. During times when the input power is less than the output power, the PFC must have sufficient energy storage to supply the dc load. Conventionally, this energy is supplied with a large capacitor, and in the case of a boost converter acting as a PFC operating in continuous conduction mode (CCM), a large high voltage capacitor. A capacitor of this type is very large, bulky and expensive. Moreover, its energy storage capabilities are under utilized. In the proposed solution the capacitor will be reduced in size so as to maximize the use of its energy storage capabilities. As a consequence, there will be a large ripple voltage on the main energy storage capacitor of the system at twice the frequency of the line voltage and this will introduce control challenges that have not previously been addressed.

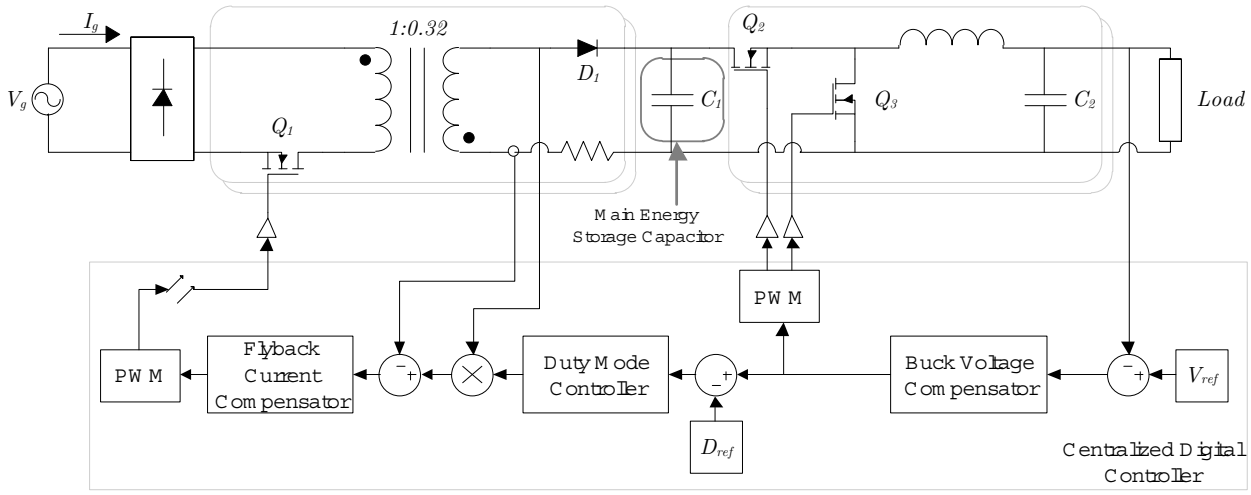


Fig. 1: Topology of the proposed system, including a block diagram of the duty mode controller.

B. New PFC Design

The topology of the proposed system was chosen such that a few basic criteria could be met:

- Galvanic isolation
- Universal input voltage (85 - $265V_{rms}$ at $50 - 60Hz$)
- Convenient output voltage for household electronics ($12V$)

In addition, the topology was chosen such that other criteria could be met, which would also reduce the cost and size of the converter:

- A small, low voltage energy storage capacitor
- A single, centralized controller
- Reduced voltages in the converter

Taking these points into account, a conventional topology of a series connection of a flyback and buck converter was chosen as shown in Fig. 1.

Both converters operate in CCM to reduce peak currents in the system [5]. To decrease the switching harmonics, an interleaved, two phase PFC stage was implemented [11], [12].

The turns ratio on the flyback transformer was chosen to provide a step down in voltage. This allows the main energy storage capacitor of the system, C_1 in Fig. 1, to be an inexpensive, low voltage component. The turns ratio chosen for the system was $1 : 0.32$.

Isolation is maintained through the use of a single optical coupler to send a gating pulse to the main switch, Q_1.

Finally, a significant innovation in the proposed converter is the location of input current and voltage sensors. Both sensors are placed on the secondary side of the transformer, allowing all sensing and control to be done on this side. Voltage sensing is accomplished when the main switch Q_1 is in the on state. During this time, the voltage across the primary side of the transformer is reflected to the secondary side and thus can be read by a sensor. Current sensing is accomplished when the main switch turns off, forcing the magnetizing current of the flyback transformer to flow through the secondary side, and then through a sensing resistor. In this way the controller can be combined into a single chip, as shown in Fig. 1 as the "Centralized Digital Controller".

C. Duty Mode Control

Combining both controllers for the PFC stage and the downstream converter on a single chip allows an advanced control technique to be developed, which will be referred to as duty mode control (DMC). Similar to how voltage and current mode control regulate voltage and current, DMC regulates a duty cycle to a desired value. Using DMC, the voltage on the main storage capacitor will be controlled such that the duty cycle of the downstream converter is held at a reference value. A simplified block diagram of the controller is shown in Fig. 1.

D. Centralized Control

The proposed centralized control method allows the entire controller to be implemented on a single field programmable gate array (FPGA). Digital control permits the use of control techniques that would be difficult or impossible to implement with standard analog control. These include DMC and a self adjusting dead zone controller as described in [13].

III. Main Energy Storage Capacitor Design

The proposed converter design will place slightly more stress onto the main energy storage capacitor of the system. The increased stress will manifest itself through a combination of an increased ripple current on the capacitor, and an increased peak voltage on the capacitor. This section will derive two equations that will help the designer manage these stress factors.

Fig. 2 shows the ripple current in the capacitor. The shaded region is the amount of charge, ΔQ, that is deposited onto the capacitor when the current is positive. This charge is added to the charge residing on the capacitor when it is at its lowest voltage, V_{MIN}. Therefore the maximum voltage on the capacitor is given by Equation (2):

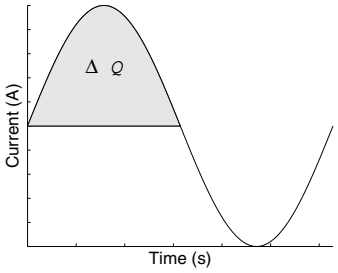


Fig. 2: The ripple current in the capacitor. The shaded region represents the charge deposited on the capacitor after $t = 0$.

$$V_{MAX} = \frac{Q_{MIN} + \Delta Q}{C} \tag{2}$$

where Q_{MIN} is the charge on the capacitor initially at $t = 0$ and C is the capacitance. Defining $\Delta V_r = V_{MAX} - V_{MIN}$ we find that:

$$\Delta V_r = \frac{\Delta Q}{C}. \tag{3}$$

Assuming that the current in the capacitor is sinusoidal with a peak value of $\sqrt{2}I_r$, the capacitor current can be easily integrated over one half cycle to obtain ΔQ:

$$\Delta Q = \frac{\sqrt{2}I_r}{\pi f_r}, \tag{4}$$

where f_r is the frequency of the second harmonic of the system. Substituting Equation (4) into Equation (3) the peak to peak ripple voltage on the capacitor is obtained in Equation (5).

$$\Delta V_r = \frac{\sqrt{2}I_r}{\pi f_r C} \tag{5}$$

Next, in an ideal PFC circuit, the current and voltage waveforms are sinusoidal and in phase with each other. Therefore, we can obtain an expression for the instantaneous input power:

$$P_{in}(t) = V_g \cos(\omega t)\, I_g \cos(\omega t) = \frac{V_g I_g}{2}\left(1 + \cos(2\omega t)\right) \tag{6}$$

where ω is the line frequency.

Equation (6) can be separated into a dc and ac component yielding:

$$P_{in}(t) = P_{dc} + P_{ac}(t) \tag{7}$$

where,

$$P_{dc} = \frac{V_g I_g}{2} \tag{8}$$

and

$$P_{ac}(t) = \frac{V_g I_g}{2}\cos(2\omega t) = P_{dc}\cos(2\omega t). \tag{9}$$

Assuming that the ac component of the input power is absorbed completely by the energy storage capacitor, we can determine the ripple on the capacitor that will result in this oscillating power. This assumption is valid as long as the magnetizing inductance and current are small enough such that $0.5 L_m I_m^2 << 0.5 C_1 V_C^2$.

The shaded region in Fig. 3 represents the energy absorbed by the capacitor for one half cycle. This absorption of energy will increase the capacitor voltage according to Equation (10). Let this energy be called ΔE.

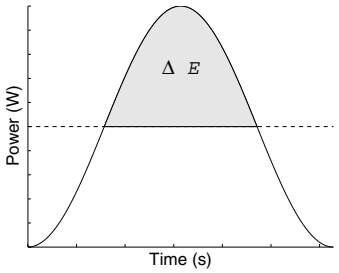


Fig. 3: The ac power absorbed by the storage capacitor. The shaded region represents the energy absorbed by the capacitor during one half cycle.

$$\Delta E = \frac{1}{2} C \left(V_f^2 - V_i^2\right) \tag{10}$$

where V_f, V_i and C are the final capacitor voltage, initial capacitor voltage and the capacitance, respectively.

Integrating the ac power over a half cycle to obtain ΔE yields:

$$\Delta E = \frac{P_{dc}}{\omega}. \tag{11}$$

Now substitute Equation (11) into Equation (10) and let $V_i = V_{MAX} - \Delta V_r$ and $V_f = V_{MAX}$:

$$P_{dc} = \frac{1}{2} C \omega \left(2 V_{MAX} \Delta V_r - \Delta V_r^2\right). \tag{12}$$

Finally substituting Equation (5) into Equation (12) for ΔV_r yields the final result:

$$P_{dc} = \sqrt{2} V_{MAX} I_r - \frac{I_r^2}{\pi f_r C}. \tag{13}$$

Equation (13) is the first design equation for the proposed converter. It is an expression for the maximum dc power one can draw from an ac source at unity power factor while effectively filtering out the ac ripple power and using a capacitor to its designed limits. This equation is useful when using electrolytic capacitor technology, which will be predominantly limited by its ripple current rating.

The second design equation comes from solving Equation 4 for I_r, substituting the result into Equation 13 and solving for the capacitance, C:

$$C = \frac{P_{dc}}{V_{MAX} \Delta V_r \pi f_r - \left(\Delta V_r\right)^2 \pi f r / 2} \tag{14}$$

Equation 14 is an equation for the minimum capacitance value required to effectively filter out the ac power from a unity power factor pre-regulator. This Equation is useful when designing converters that will use thin film technology, where the size of the capacitor will be the limiting design criteria.

IV. Analysis of DMC

A. Advantages

DMC control is advantageous in two major ways. Firstly, since the duty cycle of the downstream converter is being controlled instead of the midpoint voltage between the two converters, a voltage sensor is not required. This will reduce the cost and footprint of the converter.

Secondly, DMC control allows for smaller energy storage elements to be used. This is shown with control theory in the latter part of this section. However, to motivate this discussion consider a load step in a system with two converters connected in series. Conventionally, the sequence of events during a load step increase would be the following:

1) Load step increase occurs.
2) Voltage on output capacitor drops.
3) Voltage controller of downstream converter compensates by increasing its duty cycle.
4) Current into the downstream converter increases.
5) Midpoint voltage between converters drops.
6) Voltage controller of upstream converter compensates by increasing the duty cycle.

With DMC a similar load step yields the following order of events:

1) Load step increase occurs.
2) Voltage on output capacitor drops.
3) Voltage controller of downstream converter compensates by increasing the duty cycle.
6) Voltage controller of upstream converter compensates by increasing the duty cycle.

Therefore, the dynamics of the upstream converter (events 4 and 5) are bypassed. This can be used to help reduce the size of the bulky energy storage capacitor in between the two converters. This is also advantageous because the upstream converter will generally have a slower response than the downstream converter.

B. Theory

The theory of DMC will be demonstrated with a two converter example, as shown in Fig. 4. In the figure, two cascaded buck converters are shown. Generalized transfer functions from the output current of the system, $i^B(s)$, to the duty cycle of the upstream converter, $d^A(s)$, will be derived.

For a conventional cascaded system where both converters are operating with voltage mode control, the duty cycle of the downstream converter is the output of its controller. This is expressed in Equation 15:

$$d^B(s) = T^B(s)\, v^B(s) \tag{15}$$

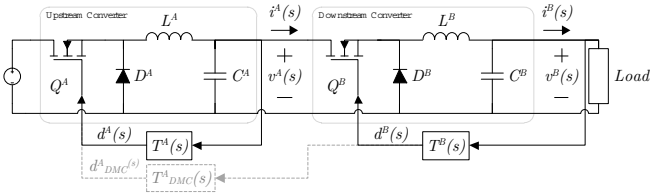


Fig. 4: Simplified block diagram of a two stage converter using conventional voltage control loops (solid black line), and a DMC control loop (dashed grey line).

Using the small signal approximation, the input current into a buck converter is proportional to the dc current in through the converter:

$$i^A(s) = I^B d^B(s) \tag{16}$$

Substitute Equation15 into Equation 16:

$$i^A(s) = I^B T^B(s)\, v^B(s) \tag{17}$$

The input voltage to the downstream converter is related to its current through the energy storage capacitor, C^A. Thus, $v^A(s)$ can be determined by substituting Equation 17 into the ideal capacitor equation to yield:

$$v^A(s) = \frac{I^B T^B(s)\, v^B(s)}{sC^A} \tag{18}$$

Finally, the duty cycle of the upstream converter is determined by multiplying its output voltage by its controller:

$$d^A(s) = \frac{I^B T^A(s)\, T^B(s)\, v^B(s)}{sC^A} \tag{19}$$

A similar equation representing DMC control can be derived by simply multiplying the duty cycle of Equation 15 by the DMC controller:

$$d^A_{DMC}(s) = T^A_{DMC}(s)\, T^B(s)\, v^B(s) \tag{20}$$

Comparing Equations 19 and 20, it is evident that any change in the output voltage is more directly communicated to the upstream converter. This allows any energy storage devices in between the two converters to be reduced since the amount of energy required to make up for any system latencies is reduced.

V. Converter Design

The important aspects of the proposed converter design will be discussed in this section. In particular, the components selected for the flyback pre-regulator will be discussed, including the selection of an appropriate energy storage capacitor for the system.

A. Flyback transformer

The flyback transformer was chosen in order to meet the following criteria:

- The primary coil can be excited with a rectified, universal ac input voltage of $85 - 265V_{RMS}$.
- The turns ratio of no more than $1 : 0.5$ to step down the voltage.
- A power rating of at least $40W$.
- Readily available for purchase.

Using this criteria, the flyback transformer chosen was model number Z9260-AL manufactured by Coilcraft®.

B. Main energy storage capacitor

The main energy storage capacitor is also the output capacitor of the flyback converter. Electrolytic technology was chosen for this capacitor to reduce the cost of the converter. Since this capacitor has a large ripple voltage on it, it must be designed in accordance with Equation (13). The technical specifications of this capacitor for one phase of the converter are shown in Table I.

TABLE I: Technical specifications for the main energy storage capacitor.

Parameter	Value	Units
P_{out}	20	W
η_{Buck}	80	%
$V_{nominal}$	50	V
ΔV_{MAX}	15	V

Using these specifications, an electrolytic $100\mu F$ capacitor manufactured by Panasonic® was chosen, model number: EEUFC1J101L. Its specifications are shown in Table II, and they can be substituted into Equation (13). The result of the power it can provide is shown in Equation (21), and is well within the design criteria of Table I with a factor of safety of 1.45.

TABLE II: Technical specifications of the main energy storage capacitor chosen, Panasonic® EEUFC1J101.

Parameter	Value	Units
I_{ripple} at $120Hz$	823	mA
V_{MAX}	63	V
R_{ESR}	0.230	Ω

$$P_{dc} = \sqrt{2}V_{MAX}I_{ripple} - \frac{I_{ripple}^2}{\pi f_{ripple} C} = 55.36W \qquad (21)$$

The capacitor chosen is low cost and readily available. Furthermore, it can handle a relatively large ripple current, which is ideal for the proposed application.

VI. Converter specifications

The converter designed in the laboratory has the performance specifications shown in Table III. Technical specifications are shown in Table IV.

TABLE III: Performance specifications of the converter designed in the laboratory.

Input Voltage	$85 - 265V_{RMS}$, $50 - 60Hz$
Output Voltage	$12Vdc \pm 0.7V$
Max. Output Power	$40W$
Power Factor	≥ 0.98 for loads $\geq 20W$
Interleaved Phases	2

TABLE IV: Technical specifications of each phase of the converter designed in the laboratory. Note that capacitor C^A is the main energy storage component of the system.

Flyback Converter		
Parameter	Value	Units
L^A	0.7	mH
C^A	100	μF
$V^A_{nominal}$	50	V
f_{sw}	400	kHz
Buck Converter		
Parameter	Value	Units
L^B	4.7	μH
C^B	47	μF
f_{sw}	800	kHz

VII. Steady state operation

Fig. 5 shows the input voltage and current under full load conditions ($40W$). The input voltage in this case was set to $110V_{RMS}$ at $60Hz$. As shown, the converter is operating with excellent power factor correction and in this particular case, the power factor is 0.99. The total harmonic distortion is 7.4% .

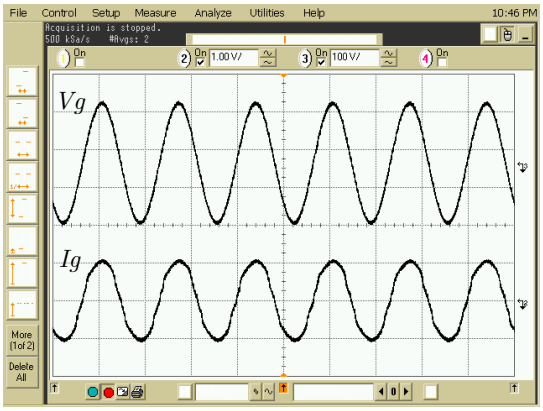


Fig. 5: The input voltage and current of the converter under full load. $V_g = 110V_{RMS}, 60Hz$. From top to bottom: Vg line voltage on CH3 at $100V/Div$ and Ig line current on CH2 at $1A/Div$. Time scale: $10ms/Div$

Fig. 6 shows the voltage on the main energy storage capacitor, the output voltage and the duty cycle of the flyback converter for the same load and input voltage conditions as in Fig. 5. In this figure, the large ripple voltage on the capacitor

is clearly visible at twice the line frequency. It has a peak to peak voltage of $13.98V$, or 31.4% of its nominal value. Table V shows the percentage ripple voltage that is obtained at half and full loads for input line frequencies of $50Hz$ and $60Hz$. The output voltage also exhibits some ripple, due to the well known problem of a limited resolution of the DPWM for the buck converter. There are many solutions to this problem, for example, a sigma delta DPWM as shown in [14], however this is not a focus of this work.

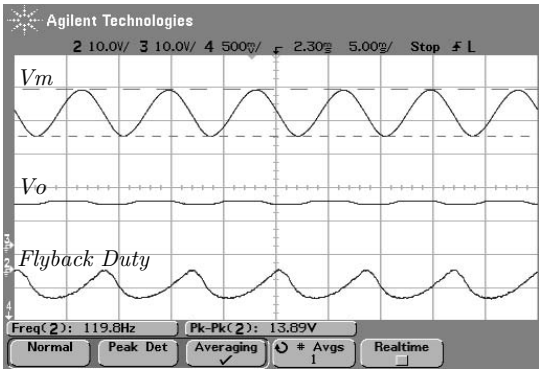


Fig. 6: From top to bottom: Vm the voltage on the energy storage capacitor on CH2 at $10V/Div$, Vo the output voltage on CH3 at $10V/Div$ and the duty cycle of the flyback converter on CH4 at $500mV/Div$. Time scale: $5ms/Div$

TABLE V: The percentage voltage ripple on the main energy storage capacitor at different loads and line frequencies.

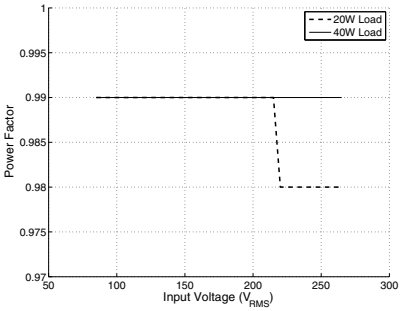
	$50Hz$	$60Hz$
$20W$	23.19%	19.23%
$40W$	37.06%	31.44%

VIII. Power factor and THD

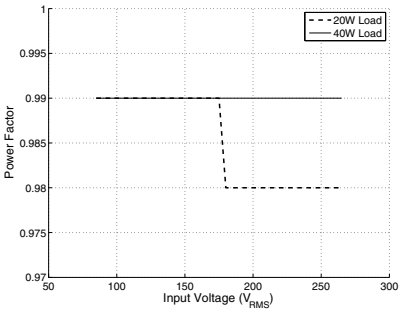
This section summarizes the performance of the converter as a power factor regulator and evaluates it on two criteria: the power factor as measured by the power supply used and the total harmonic distortion as calculated from the input current measured by the oscilloscope.

Fig. 7(a) and 7(b) show the measured power factor. As shown, the converter maintains a power factor of 0.98 or more for all input voltages under full and half load. The power factor decreases at high voltages due to the limitations on measuring small currents which will be discussed in Section XI.

In the laboratory, the THD was calculated over the entire input voltage range for both $50Hz$ and $60Hz$ line frequencies. Using this data, the worst case THD was analysed in depth and is shown in Fig. 8. This Figure shows the worst case odd harmonic content over all loads, input frequencies and voltages plotted against the harmonic current emission limits provided by the IEC61000-3-2 standard. As shown, the experimental converter system in the laboratory emitted at most half the harmonic current limit as provided by this standard, this minimum occurring at the 9th harmonic current. This also shows that a low cost, PFC supply can be built with sensing on the secondary side that exceeds any input harmonic current standards currently enforced.



(a) $f_{line} = 50Hz$



(b) $f_{line} = 60Hz$

Fig. 7: The measured power factor of the experimental converter system.

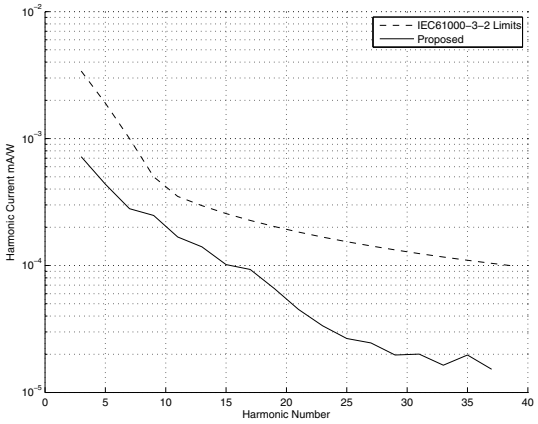
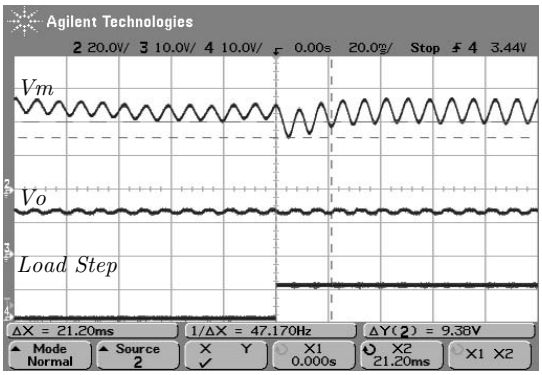


Fig. 8: Harmonic current emissions from the converter built in the laboratory plotted against the maximum allowable harmonic current emission as stated in the IEC61000-3-2 standard [1].

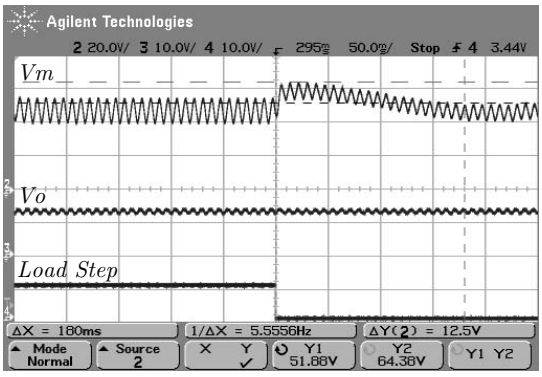
IX. Transient response

The transient response of the converter was tested with an input voltage of $110V_{RMS}$ at $60Hz$ under a 50% load step from $20W$ to $40W$. Fig. 9(a) and 9(b) show the results. The downstream buck converter uses voltage mode control, and the

upstream flyback pre-regulator uses DMC with a self tuning dead zone controller [13].



(a) load increase



(b) load decrease

Fig. 9: The transient response of the experimental converter system in the laboratory under a 50% load transient. From top to bottom: Vm the voltage on the main energy storage capacitor on CH2 at $20V/Div$, Vo the output voltage on CH3 at $10V/Div$ and the load step signal on CH4 at $20V/Div$. Time scale: $20ms/Div$

From the figures it is evident that despite the large ripple voltage on the main energy storage capacitor and the little amount of energy stored on it, digital control enabled the development of a suitable controller that can successfully maintain the mid-point voltage of the converter through large load transients.

X. Energy storage comparison

One of the main features of the proposed system is its reduced energy storage. Table X compares the proposed system to three other PFC supplies supplied by three different manufacturers.

TABLE VI: The energy storage elements of the proposed converter in comparison with other PFC power supplies.

Topology	Energy Storage (mJ/W)
Proposed	12
Boost [15]	238
Boost [16]	165
Interleaved Boost [17]	101

As shown, the proposed solution has a significant reduction in energy storage from the conventional solutions, up to *19 times less energy storage capacity*. Since energy storage elements can be large and expensive, both of these factors are reduced in a converter using the proposed design. This is a substantial improvement over other topologies and this proposed system has opened new opportunities in PFC design.

XI. Limitations of the proposed system

A. Current measurement

As mentioned earlier in this chapter, the power factor of the converter decreases at high voltages, when the current is decreased. The main source of harmonic distortion occurs near the zero crossings of the input voltage when the duty cycle is large. This problem can be attributed to the current sensing circuit. Fig. 10 shows the waveform that goes into the current sensing ADC. When the main switch of the flyback converter is switched off, current begins to flow in the secondary winding of the flyback transformer and a voltage is sensed on the current sensing resistor. Due to a small capacitance at this node created by an anti-parallel voltage protection diode, the sensed voltage exhibits an exponential waveform as seen in Fig. 10. Therefore at large duty cycles, the current measurement is not consistent with the actual input current into the converter, and the actual current is much larger than the measured input current. To overcome this limitation, the duty cycle is digitally limited at higher voltages. If it is not, the input current exhibits spikes near the zero crossings of the voltage waveform.

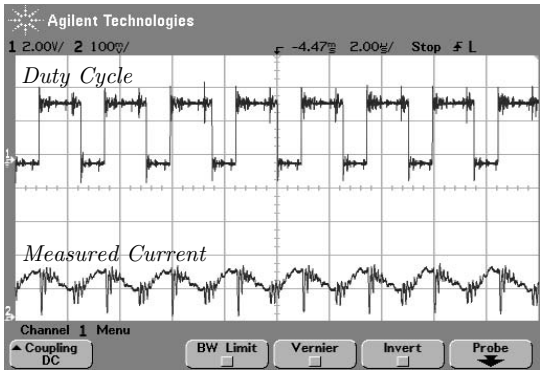


Fig. 10: Current sensing waveform. From top to bottom: the duty cycle of the flyback converter on CH1 at $2V/Div$ and the input to the current sensing ADC on CH2 at $100mV/Div$. Time scale: $2\mu s/Div$

B. Loss in main energy storage capacitor

A trade off of the proposed converter is energy storage for a large ripple voltage on the main energy storage capacitor of the system. As a consequence, the ripple current in this capacitor will generate some losses proportional to the ESR of the capacitor. The current in the main energy storage capacitor

assuming ideal components can be derived, and is shown in Equation (22).

$$i_c(t) = -P_{dc}\frac{\cos(2\omega t)}{\sqrt{\frac{P_{dc}\sin(2\omega t)}{\omega C} + V_0^2}} \tag{22}$$

Using this equation the power lost in the energy storage capacitor, P_C, is determined by Equation (23).

$$P_C = \frac{\omega}{2\pi}\int_0^{(2\pi/\omega)} i_c^2(t)\, R_{ESR}\, dt \tag{23}$$

Therefore in the worst case scenario where the average efficiency of the buck converter is 70%, the power lost in the main energy storage capacitor can be calculated to be $76.9mW$.

This analysis shows that even with a larger ripple current on the main energy storage capacitor, the losses due to this current are very small compared with the output power of the converter. Furthermore, since typical manufactured capacitors exhibit a direct relationship between energy storage and ESR, as the energy storage decreases, the ESR also decreases. Thus, a potentially smaller capacitor could be used.

C. Hold up time

Hold up time, also known as ride through time, is a converter's ability to provide a continuous output voltage in the event of a temporary fault in the ac voltage. For manufacturers of dc power rectifiers for information technology (IT) applications, there is a standard created by the Information Technology Industry Council (ITIC) which they should adhere to if the voltage sags, swells or is interrupted for a certain period of time. The ITIC recommends that a power supply have a hold up time of at least $20ms$, or one line cycle at $50Hz$ [18]. For the proposed system, the hold up time in the worst case is about $4ms$. However this does not mean the proposed system is not a viable solution. The proposed solution can be implemented for devices that do not require such a stringent hold up time, such as battery powered devices. Furthermore, for inverting applications, the CBEMA curve does not apply.

XII. Conclusion

This work proposes a solution to minimize the energy storage components of PFC rectifiers and inverters by allowing a large ripple voltage on the main energy storage capacitor and a unified digital controller to create a small portable converter.

The effectiveness of the proposed solution was shown through a prototype developed in the laboratory and the resulting converter maintained a power factor greater than 0.98 for all loading and input voltage conditions. Furthermore, all the sensing and control for the entire converter was implemented on the isolated side of the system. The controller was implemented digitally with a single FPGA. The total energy storage in the PFC stage of the converter was shown to be up to 19 times less than conventional solutions.

A new control method for controlling cascaded converters, DMC, was also proposed and implemented in an experimental converter system. This new control method was briefly studied in this work and through that analysis it was shown that DMC control can allow designers to use smaller energy storage elements in between cascaded SMPS. Furthermore, applications of DMC are not limited to PFC rectifiers and inverters, DMC can be applied to any cascaded connection of SMPS to decrease the energy storage components of that system.

A. Future work

There are many other cascaded configurations which could benefit from DMC. As mentioned, the PFC inverter is another typical application which is similar to the PFC rectifier designed and discussed in this work. The group hopes to pursue a single phase inverter which uses DMC in its controller.

Further work with the theory of DMC would also include a more rigorous analysis of how the controller of the downstream converter effects the performance of a DMC controller. In addition, how would multiple downstream converters of varying output powers be integrated into a single DMC controller.

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