

LOW-VOLUME PFC RECTIFIER BASED ON NON-SYMMETRIC MULTI-LEVEL BOOST CONVERTER

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Abstract— This paper introduces a universal-input digitally-controlled single-phase rectifier with power factor correction (PFC) based on a modified multi level boost converter topology. In comparison with the conventional boost-based systems and other multi-level solutions the new PFC rectifier has significantly smaller inductor and lower switching losses. The improvements are achieved by replacing the output capacitor of the boost converter with a non-symmetric active capacitive divider and by utilizing downstream converter stage for the divider charge balancing.

Experimental results obtained from a 400W, 200KHz, universal input voltage (90V-260V) to 400V PFC prototype demonstrate three times smaller inductor current ripple, allowing for the same inductor reduction, and up to 50% reduction in power losses, resulting in 6% efficiency improvement compared to a conventional boost PFC.

I. INTRODUCTION

The boost converter operating in continuous current mode (CCM) is among most widely used converter topologies in power factor correction (PFC) rectifiers, due to its continuous input current, low electromagnetic interference (EMI), and fairly simple control requirements [1-4].

One of the major drawbacks of the boost-based PFC is a relatively large size of its inductor preventing its use in weight and volume sensitive applications. The large boost inductor also causes non-negligible core losses [4]-[5] and results in a relatively large parasitic capacitance of the winding. This capacitance allows high frequency current to flow through the line EMI filter, increasing its size [6]. Another problem of the conventional boost-based topologies is switching losses [1],[7], causing heat dissipation problems whose handling often requires bulky cooling components.

To minimize the size of the boost-based PFC system inductors a number of methods have been proposed in the past [4-11]. Those can generally be divided in frequency-increase based and topological changes. Interleaved topologies for minimizing the total inductance volume by effectively increasing the switching frequency have been demonstrated as

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very effective solutions [8-10] for larger power ratings where the semiconductor switching components can be fully utilized.

In addition to reducing the inductor size without paralleling converter stages, topological methods [5,6] also result in minimization of the switching losses. Flying capacitor multi-cell boost, derived from multilevel converters, [6] reduces the inductor, switching losses, and voltage stress across switches. The advantages are achieved at the cost of using a relatively large extra flying capacitor. A three-level boost-based PFC introduced in [5] replaces the output capacitor of the boost converter with a compact active capacitive divider and, for the same switching frequency, results in a 50% reduction of the inductor value compared to conventional solutions.

The main goal of this paper is to introduce a novel multi-level boost based PFC rectifier of Fig.1 that allows further reduction of the inductor volume while maintaining the benefits of the previously presented multi-level solutions.

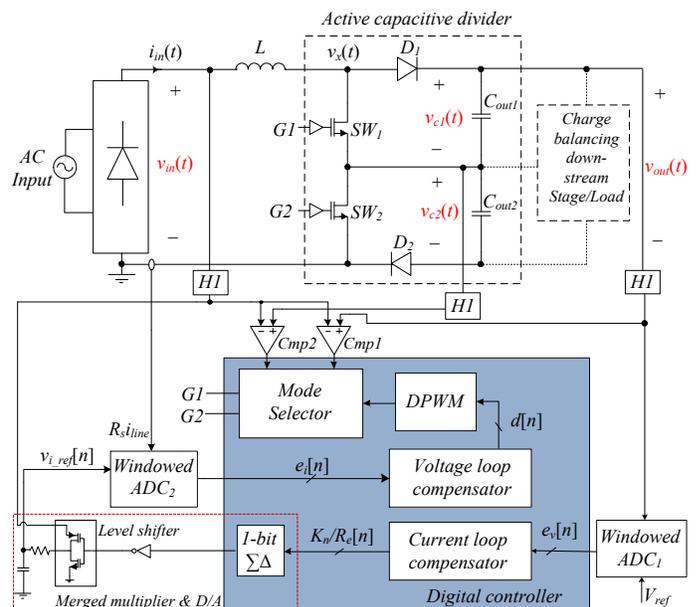


Fig. 1: Block diagram of the non-symmetric multi-level buck (NSMB) based PFC rectifier and its controller.

Compared to a four-level, flying capacitor multi-cell boost [6],[11], the introduced topology has the same inductor volume when operating at the same switching frequency. Still, the system shown here requires a smaller number of switching components and eliminates the flying capacitors. This converter reduces the size of the boost inductor to a one third of the value required for the conventional boost PFC and, for the rest of the power stage; its implementation requires the same number and volume of components as the previously presented three-level [5] solution. The inductor reduction is achieved by providing non-equal voltages across the capacitive divider cells and, in that way, effectively creating a structure that produces 4-output voltage levels without increasing the hardware complexity. The capacitive divider voltages are regulated with a downstream converter that, due to dual input operation, also has smaller volume than the conventional downstream solutions.

A digital average current programmed mode controller [12] regulates the operation of the PFC. In addition of regulating both the output voltage V_{out} and the input current shape the controller also governs the operation of the active capacitive divider.

II. PRINCIPLE OF OPERATION AND SYSTEM DESCRIPTION

To minimize the inductance volume, the introduced non-symmetric multi-level boost (NSMB) converter functions on the same principle as other multi-level solutions. It utilizes the fact that reducing the voltage variation across the boost inductor reduces the inductor size as well. To lower the variation, instead of changing the switching node ($v_x(t)$ of Fig.1) between 0 and full output voltage value, like in the conventional boost case, the voltage swing of $v_x(t)$ is varied depending on the instantaneous rectified input voltage value $v_{in}(t)$. The swing variation is performed through the active capacitive divider network, such that the condition for the proper boost operation, i.e. $v_{x_max} > v_{in}(t)$, is always satisfied, where v_{x_max} is the maximum value of the switching node voltage.

The relation between the inductor value L and its maximum voltage swing V_{swing} , which for the conventional buck is equal to the output voltage V_{out} , can be analyzed through the following equation for the maximum inductor current ripple [5]:

$$\Delta I_{ripple\max} = \frac{V_{swing}}{4L} \cdot \frac{1}{f_{sw}}, \quad (1)$$

which occurs for $D = 0.5$, where D is the duty ratio and f_{sw} is the switching frequency of the converter. It can be seen that the maximum ripple, which determines the inductor size, is linearly proportional to V_{swing} , and that by minimizing this value the inductor can be reduced as well, while maintaining the same current ripple.

To minimize the inductor, in the converter of Fig.1, an active capacitive divider replaces the output capacitor of the conventional boost. The divider limits the maximum inductor voltage swing value to $V_{out}/3$ while maintaining the maximum value of the switching node voltage larger than $v_{in}(t)$ at all

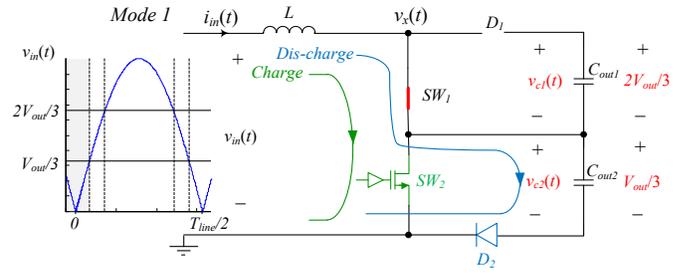


Fig.2: Operation of the NSMB converter for $v_{in}(t) < V_{out}/3$ (mode 1).

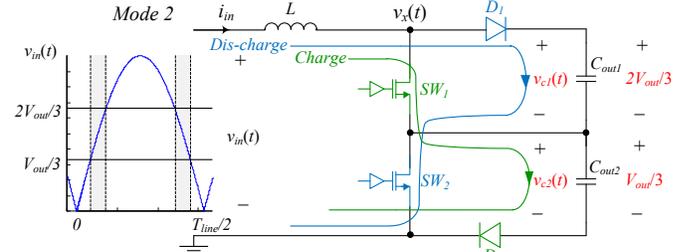


Fig.3: Operation of the NSMB converter for $V_{out}/3 < v_{in}(t) < 2V_{out}/3$ (mode 2).

times. This reduction in the swing value resulting in the proportional minimization of the boost inductor is achieved by setting the divider capacitor voltages to be approximately $2V_{out}/3$ and $V_{out}/3$ and by modifying the switching sequence of transistors SW_1 and SW_2 in accordance with the change of $v_{in}(t)$.

A. Non-symmetric capacitive divider

The operation of this non-symmetric capacitive divider can be explained by looking at the rectified line input voltage waveform and diagrams of Figs. 2 to 4. The divider has three distinctive modes of work depending on the instantaneous input voltage value.

For $v_{in}(t) < V_{out}/3$ the converter operates in *mode 1*. In this mode the switch 1 of Fig.1 is kept on, reverse biasing the diode D_1 and the switching sequence is performed with the SW_2 and the diode D_2 . The digital compensator of Fig.1 provides the duty ratio control signal for SW_2 . The conducting paths for the both portions of a switching period $T_s = 1/f_{sw}$ are shown in Fig.2, where the green line corresponds to the inductor charging process and the blue line to discharging. It can be seen that, in this mode, the maximum voltage swing across the inductor is $V_{out}/3$, existing when the input voltage is zero. This mode of operation is maintained as long as the input voltage is lower than $v_{c2}(t) \approx V_{out}/3$ and the condition for the regular boost operation satisfied.

Mode 2 of operation, shown in Fig.3, is used when $V_{out}/3 < v_{in}(t) < 2V_{out}/3$. In this mode during the first portion of a switching period, corresponding to the on transistor state in the conventional topology, the transistor SW_1 and diode D_2 are turned on. During the remaining portion of the period the transistor SW_2 and diode D_1 are conducting. It can be seen that, in this way, the inductor voltage swing is limited and its value does not exceed $V_{out}/3$. During the first portion of the switching interval its value is $v_{in}(t) - V_{out}/3$ and during the remaining time it becomes $v_{in}(t) - 2V_{out}/3$.

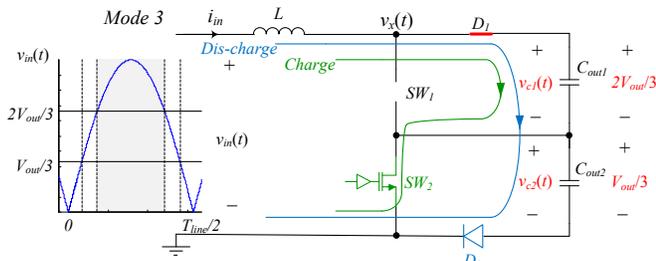


Fig.4: Operation of the NSMB converter for $v_{in}(t) > 2V_{out}/3$ (mode 3).

Mode 3, shown in Fig.4, is activated when $v_{in}(t)$ exceeds $2V_{out}/3$. Throughout this mode the transistor SW_1 is kept off allowing diode D_1 to conduct. Now, during the first portion of the switching interval the transistor SW_2 is conducting and the voltage across the inductor is $v_{in}(t) - 2V_{out}/3$. During the second portion of the interval the diode D_2 conducts and the inductor voltage is $v_{in}(t) - V_{out}$. Again, it can be seen that the inductor voltage swing is no larger than $V_{out}/3$.

Besides voltage swing minimization allowing for the reduction of the filter inductor to 1/3 of its conventional value, the NSMB also has lower switching losses, which are a main contributor to the overall losses in the conventional boost PFC topologies [7]. By looking at the previously described switching sequences, it can be noticed that the loss reduction is achieved because of a lower voltage stress. Instead of switching the full output voltage, SW_1 and D_1 are operating with a 2/3 of that value and the switches SW_2 and D_2 are interrupting even lower values not larger than $V_{out}/3$. A detailed loss analysis, given in Section III of this paper, shows that the switching and overall losses of the NSMB converter are smaller than those of the conventional boost PFC.

B. Digital Controller

The digital controller of Fig.1 is a modified version of the average current programmed mode architecture presented in [13]. In addition to regulating the input current waveform and the output voltage, it also produces switching sequences for the active capacitive divider, as described in the previous subsection.

Based on the digital equivalent of output voltage error value $e_v[n]$, produced by a windowed based ADC_1 [14], the voltage loop of the averaged current-programmed mode controller creates a reference $K[n]/R_e$ that is inversely proportional to the desired emulated resistance seen at the input of the PFC rectifier [15]. This value is then passed to the

1-bit sigma-delta modulator. This modulator, together with the inverter and the RC filter, creates a merged multiplier and digital-to-analog converter that produces analog reference $v_{i_ref}(t)$ for the current loop. This value is then compared to the sensed input current value $R_s i_{line}(t)$ and a digital equivalent of the current error signal $e_i[n]$ is created by the windowed ADC_2 . This error value is sent to the current loop compensator that produces value $d[n]$ that is the control signal for the digital pulse-width modulator (DPWM). This control value is also passed to the mode selector that, based on the state of the comparators monitoring the difference between the divider taps and the input voltage, creates a switching sequence as described in the previous subsection.

III. DOWNSTREAM CONVERTER AND CENTRE-TAP VOLTAGE REGULATION

The voltage divider at the output of the NSMB-based PFC stage allows for the use of dual-input [16], i.e. multi-level, downstream converter stages, which, in terms of the volume and power processing efficiency, are significantly better than the conventional single-input solutions [16-18]. The downstream converter is also used for centre-tap voltage regulation that, in this case, cannot be achieved applying techniques for the conventional multi-level solutions [5,11] that have equal voltages across divider capacitors.

Figure 5 shows two of many different possibilities for isolated multi-level downstream converter implementation, namely a modified flyback and forward converters. In both of these, the volume and efficiency savings are obtained on the principle of inductor voltage swing reduction reviewed in the previous section [16].

A. Centre-Tap Voltage Control

The NSMB converter requires the mid-point voltage to be regulated at $V_{out}/3$ at all times. This hinders the use of a centre tap regulation method similar to the one applied for the conventional 3-level boost PFC [5]. There, the voltages across both divider capacitors are $V_{out}/2$ and the regulation is performed through a simple alternation of capacitors charging/discharging sequence.

In this case, the downstream converter, inevitably existing in practically all systems of interest, is used for the balancing. The regulation is performed utilizing the principle presented in [16]. There, the input currents of the downstream inductive stage regulate the centre-tap of a capacitive divider in a merged switch-capacitor and buck converter stage. Here, the output currents of the divider tap voltages are regulated with

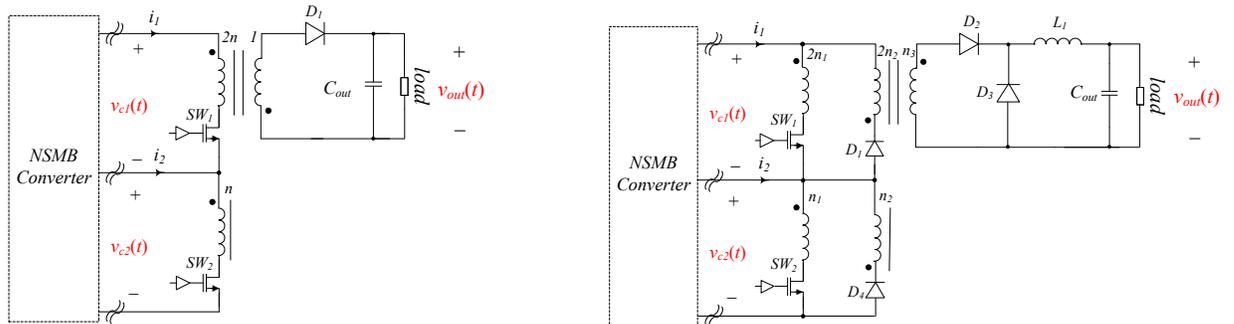


Fig.5: Dual-input flyback and forward downstream isolated converter topologies.

Table I. Comparison of switching and conduction losses of the proposed converter compared to the conventional boost

Mode	Mode '1'		Mode '2'		Mode '3'	
	Charge	Dis-Charge	Charge	Dis-Charge	Charge	Dis-Charge
Conduction path (NSMB)	$L/3, SW_1, SW_2$	$L/3, SW_1, D_2$	$L/3, SW_1, D_2$	$L/3, D_1, SW_2$	$L/3, D_1, SW_2$	$L/3, D_1, D_2$
Conduction path (Boost)	L, SW_1, SW_2	L, D_1, D_2	L, SW_1, SW_2	L, D_1, D_2	L, SW_1, SW_2	L, D_1, D_2
Switching components (NSMB)	SW_2, D_2		SW_1, SW_2, D_1, D_2		SW_2, D_2	
Switching components (Boost)	SW_1, SW_2, D_1, D_2		SW_1, SW_2, D_1, D_2		SW_1, SW_2, D_1, D_2	
Comparison of switching losses	NSMB losses ≈ 0.33 * Boost losses		Same		NSMB losses ≈ 0.33 * Boost losses	

the downstream stage in the similar manner.

B. Silicon area and the volume of passive components

The minimum silicon area required for the implementation of the NSMB can be found by looking at the voltage and current stress of the switching components. Compared to a conventional boost PFC, the silicon area required for the SW_1, SW_2, D_1 and D_2 is equal to the total area needed for the conventional. This is due to lower voltage ratings of the NSMB components (SW_1 and D_1 rated at $2V_{out}/3$ while SW_2, D_2 are rated at $V_{out}/3$). Assuming the output capacitor of the conventional boost PFC is C_{out} , rated at V_{out} , the NSMB converter rated for the same output power needs a $C_{out1} = 3C_{out}/2$, rated at $2V_{out}/3$ and $C_{out2} = 3C_{out}$, rated at $V_{out}/3$. Since the volume of a capacitor depends on its energy storage capacity [19], i.e. $W_e = \frac{1}{2}CV^2$, the total volume of the divider capacitors is no larger than that of the conventional boost converter. As a result, compared to a boost PFC, the NSMB converter reduces the inductance volume by 3 times without affecting the size of other power stage components.

C. Comparison of Losses

Table I compares the switching and conduction losses of a boost PFC with the NSMB converter during different operating modes. From the table it can be concluded that compared to a conventional boost converter, the switching losses of the NSMB converter over one line cycle are reduced mainly due to switching lower voltages across smaller switches.

By analyzing conduction losses over one cycle it can also be found that the portion of losses contributed by the switching components, i.e. switch 'on' state resistances and forward voltage drop of diodes, are equal for both converters. However, the equivalent series resistance of the inductor (DCR) in the NSMB converter is effectively reduced by three times as a result of utilizing smaller inductor, decreasing overall conduction losses. In Table I it has been assumed that the switch and diode of the conventional asynchronous boost converter are composed by a series combination of SW_1 and SW_2 and of D_1 and D_2 respectively.

IV. EXPERIMENTAL SYSTEM AND RESULTS

To validate the performance and functionality of the introduced NSMB-based PFC topology a universal-input 500 W, 200 kHz experimental prototype was built, based on the diagram of Fig.1. Also, its performances are compared to a conventional boost-based PFC solution having the same switching frequency and

output power rating. Power factor for both cases is measured to be over 0.98. The results of the experimental verifications are shown in Figs. 6 and 7.

Fig. 6 shows the key current and voltage waveforms for the both converters, where, in this case, for the demonstration purpose, the inductors of both stages are selected to be the same ($680\mu H$). It can be seen that, as expected, the NSMB has about three times smaller inductor voltage swing and the maximum current ripple as well. In other words, for the same

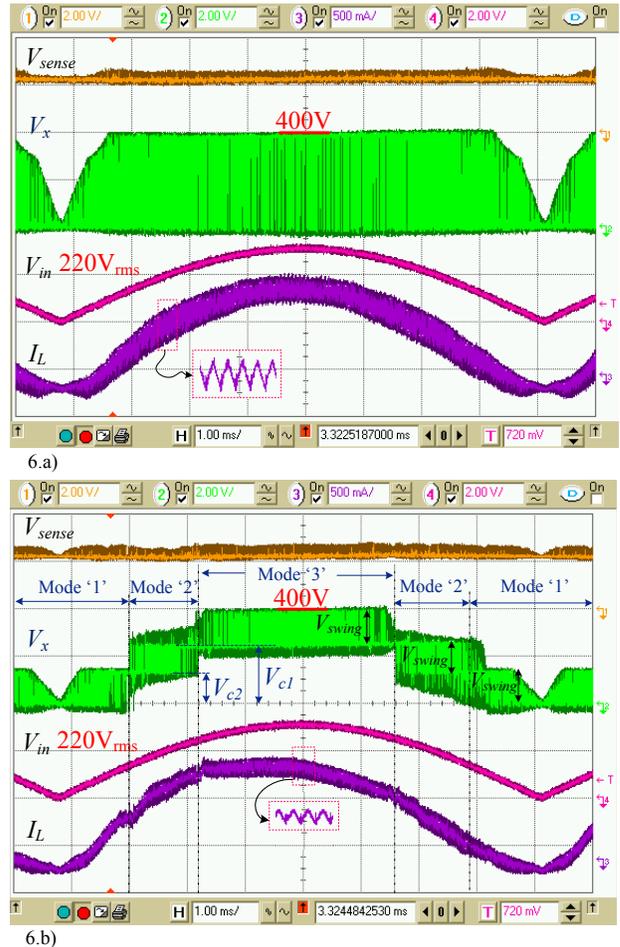


Fig.6. a)Steady-state operation of the NSMB converter. b) Steady-state operation of the conventional boost PFC. V_{sense} is the output voltage measurement signal (2V/div). Input voltage (V_{in}) and inductor switching node voltage (V_x) waveforms are 200V/div. I_L is the inductor current (500mA/div). The zoomed in version of inductor current (10 μ s/div) is also shown for portion of i_L with maximum

maximum current ripple the NSMB allows the use of a 3 times smaller inductor. Fig.7 shows efficiency comparison results for the both stages operating with 220Vrms input voltage. Also, for the efficiency comparison experiments the NSMB, has three times smaller inductor than boost, to achieve the same inductor current ripple. It can be seen that, because of the reduction of both switching and conduction losses, due to lower switching voltages and inductor dc winding resistance (DCR), the introduced NSMB-PFC has up to 6% improved efficiency over the conventional solutions.

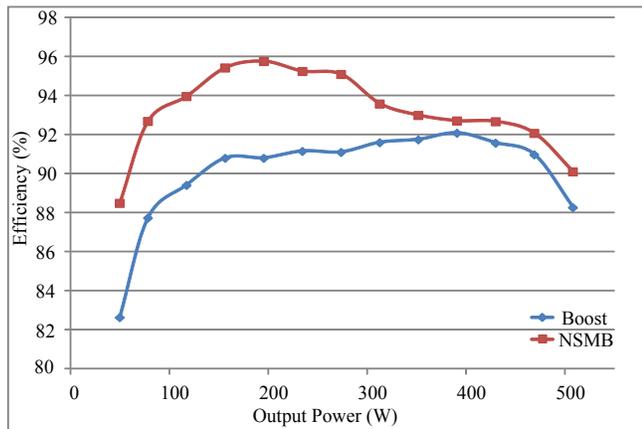


Fig. 7. Efficiency comparison of Boost and NSMB PFC converters

V. CONCLUSIONS

A PFC rectifier based on a novel digitally-controlled non-symmetric multi-level boost converter (NSMB) converter that requires three times smaller inductor and has lower losses than the conventional boost based solution is introduced. The NSMB is a modified version of the three-level boost topology. Instead of maintaining the same voltages across the output divider capacitors, in this system, they are regulated at 1/3 and 2/3 of the full output level. This modification allows for a further reduction of the inductor voltage swing and, consequently, its minimization. To regulate the centre-tap voltage, input current of a two-input low-volume downstream converter stage is utilized. Experimental comparisons with a conventional PFC verify advantages of the new system.

REFERENCES

- [1] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Power factor correction: A survey," in Proc. IEEE PESC'01, 2001, pp. 8–13.
- [2] Y. Jang, M.M. Jovanovic, "Interleaved Boost Converter With Intrinsic Voltage-Doubler Characteristic for Universal-Line PFC Front End," IEEE Transactions on Power Electronics, vol.22, no.4, pp.1394-1401, July 2007
- [3] J. Salmon, A. Knight, J. Ewanchuk, N. Noor, "Multi-level single phase boost rectifiers using coupled inductors," Power Electronics Specialists Conference, 2008. PESC 2008. IEEE , pp.3156-3163, 15-19 June 2008.
- [4] D. Maksimovic, R. Erickson, "Universal-input, high-power-factor, boost doubler rectifiers," Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual , pp.459-465 vol.1, 5-9 Mar 1995
- [5] M.T. Zhang, Y. Jiang, F.C. Lee, M.M Jovanovic, "Single-phase three-level boost power factor correction converter ," Applied Power

- Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual , pp.434-439 vol.1, 5-9 Mar 1995
- [6] F. Forest, T.A. Meynard, S. Faucher, F. Richardeau, J.J. Huselstein, C. Joubert, "Using the multilevel imbricated cells topologies in the design of low-power power-factor-corrector converters," IEEE Transactions on Industrial Electronics, vol.52, no.1, pp. 151- 161, Feb. 2005
- [7] D. Damasceno, L. Schuch, J.R. Pinheiro, "Design Procedure to Minimize Boost PFC Volume Concerning the Trade-offs Among Switching Frequency, Input Current Ripple and Soft-Switching," Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th , pp.2333-2338, 16-16 June 2005
- [8] L. Balogh, R. Redl, "Power-factor correction with interleaved boost converters in continuous-inductor-current mode," Applied Power Electronics Conference and Exposition, 1993. APEC '93. Conference Proceedings 1993., Eighth Annual , pp.168-174, 7-11 Mar 1993
- [9] P.W. Lee, Y.S. Lee, D.K.W. Cheng, and X.C. Liu, "Steady-State Analysis of an Interleaved Boost Converter with Coupled Inductors," IEEE Transactions on Industrial Electronics., vol. 47, no. 4, Aug. 2000, pp.787-795.
- [10] B.A. Miwa, D.M. Otten, M.E. Schlecht, "High efficiency power factor correction using interleaving techniques," Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual , pp.557-568, 23-27 Feb 1992
- [11] T.A. Meynard, H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE , pp.397-403 vol.1, 29 Jun-3 Jul 1992
- [12] A.H. Mitwalli, S.B. Leeb, G.C. Verghese, V.J. Thottuvelil, "An adaptive digital controller for a unity power factor converter ," IEEE Transactions on Power Electronics, vol.11, no.2, pp.374-382, Mar 1996
- [13] A. Prodic, "Digital Controller for High-Frequency Rectifiers with Power Factor Correction Suitable for On-Chip Implementation," Power Conversion Conference - Nagoya, 2007. PCC '07 , pp.1527-1531, 2-5 April 2007
- [14] B.J. Patella,A. Prodic, A. Zirger, D. Maksimovic, "High-frequency digital controller IC for DC/DC converters," Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE , vol.1, pp.374-380 vol.1, 2002
- [15] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics. New York, NY: Springer Media Inc., 2001.
- [16] A. Radić, A. Prodić, "Buck Converter With Merged Active Charge-Controlled Capacitive Attenuation," IEEE Transactions on Power Electronics, vol.27, no.3, pp.1049-1054, March 2012
- [17] J. Sun, M. Xu, Y Ying, F.C. Lee, "High Power Density, High Efficiency System Two-stage Power Architecture for Laptop Computers," Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE , pp.1-7, 18-22 June 2006
- [18] R.C.N. Pilawa-Podgurski, D.M. Giuliano, D.J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in Proceedings of IEEE Power Electronics Specialist Conference, 2008, pp. 4008-4015, June 2008.
- [19] R. Aparicio, A. Hajimiri. "Capacity limits and matching properties of lateral flux integrated capacitors," in Proceedings of IEEE Customs Integrated Circuits Conference, 2001, pp. 365-368, May 2001.