Mixed-Signal Simulation of Digitally Controlled Switching Converters

Aleksandar Prodić and Dragan Maksimović

Colorado Power Electronics Center
Department of Electrical and Computer Engineering
University of Colorado at Boulder
Boulder, CO 80309-0425, USA
Aleksandar.Prodic@colorado.edu

Abstract – **In this paper we give an overview of tasks, models and mixed-signal simulation tools to support design of digitally controlled switching power supplies where the digital controller is implemented in a dedicated FPGA or ASIC. Mixed-signal simulation models of a digitally controlled switching converter based on Matlab/Simulink and HDL/Spice simulation tools are presented. The models are used in the design of a high-frequency digital controller integrated circuit for dc-dc switching converters. Simulation and experimental results are compared.**

I. INTRODUCTION

Because of significant advances in low-cost microprocessor and DSP systems, as well as dedicated FPGA or ASIC based digital controllers, it is expected that digital control will find increasing use in high-frequency switching power supplies. In general, digital control enables a number of advantages in the system, including greater flexibility, lower sensitivity, reduction or elimination of passive tuning components, programmability, etc., but at the same time it brings additional complexity to system analysis, simulation and design [1-3].

In this paper we consider digitally controlled converters where the controller is implemented in a dedicated FPGA or ASIC (as in [1,2]). Following standard digital design practices, the controller is described using hardware description language (HDL), such as Verilog or VHDL. Using synthesis tools, the design is then targeted to FPGA or ASIC implementation. The objective of this paper is to discuss modeling issues and simulation tools suitable for design verification in this design process.

The paper is organized as follows: an overview of HDL-based digital design procedure is given in Section II. In Section III, models and tools for different stages in the design are reviewed. Two mixed-signal models are presented in Section IV. Simulation and experimental results are compared in section V.

II. HARDWARE DESCRIPTION LANGUAGE (HDL) BASED DIGITAL CONTROLLER DESIGN

Design procedure of a digital system based on a hardware description language (Verilog or VHDL for example) is shown in Figure 1.

This work was supported by National Semiconductor Corp. through the Colorado Power Electronics Center.

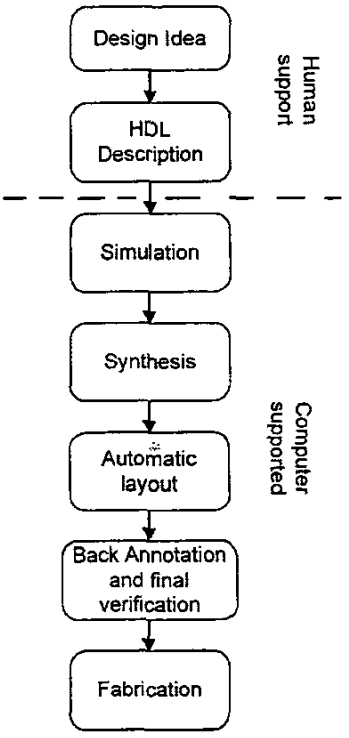

Figure 1. Design procedure of a digital system based on a hardware description language (HDL).

The process starts with a design idea and a system description through HDL code. The steps are highly automated through computer support: functionality of the digital system can be verified using specialized HDL simulators. Once the functionality is confirmed, a synthesis tool creates a gate-level netlist targeted to FPGA or ASIC implementation. At this stage, functional and timing verification of the design can be performed. In the case of ASIC design, place and route tools generate the chip layout. From the physical layout, it is possible to conduct extraction of parasitics (such as interconnect capacitances), back annotation and detailed design verification. Upon final verification that includes design-rule (DRC) and

layout versus schematic (LVS) checks, the ASIC can be submitted for fabrication.

In the design procedure of Figure 1, simulation support is necessary in all stages. Furthermore, a digitally controlled switching converter is a mixed-signal system, which is even more complex for simulation. In order to illustrate how the design process is supported by simulation models and tools, we discuss our experience in the design of the digital PWM controller ASIC described in [1,2].

Figure 2 shows a buck converter controlled by the digital controller integrated circuit that is used in simulation and experimental examples in this paper.

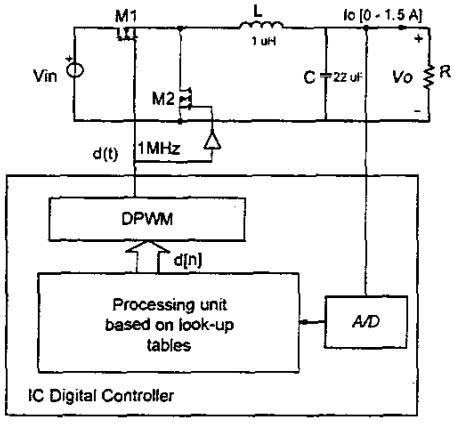

Figure 2. Design example: Buck converter controlled by digital controller integrated circuit.

III. SIMULATION TASKS, MODELS AND TOOLS

Table I gives an overview of tasks, models and mixed-signal simulation tools to support the design of digital controllers and digitally-controlled switching power supplies.

The top-level system design verification usually includes examination of small-signal frequency responses and large-signal transients. In addition to standard verification of input or load transient responses, time-domain simulations are also needed to examine effects specific for digital implementation such as nonlinear effects of limited resolution and fixed-point computations [4], including possible limit-cycle oscillations [4-6], and effects of processing delays. A simple behavioural model (i.e. equations) of the digital controller and an averaged model of the power stage are well suited for these tasks. To implement the models, we used the Matlab/Simuling environment. It has also been demonstrated how PSpice can be used for similar purposes, with added convenience from a circuit-design point of view [2].

Once the controller is described in HDL (such as Verilog [7]), it is essential to verify correct operation of the controller operation at two levels: behavioural and gate-level. Behavioural controller HDL model can be coupled with an averaged or a switched-circuit model of the power stage to examine correctness of interface signals between digital blocks and between digital blocks and the power stage. Once the digital controller design is synthesized to a gate-level HDL model, gate delays can be included to provide an additional level of timing verification. For mixed-signal simulations based on the HDL controller model and the averaged or switched-circuit model of the power stage, we used the Cadence Spectre/Verilog tool.

Finally, the most detailed simulation can be performed at the device level for both the controller and the power stage using detailed Spice models. However, such simulation is usually not practical because it is extremely time-consuming.

IV. MIXED-SIGNAL MODEL EXAMPLES

The block diagram of the controller chip is shown in Figure 3. The controller consists of an analog-to-digital converter, a look-up table based PID regulator, and a digital pulse width modulator.

A. Matlab/Simulink model

A Matlab/Simulink system model is shown in Figure 4. It includes behavioural models of all controller blocks and the power stage.

Analog-to-digital converter model consists of an element

Table I. Overview of mixed-signal simulation tasks and tools

Task	Controller model	Power stage model	Simulation tool
Frequency-domain simulation for verification of regulator design and small-signal frequency responses	Behavioral (equations)	Averaged	Matlab/Simulink or PSpice [2]
Time-domain simulation for verification of system design and transient responses	Behavioral (equations)	Averaged or switched-circuit	Matlab/Simulink or PSpice [2]
Time-domain simulation for detailed verification of digital controller design	Behavioral or gate-level (HDL)	Averaged or switched-circuit	Verilog/Spectre
Detailed time-domain simulation	Device-level (using Spice models)	Device level (using Spice models)	Spice (any version)

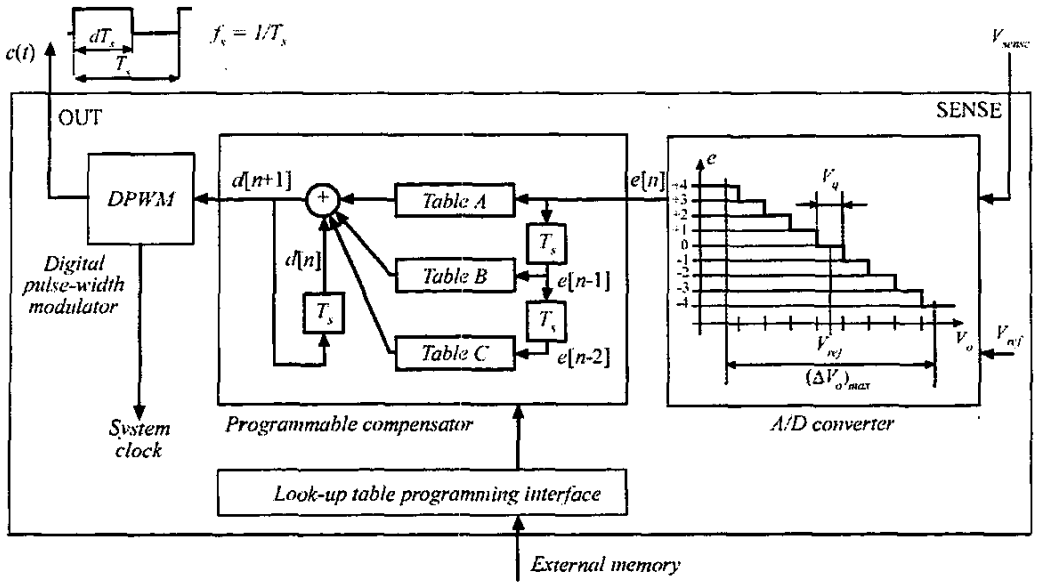

Figure 3. Block diagram of digital controller integrated circuit described in [1] and [2].

that performs subtraction of the output voltage value from the reference, converter's gain, sample and hold, quantization, delay, and saturation blocks. The PID controller model represents the equation:

$$d[n] = d[n-1] + ae[n] + be[n-1] + ce[n-2] \qquad (1)$$

where, $d[n]$ is the discrete value at the output of PID regulator, $e[n]$ is discrete value of the error signal at the output of the analog-to-digital converter, $d[n-i]$ and $e[n-i]$ are the output and the error values i-cycles before the current cycle, respectively, while the coefficients a, b and c are the controller coefficients. In the considered design example, the DPWM model truncation of the input (which

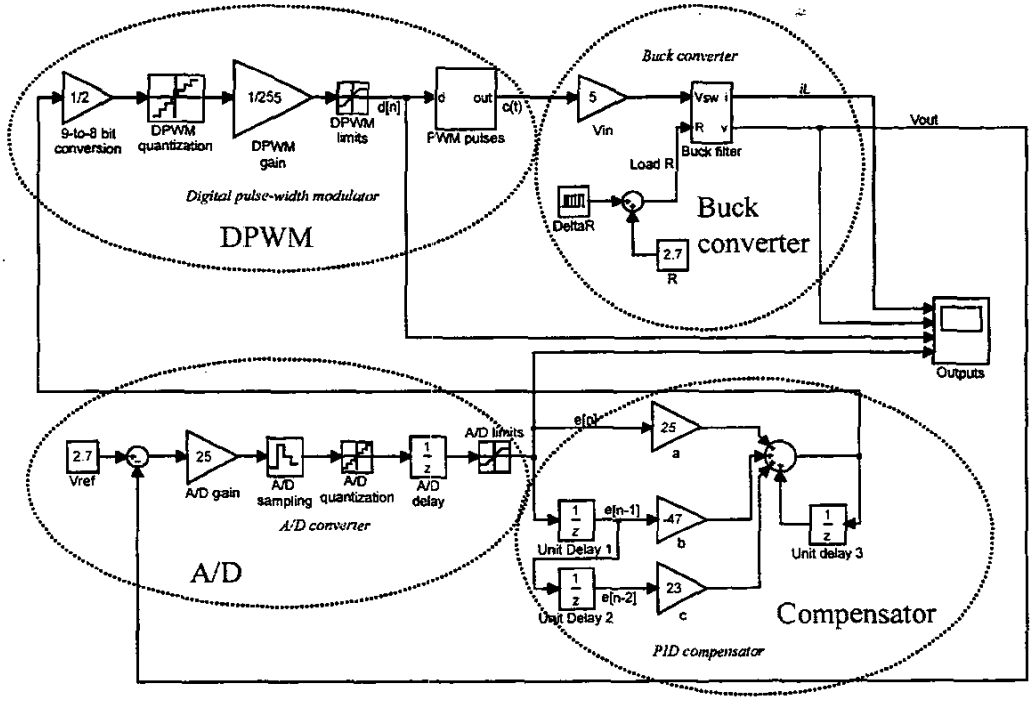

Figure 4. Matlab/simulink model of a buck converter controlled by the digital controller integrated circuit.

is a 9-bit value) to the 8-bit DPWM resolution. A quantizer is followed by a gain block and a 0-to-1 limiter. Finally, a pulse-width modulator generates the output pulses with the duty cycle corresponding to the input value.

The buck converter is modelled as a pulsating input voltage, a state-space model of the buck L-C filter, and a load resistor that can be changed in order to simulate load transients.

This top-level model provides fast simulation and conceptual system verification. Effects of processing delay, quantization and fixed-point computations with limited resolution can be examined.

B. Verilog/Spice Model

Detailed verification of the HDL-based digital controller and the power-stage circuit requires a mixed-signal model supported by a combination of digital and analog simulation tools.

Figure 5 shows a mixed-signal Spice/Verilog model of the digitally controlled switching converter.

In this case the system is divided into two parts, HDL-described digital controller and analog power stage. To speed-up the simulation, a behavioural (Verilog-A) model of the A/D converter is included. The digital part consists of a decoder, PID regulator and a digital pulse width modulator. The analog and the digital block communicate with each other through the analog-to-digital converter and the digital pulse width modulator. The entire system is simulated using the Cadence Spectre/Verilog mixed-signal tool.

An important advantage of the mixed-signal simulation approach is that the same behavioral HDL description used for simulation leads to the digital controller implementation via synthesis tools that produce equivalent gate-level netlists. In addition, the power stage can be modeled either using idealized models to speed-up long-term transient simulations, or using detailed Spice models to examine details of switching transitions and losses.

V. SIMULATION AND EXPERIMENTAL RESULTS

The mixed-signal models described in Section III are used in the design of the buck converter operating at the switching frequency of 1 MHz, and controlled by the ASIC described in [1,2]. The block diagram of the system is shown in Figures 2 and 3.

Figure 6 shows results of Matlab/Simulink simulation of the system for the case when the resolution of the digital pulse width modulator is too low, causing "limit cycle" oscillations [4-6].

Figures 7.a and 7.b compare load transient responses obtained by Matlab/Simuling simulation with experimental results. experimental results.

Figure 8 shows load transient response simulation results obtained using the mixed-signal Spice/Verilog simulation. This simulation over 200 switching cycles (the switching frequency is 1 MHz) using the Spectre/Verilog simulator on Sun Ultra 10 workstation took several minutes. In comparison, an all-analog simulation of the same system takes several hours per switching cycle.

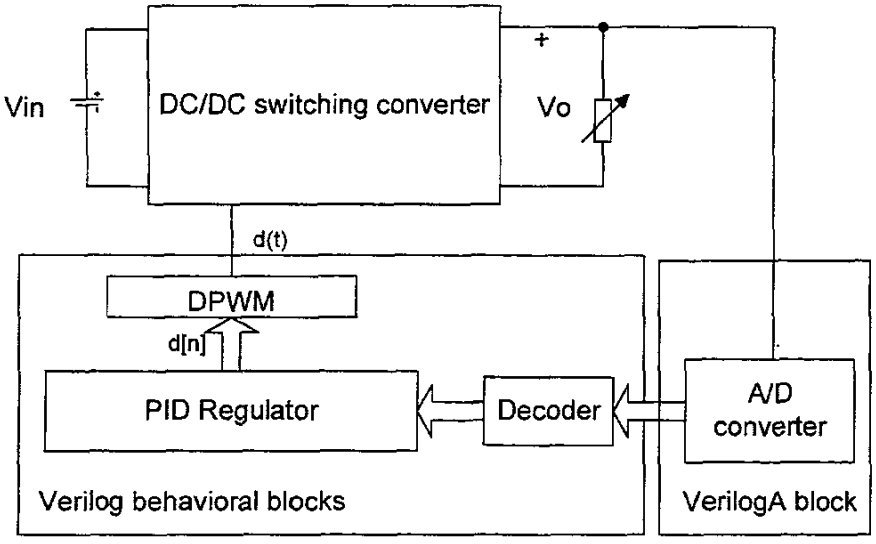

Figure 5. Verilog/Spice model of a digitally controlled switching converter.

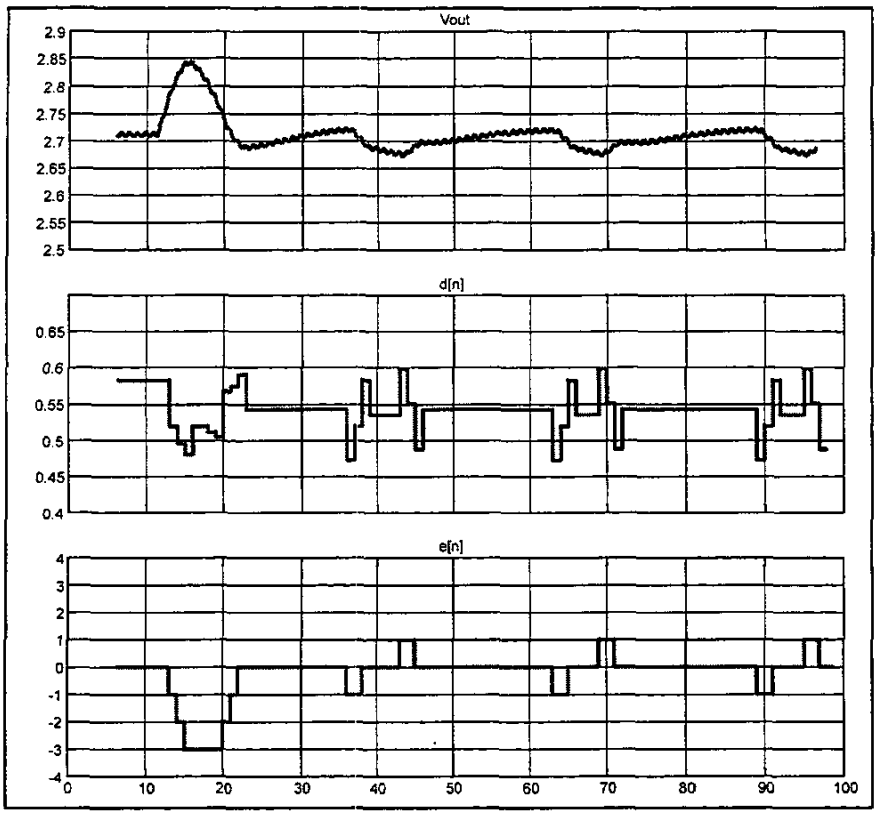

Figure 6. Matlab/Simulink simulation of a load transient followed by limit-cycle oscillations.

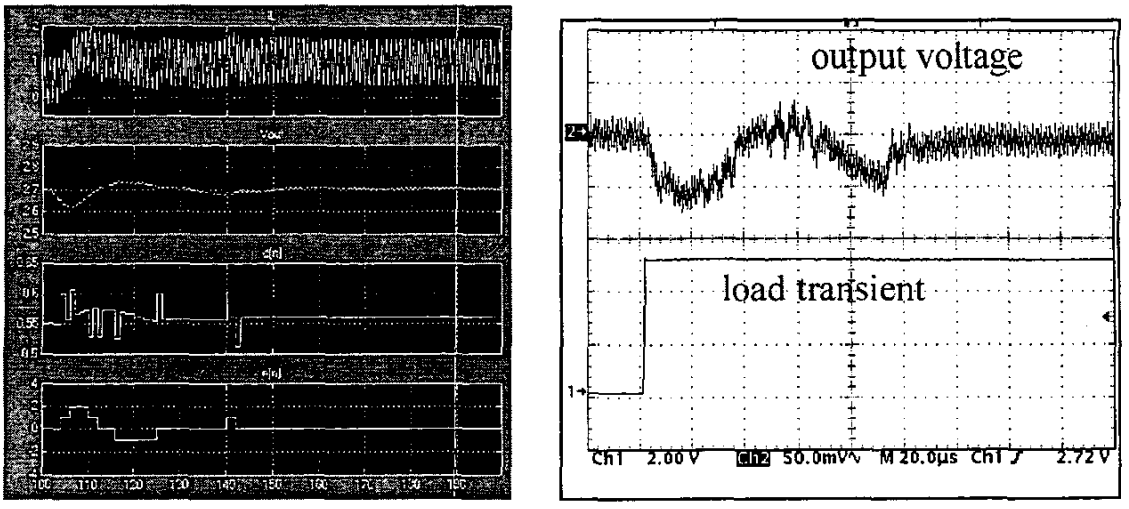

Figure 7. Load transient response for the output current change from 0.3 A to 1 A (Left hand side) simulation results obtained using the Matlab/Simulink model: (Right hand side) experimental results.

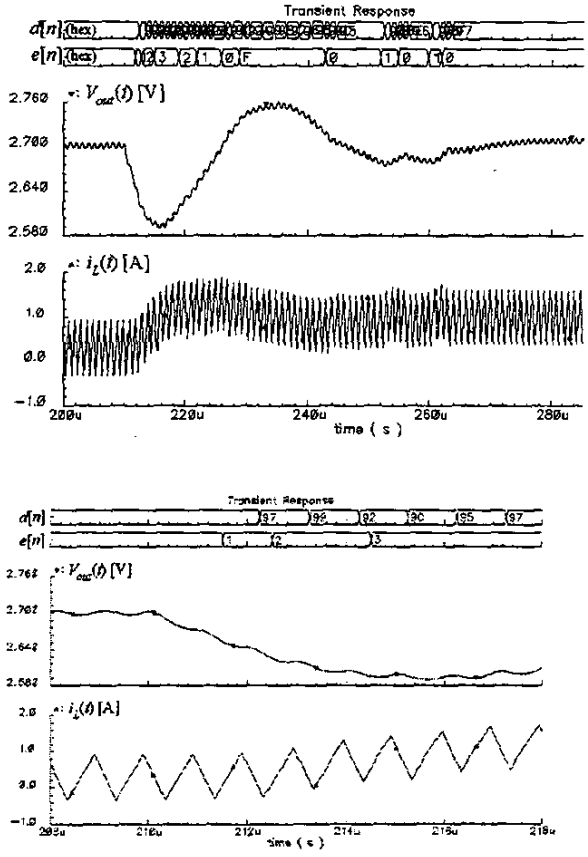

Figure 8. Load transient response results obtained using mixed-signal Spice/Verilog simulation.

IV. CONCLUSIONS

In this paper we give an overview of tasks, models and mixed-signal simulation tools to support the design of digitally-controlled switching power supplies where the digital controller is implemented in a dedicated FPGA or ASIC. Two mixed-signal simulation models are described, together with a comparison of simulation and experimental results.

VI. REFERENCES

[1] B. Patella, "Implementation of a High Frequency, Low-Power Digital Pulse Width Modulation Controller Chip," M.S. Thesis, University of Colorado at Boulder, 2000.

[2] B. Patella, A. Prodic, A. Zirger, and D. Maksimovic "High-Frequency Digital Controller IC for DC/DC Converters," IEEE Applied Power Electronics Conference, 2002.

[3] D. Adar and S. Ben-Yaakov, "Generic Average Modeling and Simulation of Discrete Controllers," IEEE APEC 2001.

[4] A. Prodic, D. Maksimovic, and R. W. Erickson "Design and Implementation of a Digital PWM Controller for a High-Frequency Switch DC-DC Power Converters," IEEE IECON 2001.

[5] A. V. Petrechev, S. R. Sanders, "Quantization Resolution and Limit-Cycle in Digitally Controlled PWM Converters," IEEE Power Electronics Specialists Conference, 2001, pp. 465-471.

[6] Z. Lu, Z.Qian, Y. Zeng, "Reduction of Digital PWM Limit Ring with Novel Control Algorithm," IEEE Applied Power Electronics Conference 2001, Vol.1, 1995, pp. 521-534.

[7] Samir Planitkar, *Verilog HDL: A Guide to Digital Design and Synthesis* – Prentice Hall, 1996.